

NTR4503N

Power MOSFET

30 V, 2.5 A, Single N-Channel, SOT-23

Features

- Leading Planar Technology for Low Gate Charge / Fast Switching
- 4.5 V Rated for Low Voltage Gate Drive
- SOT-23 Surface Mount for Small Footprint (3 x 3 mm)
- Pb-Free Package is Available

Applications

- DC-DC Conversion
- Load/Power Switch for Portables
- Load/Power Switch for Computing

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	30	V
Gate-to-Source Voltage			V _{GS}	±20	V
Continuous Drain Current (Note 1)	Steady State	T _A = 25°C	I _D	2.0	A
		T _A = 85°C		1.5	
	t ≤ 10 s	T _A = 25°C	2.5		
Power Dissipation (Note 1)	Steady State	T _A = 25°C	P _D	0.73	W
Continuous Drain Current (Note 2)	Steady State	T _A = 25°C	I _D	1.5	A
		T _A = 85°C		1.1	
Power Dissipation (Note 2)		T _A = 25°C	P _D	0.42	W
Pulsed Drain Current	t _p = 10 μs		I _{DM}	6.0	A
ESD Capability (Note 3)	C = 100 pF, RS = 1500 Ω		ESD	125	V
Operating Junction and Storage Temperature			T _J , T _{stg}	-55 to 150	°C
Source Current (Body Diode)			I _S	2.0	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	R _{θJA}	170	°C/W
Junction-to-Ambient – t < 10 s (Note 1)	R _{θJA}	100	
Junction-to-Ambient – Steady State (Note 2)	R _{θJA}	300	

1. Surface-mounted on FR4 board using 1 in sq pad size.
2. Surface-mounted on FR4 board using the minimum recommended pad size.
3. ESD Rating Information: HBM Class 0.

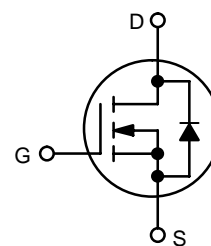


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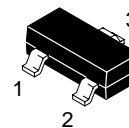
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V _{(BR)DSS}	R _{DS(on)} TYP	I _D MAX
30 V	85 mΩ @ 10 V	2.5 A
	105 mΩ @ 4.5 V	

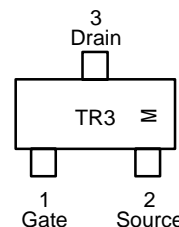
N-Channel



MARKING DIAGRAM/ PIN ASSIGNMENT



SOT-23
CASE 318
STYLE 21



TR3 = Specific Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
NTR4503NT1	SOT-23	3000/Tape & Reel
NTR4503NT1G	SOT-23 (Pb-Free)	3000/Tape & Reel
NTR4503NT3G	SOT-23 (Pb-Free)	10000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30	36		V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$			1.0	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}, T_J = 125^\circ\text{C}$			10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.0	1.75	3.0	V
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 2.5\text{ A}$		85	110	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 2.0\text{ A}$		105	140	
Forward Transconductance	g_{FS}	$V_{DS} = 4.5\text{ V}, I_D = 2.5\text{ A}$		5.3		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 15\text{ V}$		135		pF
Output Capacitance	C_{oss}			52		
Reverse Transfer Capacitance	C_{rss}			15		
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 24\text{ V}$		130	250	pF
Output Capacitance	C_{oss}			42	75	
Reverse Transfer Capacitance	C_{rss}			13	25	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 2.5\text{ A}$		3.6	7.0	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.3		
Gate-to-Source Charge	Q_{GS}			0.6		
Gate-to-Drain Charge	Q_{GD}			0.7		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 24\text{ V}, I_D = 2.5\text{ A}$		1.9		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.3		
Gate-to-Source Charge	Q_{GS}			0.6		
Gate-to-Drain Charge	Q_{GD}			0.9		

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DD} = 15\text{ V}, I_D = 1\text{ A}, R_G = 6\ \Omega$		5.8	12	ns
Rise Time	t_r			5.8	10	
Turn-Off Delay Time	$t_{d(off)}$			14	25	
Fall Time	t_f			1.6	5.0	
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DD} = 24\text{ V}, I_D = 2.5\text{ A}, R_G = 2.5\ \Omega$		4.8		ns
Rise Time	t_r			6.7		
Turn-Off Delay Time	$t_{d(off)}$			13.6		
Fall Time	t_f			1.8		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 2.0\text{ A}$		0.85	1.2	V
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, I_S = 2.0\text{ A}, dI_S/dt = 100\text{ A}/\mu\text{s}$		9.2		ns
Reverse Recovery Charge	Q_{RR}			4.0		nC

4. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.

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TYPICAL PERFORMANCE CURVES

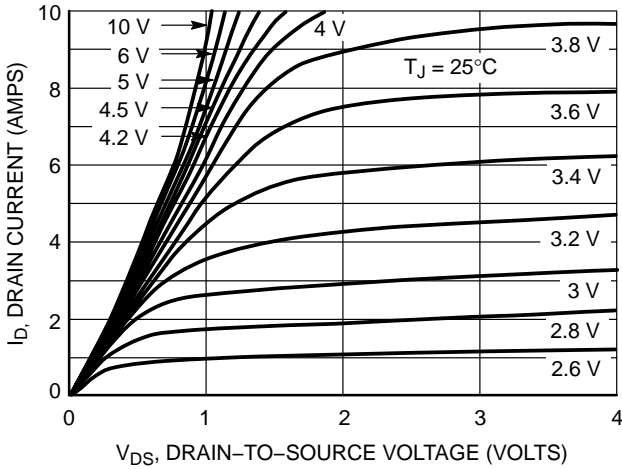


Figure 1. On-Region Characteristics

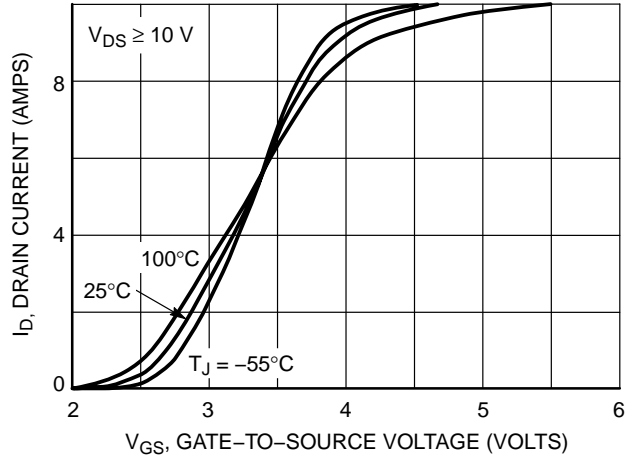


Figure 2. Transfer Characteristics

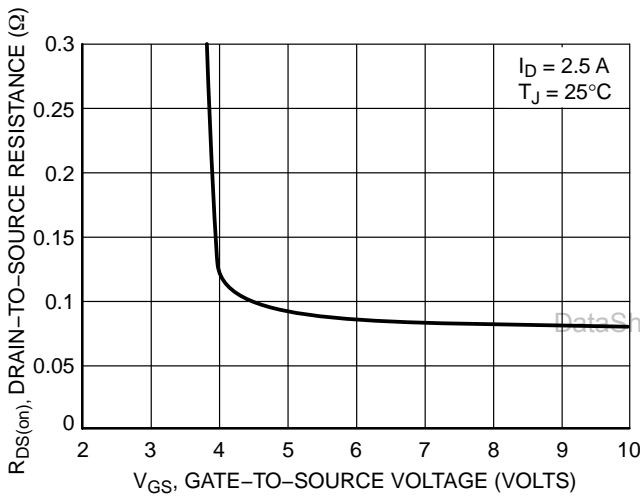


Figure 3. On-Resistance vs. Gate-to-Source Voltage

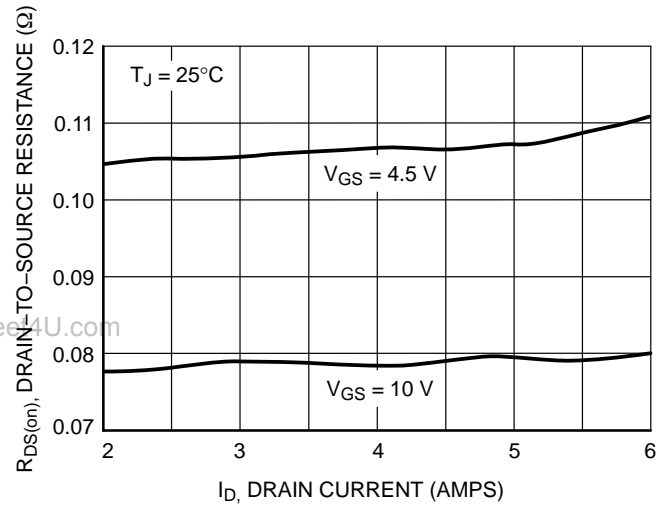


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

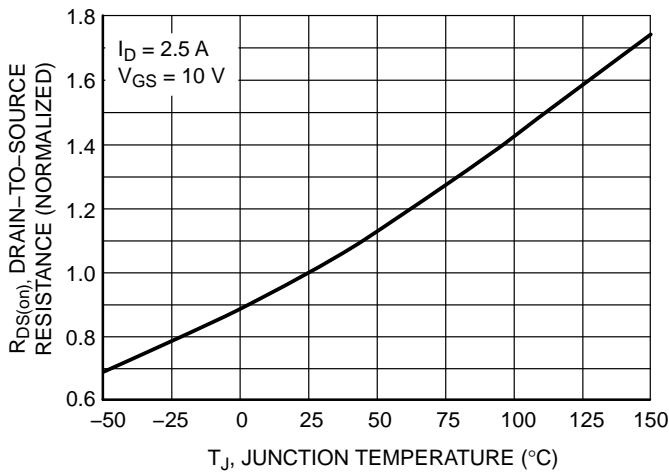


Figure 5. On-Resistance Variation with Temperature

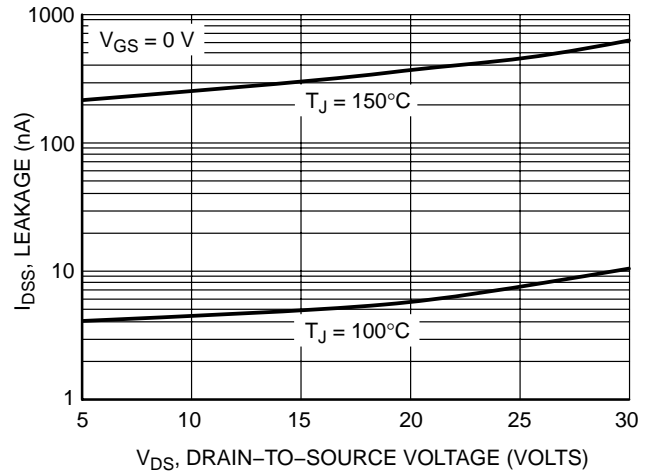


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL PERFORMANCE CURVES

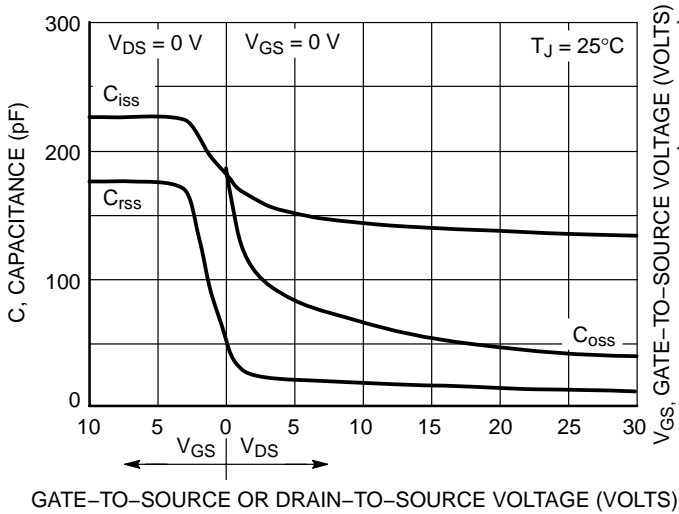


Figure 7. Capacitance Variation

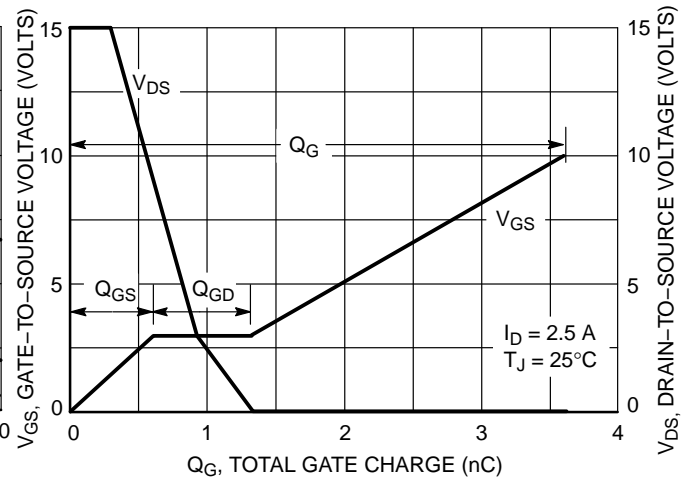


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

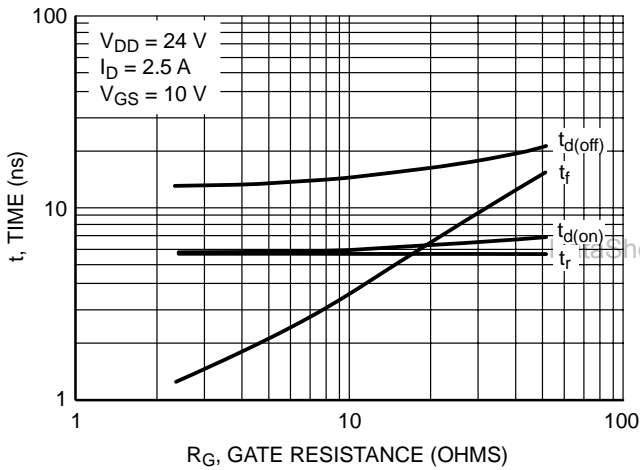


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

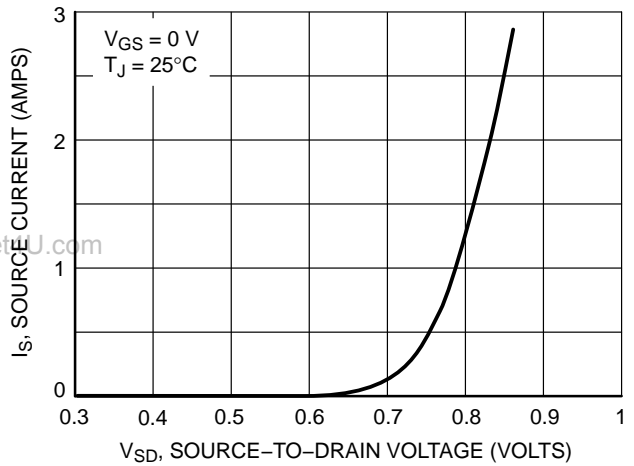


Figure 10. Diode Forward Voltage vs. Current

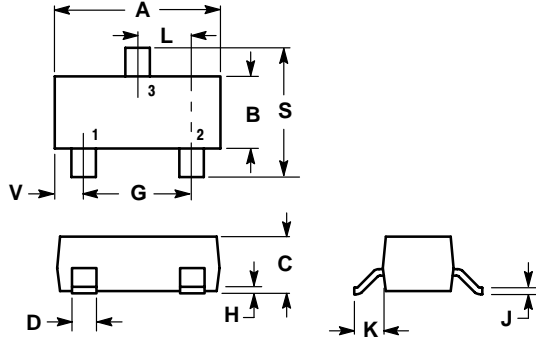
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DataShee

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PACKAGE DIMENSIONS

**SOT-23
(TO-236)
CASE 318-08
ISSUE AK**

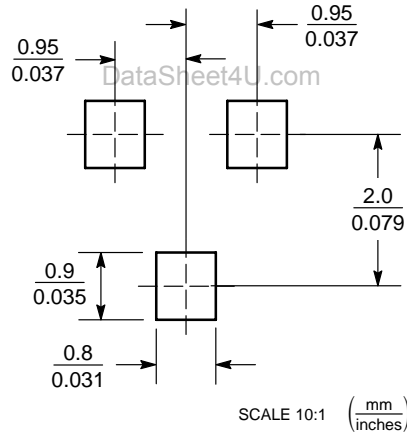


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
 4. 318-01 THRU -07 AND -09 OBSOLETE, NEW STANDARD 318-08.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

- STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

SOLDERING FOOTPRINT*




*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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