NTR0202PL

Power MOSFET
−20 V, −400 mA, P−Channel
SOT−23 Package

ON Semiconductor®

http://onsemi.com

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
−20 V	550 mΩ @ −10 V	−400 mA

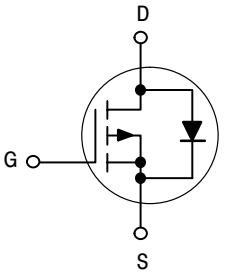
Features

- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
  R_{DSon} = 0.80 Ω, V_{GS} = −10 V
  R_{DSon} = 1.10 Ω, V_{GS} = −4.5 V
- Miniature SOT−23 Surface Mount Package Saves Board Space
- Pb−Free Package is Available

Applications

- DC−DC Converters
- Computers
- Printers
- PCMCIA Cards
- Cellular and Cordless Telephones

P−Channel



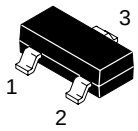
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	−20	V
Gate−to−Source Voltage − Continuous	V_{GS}	±20	V
Continuous Drain Current @ T_A = 25°C Pulsed Drain Current ($t_p \le 10$ μs)	I_D I_{DM}	−0.4 −1.0	A
Total Power Dissipation @ T_A = 25°C (Note 1)	P_D	225	mW
Operating and Storage Temperature Range	T_J, T_{stg}	− 55 to 150	°C
Thermal Resistance − Junction−to−Ambient	$R_{\theta JA}$	556	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 s	T_L	260	°C

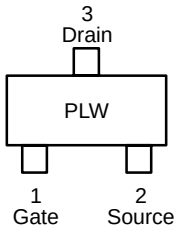
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

MARKING DIAGRAM/ PIN ASSIGNMENT



SOT−23
CASE 318
STYLE 21



PL = Specific Device Code
W = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NTR0202PLT1	SOT−23	3000 Tape & Reel
NTR0202PLT1G	SOT−23 (Pb−Free)	3000 Tape & Reel
NTR0202PLT3	SOT−23	10,000 Tape & Reel
NTR0202PLT3G	SOT−23 (Pb−Free)	10,000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (V_{GS} = 0 V, I_D = −10 μA) (Positive Temperature Coefficient)		$V_{(BR)DSS}$	−20	 33		V mV/°C
Zero Gate Voltage Drain Current (V_{DS} = −20 V, V_{GS} = 0 V, T_J = 25°C) (V_{DS} = −20 V, V_{GS} = 0 V, T_J = 150°C)		I_{DSS}			 −1.0 −10	μA
Gate−Body Leakage Current (V_{GS} = ± 20 V, V_{DS} = 0 V)		I_{GSS}			±100	nA
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = −250 μA) (Negative Temperature Coefficient)		$V_{GS(th)}$	−1.1	−1.9 3.0	−2.3	V mV/°C
Static Drain−to−Source On−Resistance (V_{GS} = −10 V, I_D = −200 mA) (V_{GS} = −4.5 V, I_D = −50 mA)		$R_{DS(on)}$		 0.55 0.80	 0.80 1.10	Ω
Forward Transconductance (V_{DS} = −10 V, I_D = −200 mA)		g_{fs}		0.5		Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = −5.0 V, V_{GS} = 0 V, F = 1.0 MHz)	C_{iss}		70		pF
Output Capacitance		C_{oss}		74		
Reverse Transfer Capacitance		C_{rss}		26		
SWITCHING CHARACTERISTICS (Note 3)						
Turn−On Delay Time	(V_{DD} = −15 V, I_D = −200 mA, V_{GS} = −10 V, R_G = 6.0 Ω)	$t_{d(on)}$		3.0		ns
Rise Time		t_r		6.0		
Turn−Off Delay Time		$t_{d(off)}$		18		
Fall Time		t_f		4		
Total Gate Charge	(V_{DS} = −15 V, I_D = −200 mA, V_{GS} = −10 V)	Q_{TOT}		2.18		nC
Gate−Source Charge		Q_{GS}		0.41		
Gate−Drain Charge		Q_{GD}		0.40		
BODY−DRAIN DIODE CHARACTERISTICS (Note 2)						
Diode Forward Voltage (Note 2) (I_S = −400 mA, V_{GS} = 0 V) (I_S = −400 mA, V_{GS} = 0 V, T_J = 150°C)		V_{SD}		 −0.8 −0.65	−1.0	V
Reverse Recovery Time	(I_S = −1.0 A, V_{GS} = 0 V, dI_S/dt = 100 A/μs)	t_{rr}		11.8		ns
		t_a		9		
		t_b		3		
Reverse Recovery Stored Charge	(I_S = −1.0 A, V_{GS} = 0 V, dI_S/dt = 100 A/μs)	Q_{RR}		0.007		μC

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

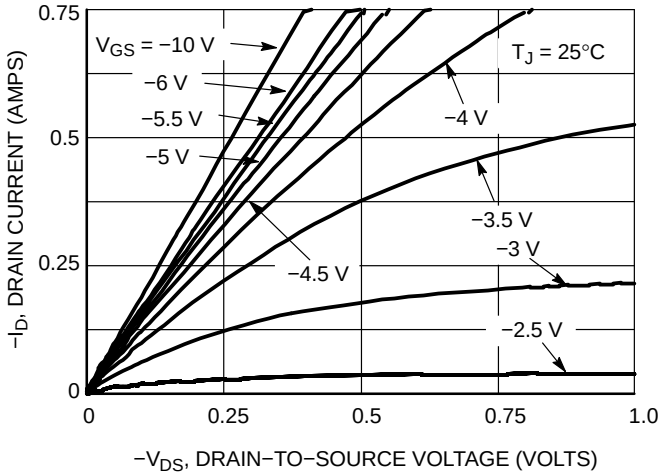


Figure 1. On−Region Characteristics

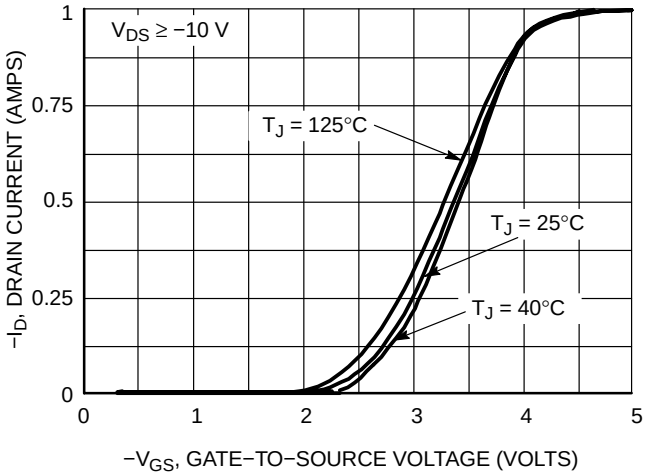


Figure 2. Transfer Characteristics

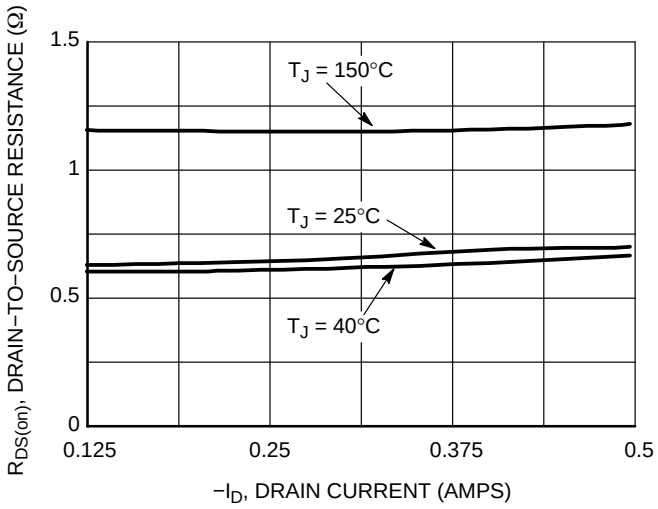


Figure 3. On−Resistance versus Drain Current

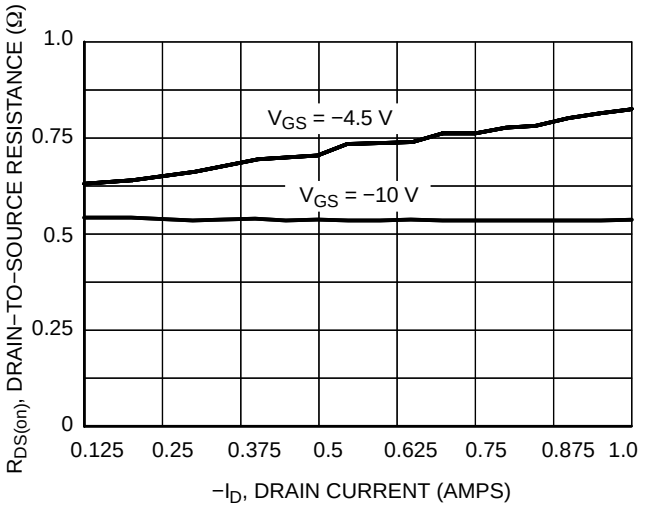


Figure 4. On−Resistance versus Drain Current and Gate Voltage

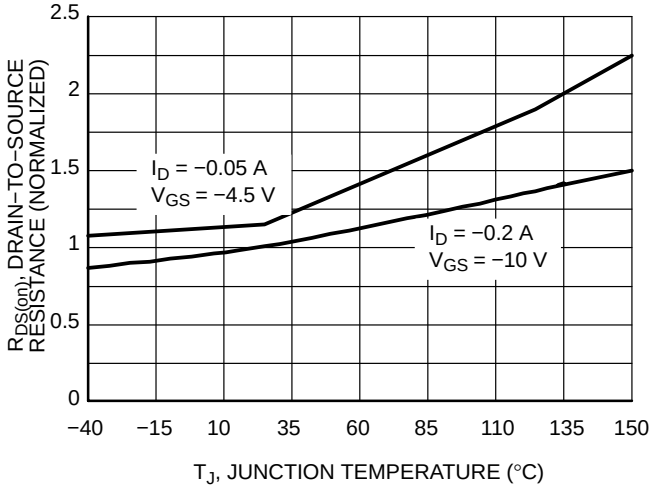


Figure 5. On−Resistance Variation with Temperature

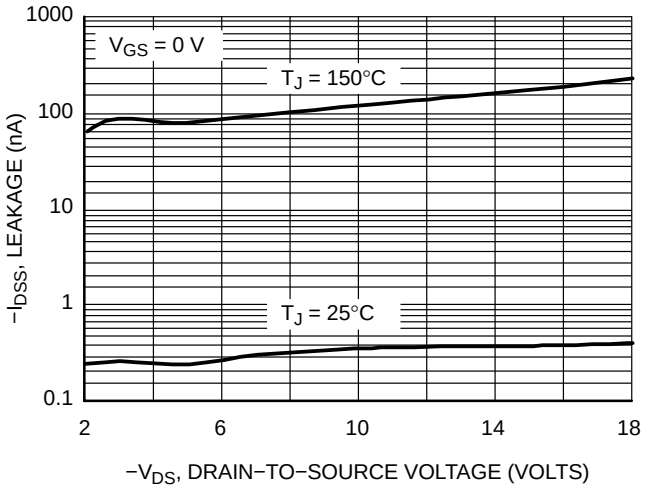


Figure 6. Drain−to−Source Leakage Current versus Voltage

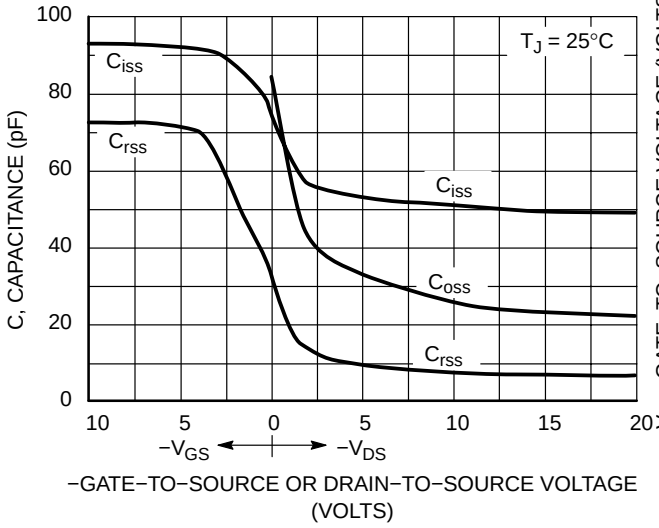


Figure 7. Capacitance Variation

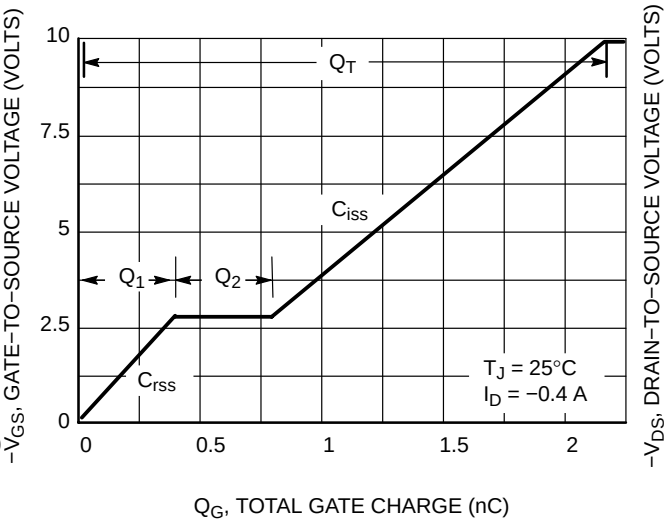


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

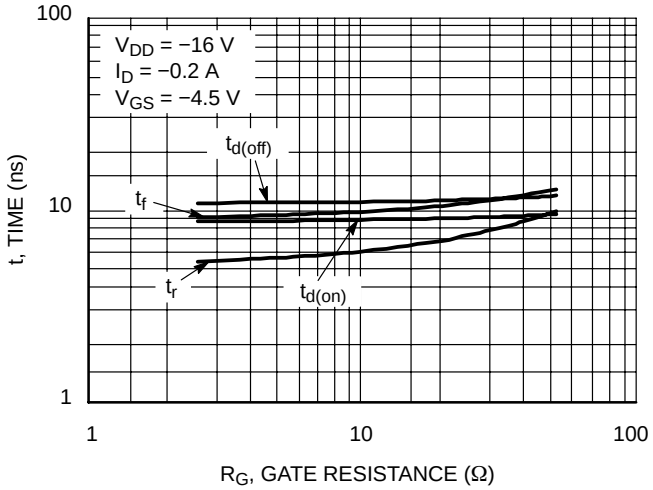


Figure 9. Resistive Switching Time Variation versus Gate Resistance

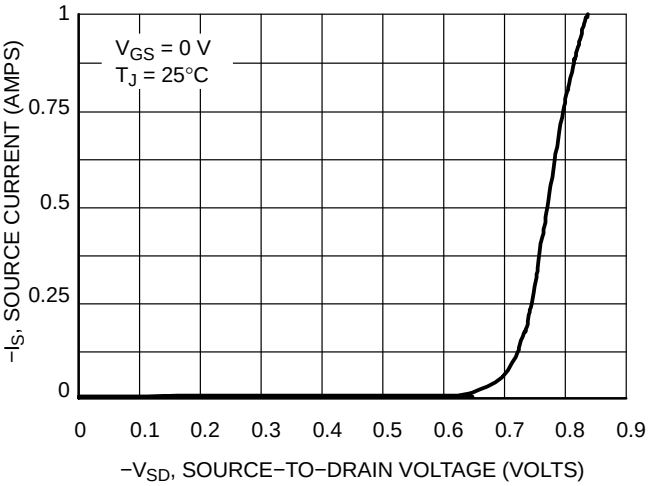
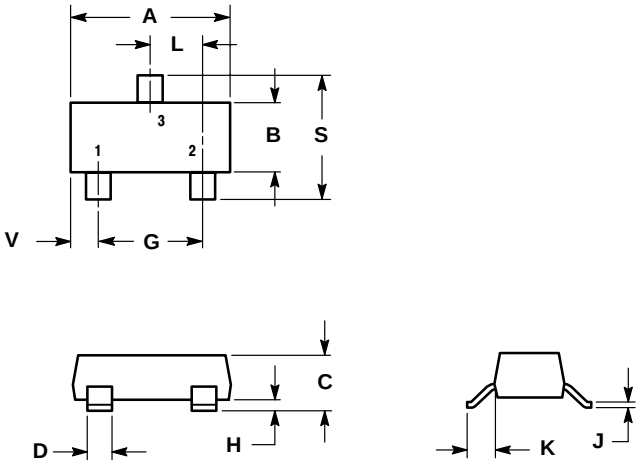


Figure 10. Diode Forward Voltage versus Current

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−09
ISSUE AJ

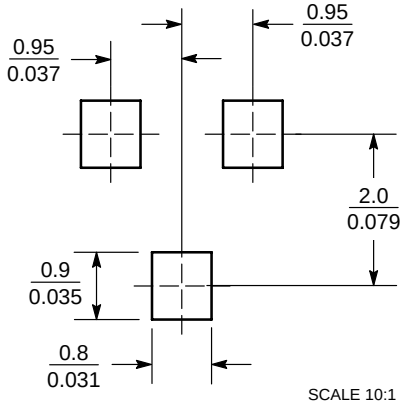


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−01, −02, AND −06 OBSOLETE, NEW STANDARD 318−09.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0385	0.0498	0.99	1.26
D	0.0140	0.0200	0.36	0.50
G	0.0670	0.0826	1.70	2.10
H	0.0040	0.0098	0.10	0.25
J	0.0034	0.0070	0.085	0.177
K	0.0180	0.0236	0.45	0.60
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.0984	2.10	2.50
V	0.0177	0.0236	0.45	0.60

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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