Application Note

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Interfacing SDRAM Devices to the MPC8280 at 100 MHz

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The demand for ever higher bus frequencies when using MPC8260 PowerQUICC II™ communications processors has led to the introduction of the enhanced MPC8280 PowerQUICC II family—the MPC8280, the MPC8275, and the MPC8270 (collectively referred to in this document as the MPC8280). PowerQUICC II family members contain PowerPC™ processor cores.

This document discusses the interface of SDRAM memory devices using the MPC8280 on-chip SDRAM controller operating with a bus frequency of 100 MHz.

1 Introduction

The MPC8280 is similar to the MPC8260 family of devices except that it has been implemented in Motorola's advanced .13-µm (HiP7) process, which allows the devices to operate at higher clock frequencies.

The major enhancements to the MPC8280 compared with earlier MPC8260 devices are as follows:

- System core microprocessor supporting frequencies of 166–450 Mhz
- CPM dual-port RAM (original MPC8260 has the 24 Kbytes)
  - 32 Kbytes CPM RISC data RAM for storage of protocol parameters
  - 32 Kbytes CPM RISC instruction RAM for storage of CPM microcode
- Reduced core supply voltage of 1.45–1.6 V
- Bus frequency of 100 MHz
- Communication interfaces
  - ATM: Extended number of PHYs for FCC2 (MPC8280 only)
  - Internal rate scheduling for 31 PHYs
  - RMII interface
- Universal serial bus (USB) controller

The increased bus frequency of 100 MHz leads to some restrictions on the interface bus due to the shorter cycle time. These restrictions require the use of faster memory devices with reduced setup and hold time requirements. We will now consider the bus interface in more detail.

2 Bus Interface Timing Specifications

The interaction of several of the 60x bus interface signals is shown in Figure 1. Table 1 and Table 2 show the timing parameters associated with the 60x bus interface when it is operating at 100 MHz.

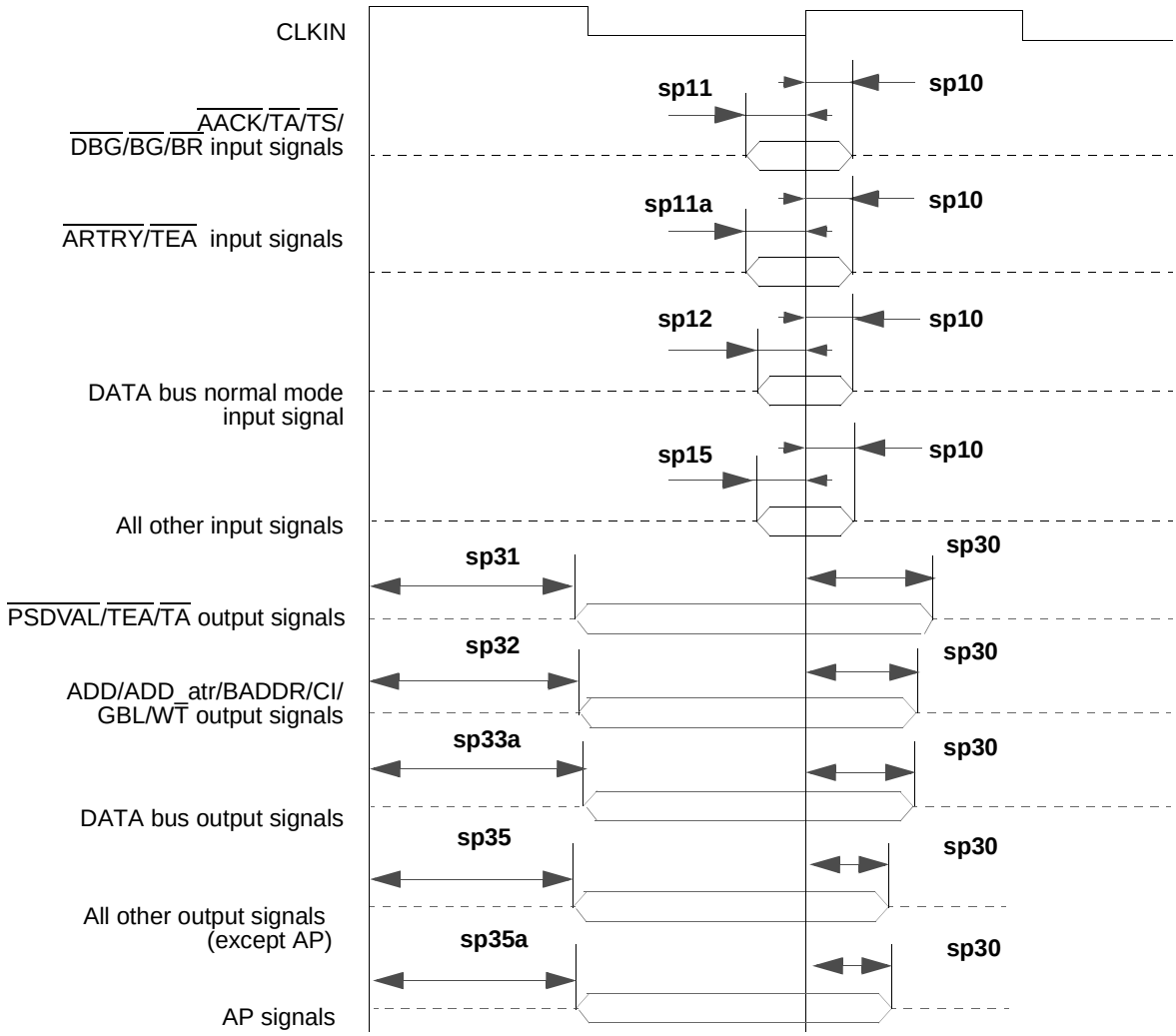

Figure 1. 60x Bus Signals

Table 1. AC Characteristics for SIU Inputs [1]

Spec Number		Characteristic	Value (ns)	
Setup	Hold		Setup	Hold
			100 MHz	100 MHz
sp11	sp10	$\overline{\text{AACK}}/\overline{\text{TA}}/\overline{\text{TS}}/\overline{\text{DBG}}/\overline{\text{BG}}/\overline{\text{BR}}$	3.5	0.5
sp11a	sp10	$\overline{\text{ARTRY}}/\ \overline{\text{TEA}}$	4	0.5
sp12	sp10	Data bus in normal mode	3.5	0.5
sp13	sp10	Data bus in ECC and PARITY modes	3.5	0.5
sp13a	sp10	Pipeline mode—Data bus in ECC and PARITY modes	2.5	0.5
sp14	sp10	DP pins	3.5	0.5
sp14a	sp10	Pipeline mode—DP pins	2.5	0.5
sp15	sp10	All other pins	3.5	0.5

[1] Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Table 2. AC Characteristics for SIU Outputs [1]

Spec Number		Characteristic	Value (ns)	
Max	Min		Maximum Delay	Minimum Delay
			100 MHz	100 MHz
sp31	sp30	$\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$	5.5	1
sp32	sp30	ADD/ADD_atr/BADDR/CI/GBL/WT	5.5	1
sp33a	sp30	Data bus	5.5	0.7
sp33b	sp30	DP	5.5	1
sp34	sp30	Memory controller signals/ALE	5.5	1
sp35	sp30	All other signals	5.5	1
sp35a	sp30	AP	7	1

[1] Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

Activating the data pipeline mode by setting BRx[DR] in the memory controller improves the AC timing because data beat accesses to memory controller address spaces are delayed by one cycle.With this mode enabled the output timing for the data bus and DP pins are the same as the timing for a normal bus.

3 Interface to SDRAM at 100 MHz

The on-chip SDRAM controller on the MPC8280 is designed to provide a 'glueless' interface to standard SDRAM devices and DIMM modules. The electrical specification for standard SDRAM devices defines the following timing:

- Inputs
  - Setup time for ADDRESS, DATA, CS, RAS, CAS, WE, DQM is 1.5 ns minimum
  - Hold time for all signals is 0.8 ns
- Outputs
  - Data output hold time is a minimum of 3 ns for normal loads and 1.8 ns for a low load situation

3.1 MPC8280 Writing to SDRAM

At a bus frequency of 100 MHz the cycle time is 10 ns. When the MPC8280 writes to the SDRAM the address and address attributes are valid at a maximum 5.5 ns (sp32/sp30) after a rising clock edge. The SDRAM requires a minimum 1.5 ns of setup time before the next rising edge.

Therefore, this allows 10 – 5.5 – 1.5 = 3 ns for clock skew and track delay in the interface. The MPC8280 outputs the data also at a maximum of 5.5 ns (sp33a/sp30) after a rising clock edge and the SDRAM requires only a minimum setup time of 1.5 ns for data.

This allows 10 – 5.5 – 1.5 = 3 ns for clock skew and track delay. The MPC8280 maintains the data for 0.7 ns after the clock edge or for 1 ns after the clock edge if the load is greater than 20 pF. The SDRAM device requires a hold time of 0.8 ns. Therefore, there is a margin of 0.2 ns because the control signals from the MPC8280 are held for 1 ns and the SDRAM device only requires 0.8 ns.

3.2 MPC8280 Reading from SDRAM

During a read cycle from the MPC8280 to the SDRAM the address and address attributes are valid at a maximum of 5.5 ns (sp32/sp30) after a rising clock edge. The SDRAM requires a minimum of 1.5 ns of setup time before the next rising edge. This again allows 10 – 5.5 – 1.5 = 3 ns for clock skew and track delay. The SDRAM outputs the required data at a maximum of 5.4 ns after the rising clock edge for a PC133 SDRAM with a CAS latency of 3. The MPC8280 requires 3.5 ns (sp12/sp10) for setup time. This leaves 10 – 5.4 – 3.5 = 1.1 ns for clock skew and track delay.

The SDRAM maintains the data for 3 ns for normal load but only 1.8 ns for low loads. The MPC8280 requires a hold time of only 0.5 ns. Therefore, even with a low load there is a margin of 1.8 – 0.5 = 1.3 ns. Again, the control signals from the MPC8280 are held for 1 ns and the SDRAM device requires only 0.8 ns. Therefore there is a margin of 0.2 ns for track delay and clock skew.

3.3 Restriction on the Interface to SDRAM

The above timing analysis shows that for an ideal situation with zero clock skew between the MPC8280 and the SDRAM the timing requirements are all met. The 0.2-ns margin is small but, assuming a PCB track delay of approximately 0.1 ns per inch, the margin allows for track lengths of up to 2 inches (5 cm).

In a real design there will be clock skew present between the MPC8280 and the SDRAM that will negatively affect the margins. However, there will also be longer track lengths that will have a positive effect by increasing the signal delay.

If, in a system with a clock driver with a 0.1-ns skew between the SDRAM clock and the MPC8280 clock, we assume an equal track length between the clock driver and the MPC8280 and the clock driver and the SDRAM, there is still a margin of 0.1 ns in the interface. Also, the longer tracks between the MPC8280 and the SDRAM add more margin to both the read and write cycles.

For further information on implementing clock skew and track delay into a design, please refer to the "Timing Considerations when Interfacing PQII to SDRAM" white paper that is detailed in Section 4, "Reference Material."

4 Reference Material

The documents listed in Table 3 are all available at http://www.motorola.com/semiconductors/:

Table 3.

Title	Document Order Number
MPC8260 PowerQUICC II™ Family Reference Manual	MPC8260UM
MPC8280 Addendum to the MPC8260 PowerQUICC II Family Reference Manual	MPC8280UMAD
"MPC8280 PowerQUICC II Family Device Errata"	MPC8280CE
"MPC8280 Family Hardware Specifications"	MPC8280EC
"MPC8260 PowerQUICC II Design Checklist"	AN2290
"MPC8260 SDRAM Timing Diagram"	AN2178
"Timing Considerations when Interfacing the PowerQUICC II to SDRAM"	MPC826XSDRAMWP

5 Conclusion

The above analysis has shown that with careful design practice the MPC8280 will have a glueless interface to standard SDRAM memory devices while operating at bus frequencies up to and including 100 MHz.

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