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The Universal Serial Bus (USB) protocol is a hardware bus interface that was introduced in 1997 to connect peripherals such as a keyboard, mouse, joystick, scanner, printer and telephony devices to a PC. USB specification 1.1 has a maximum bandwidth of 12 Mbps and up to 127 devices can be attached. Full-speed devices use the full 12 Mbps bandwidth, while low-speed devices can transfer data using a 1.5 Mbps subchannel. Revision 2.0 of the USB specification added a high-speed mode with an increased bandwidth of 480 Mbps. As well as the increased bandwidth, USB 2.0 introduced new functionality to the 1.1 standard, namely USB On-The-Go (OTG).

Today, many portable devices can be connected to the PC to exchange data, such as portable digital assistants, mobile phones, digital cameras, and portable storage devices. As these portable devices become more technologically advanced, there is less of a need to connect them directly to a PC. Subsequently, it would be more beneficial to the user to connect them directly to each other without the need of a PC. For example, at the moment, to print out photographs taken with a digital camera, the user has to download the images to a PC. The PC must be connected to a printer to print out the image in hard copy. It would be far better to remove the PC, and to be able to attach the digital camera directly to a printer to print out the photograph.

USB OTG supports point-to-point connectivity, which means that a single connection can be made between two devices. In order to determine which of the two devices will take the role of host or device, host negotiation must take place. OTG also allows the peripherals to switch roles without changing the cabling. It must be noted that a USB OTG host acts in a limited host capacity in comparison to traditional USB host modules.

For more information on USB1.1, USB2.0, and USB OTG specifications, please refer to the USB website at: http://www.usb.org/home.

The MCF5249 ColdFire processor is the first ColdFire microprocessor intentionally designed to include low-power features such as 96 Kbytes of on-chip SRAM and a 1.8-V core power supply for portable applications. Interfacing the MCF5249 ColdFire microprocessor to a stand-alone USB OTG controller provides a solution for an increasing number of portable applications requiring USB OTG functionality.

This application note details the hardware design of a daughter card which interfaces the MCF5249 to the Philips ISP1362 USB OTG controller. An integrated solution would be more cost effective, would make EVB design simpler, and would result in smaller space requirements; however USB OTG is still in its infancy and stand-alone controllers have only recently become widely available. The low cost of the MCF5249 and the module integration make this an ideal solution until integrated USB OTG modules become available.

The reference design is based on the M5249C3 development board using a daughter card to provide the stand-alone USB OTG controller circuitry. This application note details the hardware design process, starting with an overview of the MCF5249 processor and the Philips ISP1362 USB OTG controller. It then examines the hardware design in more detail. Full schematics and schematic notes can be downloaded from the MCF5249 web page on Motorola's ColdFire website: www.motorola.com/ColdFire.

This reference design concentrates primarily on the hardware design of the daughter card. At this time, no specific software drivers are available. The functionality of the board has been tested with basic register read/write commands. USB device software stacks, which could be ported to this design, are available on the ColdFire website. USB stacks are also available from the uCLinux website.

1   Design Overview

The objective of this section is to outline the principles of the MCF5249 USB OTG reference design, to give an overview of the MCF5249 ColdFire Microprocessor and the Philips Semiconductors ISP1362 USB OTG controller, and to explain the reasons for choosing them for this design. For additional and more detailed information on the MCF5249, please refer to the MCF5249 product web page: www.motorola.com/ColdFire. For more information on the ISP1362 please refer to the data sheet that can be found at: http://www.semiconductors.philips.com/buses/usb/products/otg/isp136x/

The MCF5249 interfaces to the ISP1362 via the external bus interface. A basic block diagram of the hardware is shown below in Figure 1. The Philips ISP1362 has two USB ports. The first can be configured to operate as USB host, device, or OTG. The second port operates in USB host mode only. For the purpose of this design, port 1 can be configured to operate in USB device or OTG mode, and port 2 is configured to operate in USB host mode, giving the user the choice of using USB host, device, or OTG functionality.
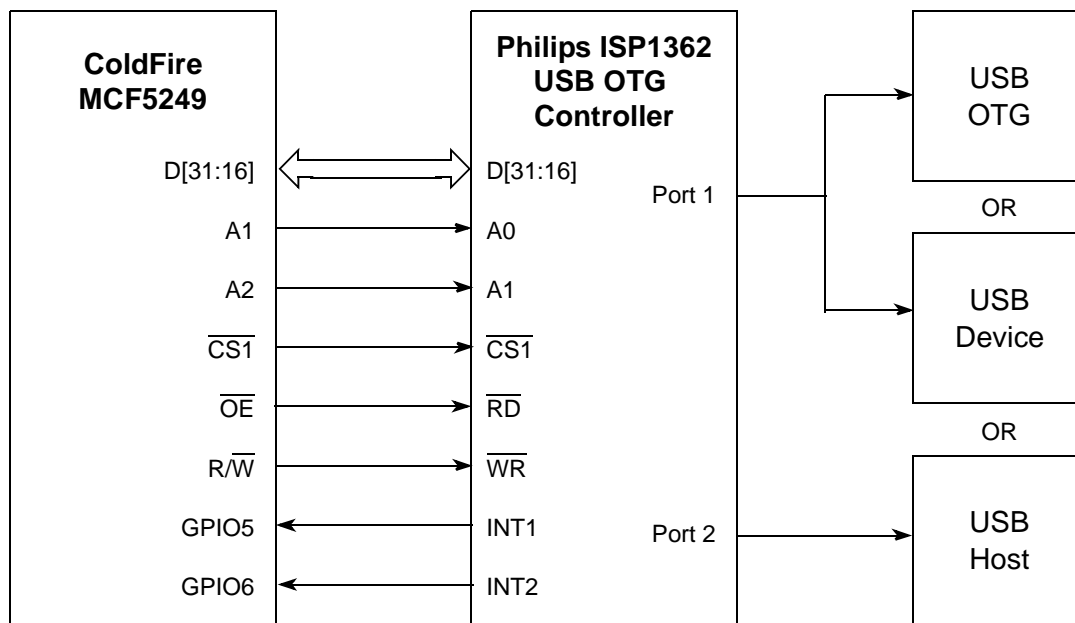

Figure 1. USB OTG Reference Design Block Diagram

1.1 MCF5249 ColdFire Microprocessor

The MCF5249 is a 32-bit embedded processor based on the V2 ColdFire core. The MCF5249 is an excellent general-purpose system controller with over 125 Dhrystone MIPS at 140 MHz performance. On-chip peripherals include an enhanced Multiply Accumulate Controller (eMAC), SmartMedia interface, 12-bit ADC, and a Flash memory card interface. In addition, the MCF5249 also features the peripheral set standard on all ColdFire microprocessors including the System Integration Module (SIM), DMA, dual UART, QSPI, I^2C^{TM}, general-purpose timers, and the real-time BDM (Background Debug Interface) interface.

Additional features that make this processor attractive to customers designing portable applications are the 1.8-V core power supply which provides low-current consumption ideal for battery operated devices and 96 Kbyte on-chip SRAM. The on-chip SRAM features power management such that power dissipation can be decreased depending on how the user utilizes the memory space.

The MCF5249 also features serial audio peripherals (I^2S^{TM}) designed for portable MP3 CD players. As the MCF5249 was designed for portable applications, it is the ideal processor to interface to the USB OTG standard.

Finally, most USB controllers available today have a 16-bit data bus. The MCF5249 and the Philips ISP1362 both have a 16-bit external bus making the interface between the two slightly less complicated.

1.2 Philips ISP1362 USB OTG Controller

The ISP1362 is a single-chip USB OTG controller compliant with the *On-The-Go Supplement to the USB 2.0 Specification Rev 1.0.* The host and device controllers are compliant with *Universal Serial Bus Specification Rev 2.0,* supporting data transfer rates of both full speed (12 Mbps) and low speed (1.5 Mbps).

As mentioned above, the ISP1362 has two ports. For the purpose of this design, port 1 is hardware configured to operate in either device or OTG mode. Port 2 is hardware configured to operate in host mode. The OTG port can switch roles from host to device or from device to host through the host negotiation protocol (HNP) as specified in the OTG supplement.

The ISP1362 features a software-controlled connection to the USB bus called SoftConnect which is used when port 1 is operating in device mode. SoftConnect replaces the requirement for an external 1.5-K pull-up resistor connected to the D+ signal to indicate a physical connection to the USB bus. Alternatively, an external pull-up can be used, but for this design SoftConnect is enabled.

The ISP1362 has internal 15-K pull-down resistors for the host controller eliminating the need to add these externally. It also has internal 15-K pull-down and 1.5-K pull-up resistors on the OTG D+ and D– signals, eliminating the need to add these externally. In this design, all internal resistors should be enabled.

The ISP1362 also features a good USB connection indicator, called GoodLink, that blinks with USB traffic. This is also implemented on the daughter card design.

The USB host supports all four types of data transfer: control, bulk, interrupt, and isochronous.

The USB device supports 2 control endpoints and up to 14 configurable endpoints, which can be programmed to any of the 4 transfer types.

2 Hardware Design

The MCF5249 USB OTG reference design is developed around the M5249C3 evaluation board using a daughter card for the USB OTG controller. The daughter card connects to the evaluation board using expansion connectors already provided on the M5249C3 board.

The M5249C3 board provides an RS232 interface, BDM interface, 8 Mbyte SDRAM, and 2 Mbyte Flash ROM for system development. For additional information on the evaluation board, including full schematics, refer to the M5249C3 user's manual on the MCF5249 web page.

The main features and key issues (interface, clocking, over-current protection, etc.) are explained in the subsections below.

2.1 MCF5249 External Bus Interface

The ISP1362 is interfaced to the MCF5249 via the external bus interface. The external bus interface pins are utilized as follows:

- A0 determines whether the controller is to be in the command or data phase.
- A1 determines, on a per-access basis, whether the controller is to operate in host or device mode:
    - 0 Host control (HC) is selected
    - 1 Device control (DC) is selected
- $\overline{CS1}$ enables the HC/DC driver to access the buffer memory and registers of the HC/DC.
- $\overline{RD}$, when asserted low, indicates that the HC/DC driver is requesting a read to the buffer memory and registers of the HC/DC.
- $\overline{WR}$, when asserted low, indicates that the HC/DC driver is requesting a write to the buffer memory and registers of the HC/DC.
- D[31:16] connects the external 16-bit data bus to the internal registers and buffer memory of the ISP1362.

The USB controller supports programmed I/O (PIO) and Direct Memory Access (DMA); however, in this design only PIO has been implemented.

PIO mode allows the MCF5249 to access the internal control registers and buffer memory of the ISP1362. It occupies only four memory locations of the MCF5249. For recommended ISP1362 memory allocation, refer to the ISP12362 data sheet: http://www.semiconductors.philips.com/buses/usb/products/otg/isp136x/

2.2 Clocking

The ISP1362 runs with a 12 MHz crystal with an on-chip PLL. The MCF5249 runs at 140 MHz with an external bus speed of 70 MHz.

Please refer to the timing diagrams in the MCF5249 user manual and the ISP1362 data sheet.

The ISP1362 operates asynchronously. All data transmission is clocked on $\overline{CS1}$ and/or $\overline{OE}$ and R/$\overline{W}$.

Minimum times for read and write cycles in the ISP1362 are given as 25 ns and 22 ns respectively. In order to maintain these timings, it is advised to add at least 1 wait state to $\overline{CS1}$ on the MCF5249.

2.3   USB Connectors

Standard series "A" (host) and series "B" (device) receptacles are present for host or device operation. Host and device operation are fixed depending on the connector; no additional signals are required.

As USB OTG is intended for use in portable devices, the Mini-AB connector defines a dual-role device (acts as host or device) and is physically smaller than the traditional series "A" and series "B" connectors. A Mini-AB receptacle is attached to Port 1 for OTG operation.

The Mini-AB connector has an additional pin called the ID pin. The OTG default role of the ISP1362 is controlled by the ID pin, which in turn is controlled by the type of plug connected into the Mini-AB receptacle. If ID = LOW (mini-A plug connected), it becomes a host by default. If ID = HIGH (Mini-B plug connected), it becomes a device by default.

The ID signal can be polled by the MCF5249 to check if it is being pulled high or low.

Please refer to the schematic summary note, Section 8, for more details on USB signals and connectors and how they are used in this design.

2.4   USB Current Requirements

The USB bus distributes 500 mA of power through each host port. Thus, low-power devices that might normally require a separate AC adapter can be powered through the USB cable. However, a USB-OTG enabled device must also be able to source power on Vbus as well, which is not practical for many battery-powered devices, so the OTG supplement allows dual-role devices to supply as little as 8 mA to meet the needs of the peripherals.

When operating in host mode, an over-current protection circuit is required on Vbus. This is implemented on the daughter card with a Micrel dual-channel power distribution switch.

This is not required when operating in OTG or device mode, therefore Vbus is connected directly. OTG and device mode also have to be Vbus sensing in order to detect when another USB device requests the start of a session.

2.5   Interrupts

int[1:2] are connected to gpio[5:6] on the MCF5249. Pins GPIO5 and 6 on the MCF5249 have the primary function of int[5:6].

2.6   Reset

The USB controller will be reset when the processor is reset with the $\overline{\text{RESET}}$ signal from the M5249C3 board. The reset time required for the ISP1362 is 10 ms. The reset signal from U9 (MAX6355LSUT-T) on the M5249C3 is held active for 100 ms, which is well within the 10 ms requirement for the daughter card.

2.7   Suspend/Wake-up

There are two wake-up pins, one dedicated to the device controller and one for the host controller (D_SUSPD/$\overline{\text{WUP}}$ and H_SUSPD/$\overline{\text{WUP}}$). This means that the controller can be placed in the suspend mode when not in use and activated when required, thus saving power.

2.8   Power

The M5249C3 board provides a 3.3-V and 5-V supply.

3   Mode of Operation

The daughter card can be configured to operate in three modes: host, device, and OTG.

3.1   Configuration for Host Mode

To configure for host mode, place USB series "A" plug into series "A" receptacle.

3.2   Configuration for Device Mode

To configure for device mode, follow the steps below.

1.   Place USB series "B" plug into series "B" receptacle.
2.   Set jumper HOSTENB1 between pins 1 and 2.
3.   Remove jumper OTGENB1.

3.3   Configuration for OTG Mode

To configure for OTG mode, follow the steps below.

1.   Place Mini-A or Mini-B plug into Mini-AB receptacle
2.   Set jumper HOSTENB1 between pins 1 and 2.
3.   Set jumper OTGENB1 between pins 1 and 2.

3.4   Configuration for Port 1 Host Mode

If host mode is required on port 1, an additional series "A" receptacle is required on the board connected to OTG_DP1 and OTG_DM1.

•   Set jumper HOSTENB1 between pins 2 and 3.

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