Application Note

AN2638

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Effects of Clock Jitter on the MPC8260 (HiP3 and HiP4)

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Clock jitter can cause unwanted effects on high-speed system design. In general it is important for the system designer to ensure proper board (PCB) layout for power and ground planes, as well as the signal layer.

This document describes the possible causes and effects of clock jitter on the operation of the MPC8260 PowerQUICC II™ (HiP3 and HiP4) family of devices (refer to Table 1 for a complete list). More importantly, this document discusses various types of clock jitter, how to measure clock jitter, and recommendations for reducing its effects.

Table 1. MPC8260 PowerQUICC II Family of Devices (HiP3 and HiP4)

Device	Silicon							
	Process	0.29µm (HiP3)					0.25µm (HiP4)		
	Revision	A.1	B.1	B.2	B.3	C.2	A.0	B.1	C.0
MPC8260(A) [1]		√	√	√	√	√	√	√	
MPC8250 [2]							√	√[2]	√[2]
MPC8255(A)[1]		√	√	√	√	√	√	√	
MPC8264							√	√	
MPC8265							√	√	√
MPC8266							√	√	√

1 "A" designates HiP4 revisions of a device that was originally available in a HiP3 version.
2 Also available in 516 PBGA (VR or ZQ) package in HiP4 Rev B.1 and Rev C.0 only.

Users are encouraged to consult following reference documentation for additional information about timing specification and design considerations.

Table 2. References

Document Category	Document Title	Document ID
Hardware Specifications	*MPC8260 (HiP3) Hardware Specifications*	MPC8260EC/D
	MPC826xA (HiP4) Family Hardware Specifications	MPC8260AEC/D
Reference Manual	*MPC8260 PowerQUICC II™ Family Reference Manual*	MPC8260UM/D
Application Notes	*MPC8260 PowerQUICC II™ Design Checklist*	AN2290/D

1 Clock Jitter

Clock jitter is defined as when the clock's output varies—either leads or lags—from its ideal position. Clock jitter can be classified as one of the three following categories:

- Cycle to cycle jitter
- Time interval jitter
- Period jitter

1.1 Cycle to Cycle Jitter

In an ideal case all clock waveforms should have equal periods. i.e. $t_{x} = t_{y} = t_{z}$ .....

However, a cycle to cycle jitter is the difference between every two consecutive periods of a periodic waveform. Figure 1 represents the following relationships:

$T_{j1} = t_{x} - t_{y}$
$T_{j2} = t_{y} - t_{z}$
Total jitter = $T_{j1} + T_{j2}$

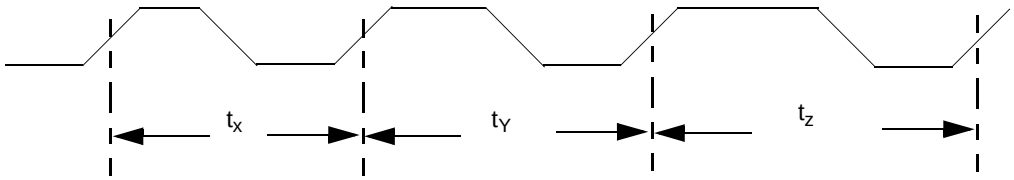

Figure 1. Cycle to Cycle Jitter

1.2 Time Interval Jitter

Time interval jitter can be differentiated between long term and short term clock jitter. The long-term jitter measurement is the maximum change in the clock output transition from ideal clock position over many clock cycles.Figure 2 represents the long term clock jitter measurement.

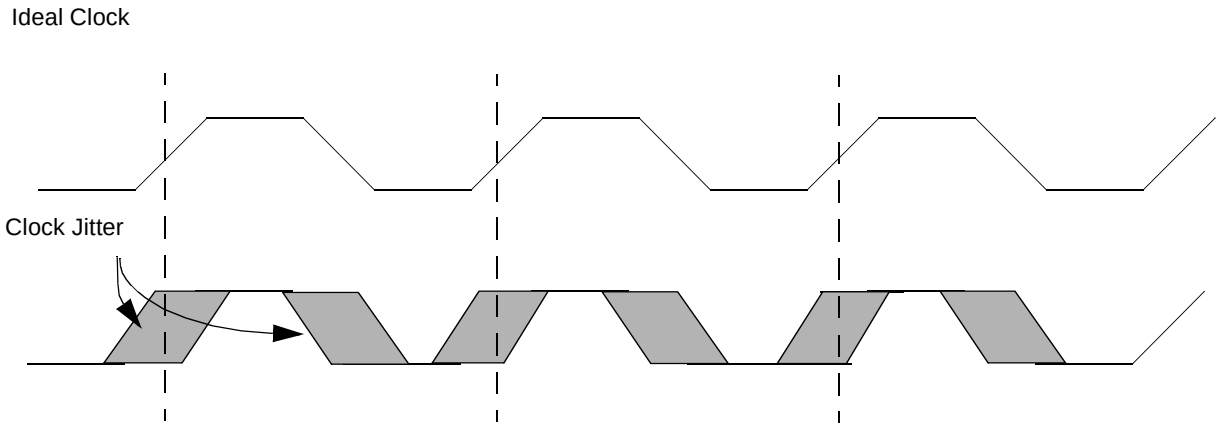

Figure 2. Time Interval Jitter

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1.3 Period Jitter

Frequency (period) jitter is the frequency deviation of the waveform from the average frequency. Period jitter is a critical measurement for system timing margins. It is important to take period jitter measurements into account when designing a high-speed system. Figure 3 shows an example of period jitter.

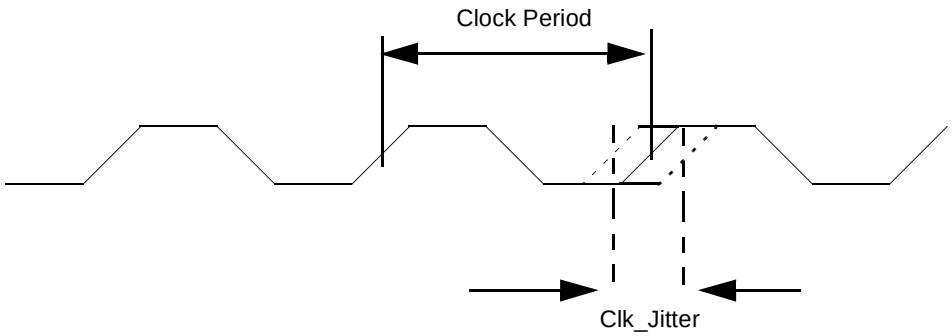

Figure 3. Period Jitter

2 Possible Cause of PLL Jitter

External noise induced by a printed circuit board (PCB) can contribute to PLL noise. The effect of external (board level) noise on PLL performance can be minimized by careful PCB layout, adequate filtering of the PLL supplies, and insuring a clean input clock.

The power distribution on the PCB should guarantee voltage supply within the specification during operation. The PCB layout should be such to minimize the noise coupling between the main supply and the PLL supply. The noise level on the PLL supply (VCCSYN) affects the noise level of the PLL VCO.

Clock jitter can cause a number of undesired effects on the system, such as data corruption in the system memory (SDRAM) due to AC timing violation.

Figure 4 shows the comparison of “SDRAM Clock” and “Internal Clock” on a typical data output signal. The data is valid on the rising edge of the clock signal. However, because of clock jitter the rising edge of the clock has occurred prior to the data becoming valid. In this case data corruption can occur.

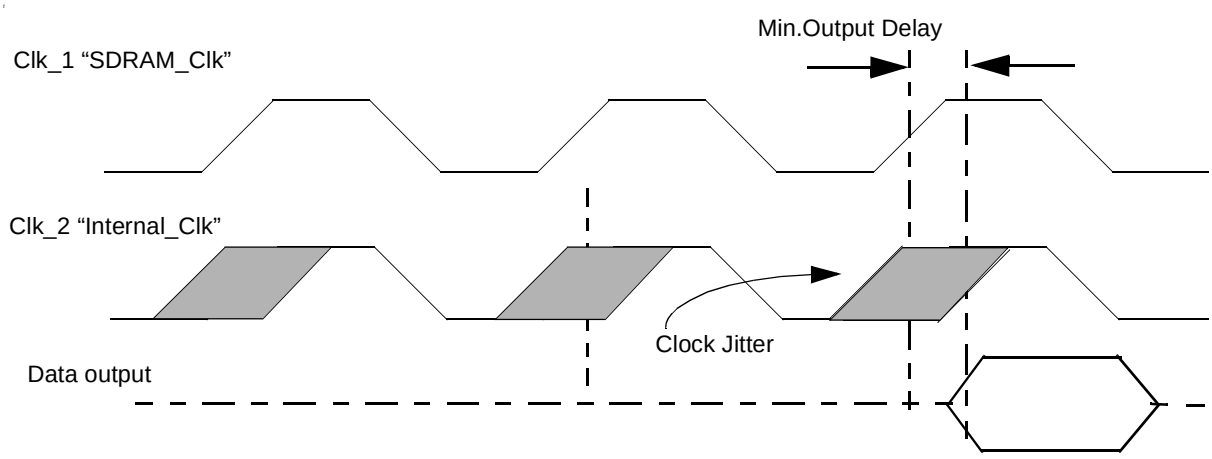

Figure 4. Comparison of SDRAM Clock Signal with Internal Clock on typical Data Output cycle

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3 Phase Lock Loop (PLL)

A phase lock loop, shown in Figure 5, is a feedback system that operates on the excess phase of nominally periodic signals. The range in which the Voltage Controlled Oscillator (VCO) can lock onto a new signal is sometimes referred to as the PLL locking range. Once the PLL is locked, it is said to be tracking a signal. In the PLL locked condition, the input and output PLL signals have equal frequencies with minimum phase difference and the phase detector generates pulses whose widths are equal to the time difference between the zero crossing of the input and output.

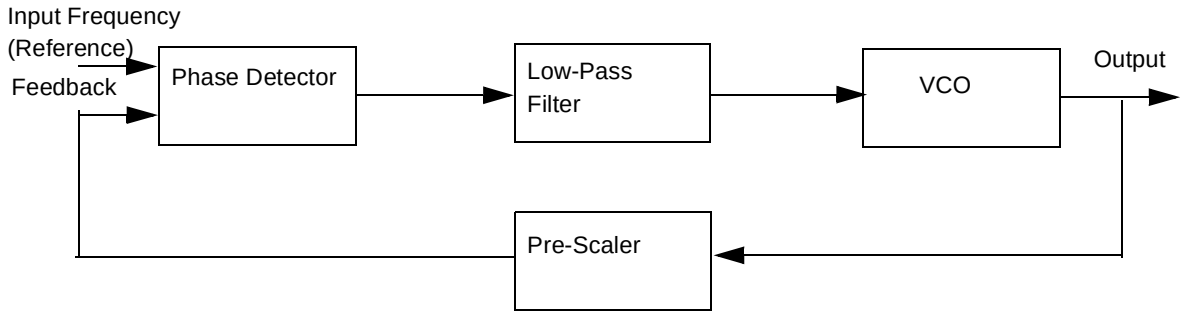

Figure 5. Phase Lock Loop Block

Because the PLL operates on the phase of signals, it is susceptible to phase noise or jitter. Phase noise at either the input signal or the VCO can influence PLL operation.

- Phase noise of the VCO—The PLL loop bandwidth should be maximized to reduce VCO phase noise and lock time. The VCO's immunity to noise that comes through the power supply or the ground is determined mainly by internal PLL power supply noise filtering capability. Noise at the frequency around the PLL bandwidth is a main cause of the phase jitter. High frequency power supply noise mainly affects period jitter and cycle-to-cycle jitter, while low frequency power supply noise is mainly filtered by the loop filter.
- Phase noise at input signal—The PLL loop bandwidth should be minimized to filter the input signal phase noise.

The loop filter dynamic behavior is controlled by the value of LPF capacitor. When the Multiplication Factor (MF) increases, the LPF capacitor must be larger (as explained in Table 10-1 in the *MPC8260 PowerQUICC II™ Family Reference Manual*) and the PLL bandwidth is decreased. Thus, assuming a stable input clock, the use of a smaller MF and a higher reference clock frequency to maintain a design's PLL frequency minimizes the PLL jitter.

Therefore, the following items may reduce jitter:

- A clean reference clock. It is recommended that designs provide a power supply that is clean from noise at a PLL bandwidth of 200kHz – 2MHz (or even wider for better PLL performance).
- A higher reference clock frequency
- A smaller MF
- Well filtered PLL power supply

3.1 PLL Transfer Function

In theory the PLL loop filter equivalent circuit can be shown as Figure 4 in which the internal filter capacitor C_{int} is parallel to C_{xfc} both capacitors are in series to internal filter R_{int}.

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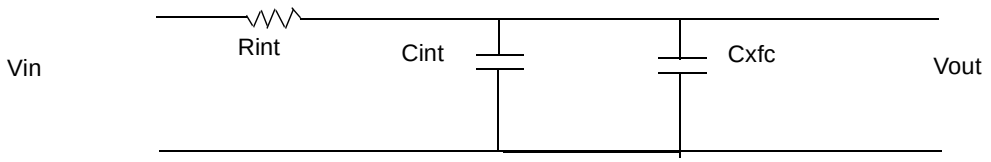

Figure 6. PLL Loop Filter

Table 3provides a brief description for each transfer function elements.

Table 3. PLL Transfer Function Elements

Transfer Function	Remark
ζ	Damping function
ϖ_n	Loop bandwidth
$H_{(s)}$	Feedback Transfer function
LPF	Low Pass Filter
G_n	Forward transfer function
K	Loop Gain
s	Input frequency

The PLL low pass filter of the first order has the following transfer function:

$$G_{LPF} = \frac{1}{\frac{s}{\varpi_{LPF}} + 1}$$

Therefore, the PLL closed loop transfer function is as follows:

$$H(s) = \frac{\varpi_n^2}{s^2 + 2\zeta\varpi_n s + \varpi_n^2}$$

The damping factor and loop bandwidth defined as:

$$\zeta = \frac{1}{2}\sqrt{\frac{\varpi_{LPF}}{K}} \quad \text{and} \quad \varpi_n = \sqrt{\varpi_{LPF} K}$$

The loop gain (K) and loop bandwidth (ω) cannot be independently selected because a change in one of the parameters will have an adverse effect on the other parameter. Therefore, to allow independent change in (K) and (ω), a component of R_{xfc} is added to the PLL low pass filter.

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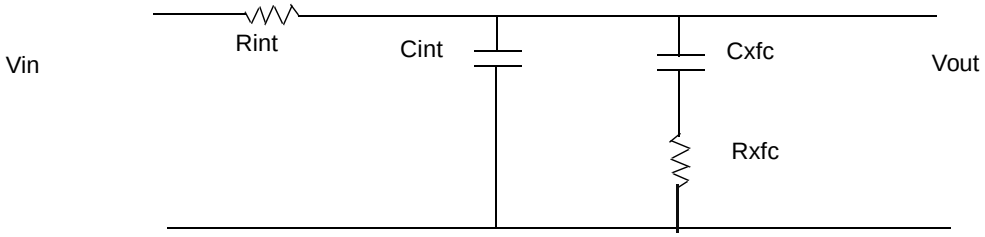

Figure 7. PLL loop filter with R_{xfc}

The addition of R_{xfc}, modifies the transfer function as follows:

$$G_{LPF} = \frac{R_{XFC}C_{XFC}s + 1}{(R_{int} + R_{XFC})C_{XFC}s + 1}$$

3.2 Frequency Response

Figure 8 shows a frequency response compression graph of filter configuration. This compression shows that the combination of C_{xfc} + R_{xfc} demonstrated the best case scenario for wider frequency response area, thus allowing the PLL operation less susceptible to jitter.

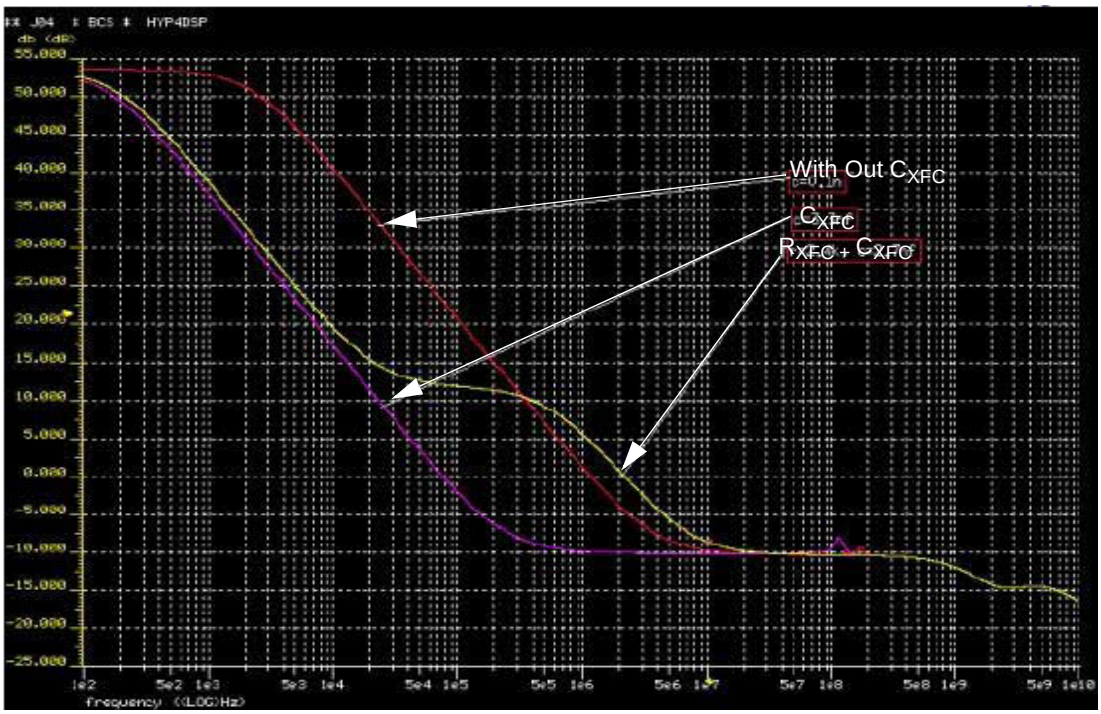

Figure 8. Frequency Response Comparison

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3.3 XFC Filter

The XFC (external filter capacitor), shown in Figure 9, is critical to the operation of the main internal PLL circuits. The value of this capacitor determines the stability of the PLL and its ability to lock quickly onto the input signal edge and remain locked. The XFC provides control voltage for the system PLL VCO. There are current sources within the PLL that charges the XFC. Lower capacitance responds more quickly to the charge current; thus the PLL reacts faster but it may have overshoots/undershoots. To calculate the XFC value, use the formula provided in Chapter 10, "Clocks," in the *MPC8260 PowerQUICC II™ Family Reference Manual.*

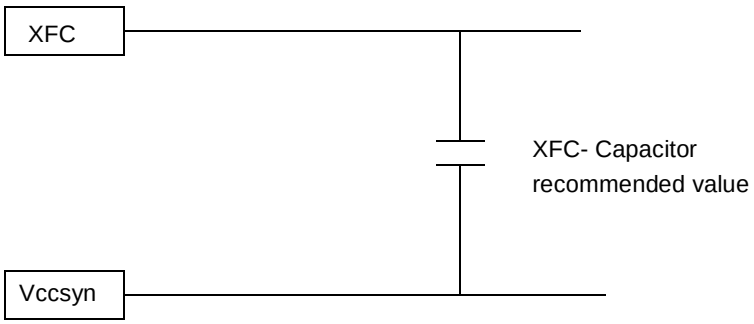

Figure 9. XFC Filter Circuit

3.4 PLL Supply Filtering

On the MPC8260, VCCSYN/VCCSYN1 provide power to the PLL circuitry. To ensure stability of the PLL and minimize noise level, these PLL power supply pins should be filtered with capacitors with low and high frequency characteristics. Figure 10 shows an example of PLL supply filter circuit. Note that capacitors should have low effective series inductance (ESL). It is recommended that each PLL supply have a dedicated filter. For more information, refer to *MPC8260 PowerQUICC II™ Design Checklist* (AN2290/D).

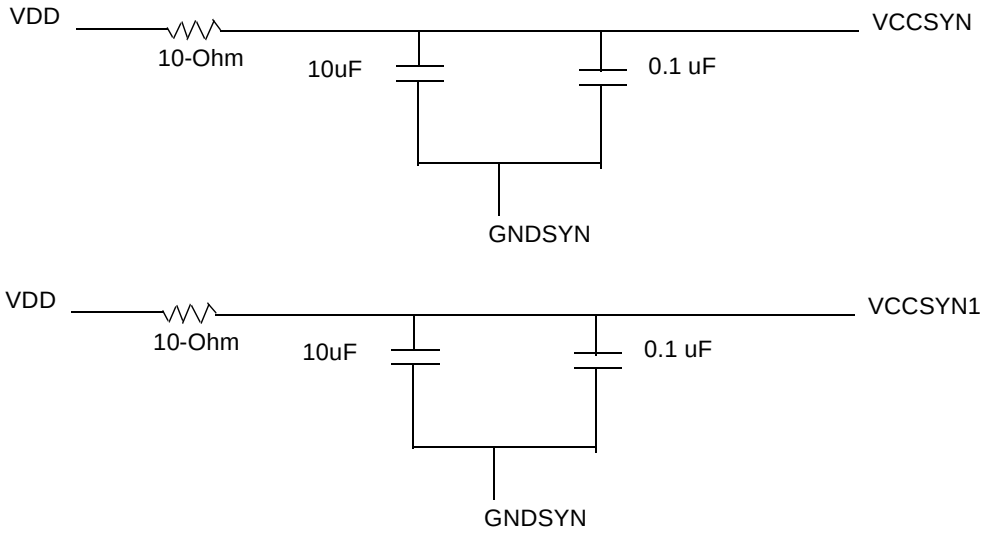

Figure 10. PLL Supply Filter

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4 How to Minimize Clock Jitter

The following are possible ways to reduce clock jitter and avoid AC timing violations.

4.1 Power Supply

A main factor that can contribute to clock jitter is the presence of significant voltage drops in a design's power supply. Therefore, it is important to ensure that both the device's power and ground input pins have proper routing on the printed circuit board and to maintain a stable device voltage at all times. A poorly designed power source or board layouts may contribute to clock jitter during increased I/O activity and CPU activity on device.

VDDL voltage should not drop below the minimum recommended operating condition as specified in the appropriate hardware specification document (refer to Table 2).

4.2 XFC RC Filter

On systems where excessive PLL jitter causes AC timing violations, a 2.4Kohm resister (R_{XFC}) can be added in series with the specified (C_{XFC}) capacitor. As discussed in Section 3.1, "PLL Transfer Function," this resister/capacitor (RC) filter acts as a noise rejection circuit, thus allowing for fast clock recovery for a wider frequency bandwidth and less susceptibility to phase noise or jitter. For the best result, the XFC capacitor should be placed as close as possible to the XFC pin on the MPC8260. The 2.4Kohm R_{XFC} value stays constant for all multiplication factors. For selecting C_{XFC} capacitor values, refer to *MPC8260 PowerQUICC II Family Reference Manual*. Figure 11 shows the physical connection of the XFC RC filter circuit.

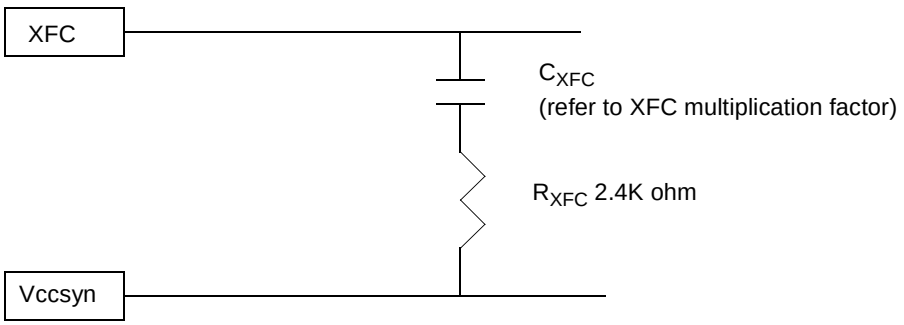

Figure 11. External PLL filter

5 Jitter Measurement

Before proceeding to jitter measurement, the user must verify that the system power supply can provide clean power to the input pins on the MPC8260. It is critical that the measuring method is accurate and repeatable. The following steps will help to ensure that repeatable timing measurements are obtained:

1. For clock jitter measurement we used Agilent Infinium Scope (2 channels @ 2 GSamples / sec.) with an Agilent 1160 passive probe. The probe used had a bandwidth of 500Mhz (scope + probe) and a compensation range of (6 - 9) pF. Other manufactures also have equipment available for these measurements.
2. For best measurements connect the probe tips as close as possible to the SDRAM CLOCK_IN pin and CAS signals.

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3. Ensure probe ground pins are close to the signal pins
4. In terms of the scope setting, we used infinite persistence option to capture minimum/maximum of the clock variation (jitter).
5. The measurement should be taken while the Device Under Test (DUT) is running the application software at peak rate.
6. The signal measurements should be taken at the mid level crossing point between SDRAM CLOCK_IN and CAS signal.

6 Clock Jitter Effects on AC Timing

On systems where PLL experiences excessive jitter beyond the allowed AC requirement of the system, the timing specification 30 (sp30) hold time will be in violation. As stated in the hardware specifications document, sp30 is the minimum hold time for output signals. It is 0.5ns and is referenced to the internal clock signal. Some of the symptoms that can occur when sp30 does not meet the specifications are corruption on the address and data buses. In the following sections we will discuss sp30 measurement of an ideal case with minimum jitter and a worse case scenario of clock jitter.

6.1 Ideal Case (Minimum Jitter)

Figure 12 shows a scope capture that illustrates sp30 measurement that meets the specification of 0.5 ns. Probe 1 was connected to SDRAM CLOCK_IN and probe 2 was connected to the CAS signal on the MPC8260. This measurement is taken in “infinite persistence” mode to capture the clock jitter.

Figure 12. sp30 Timing and Clock Jitter Specification

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6.2 Worse case (Excessive Jitter)

In comparison, Figure 13 illustrates the scope capture of worse-case clock jitter. Probe 1 was connected to SDRAM CLOCK_IN and probe 2 was connected to the CAS signal on theMPC8260. The measurement is taken in “infinite persistence” mode to capture the minimum-to-maximum clock period variation.

Figure 13. Worse Case Clock Jitter

7 Conclusion

The following list summarizes the key points for preventing clock jitter when designing a high-speed design system:

1. Ensure proper board layout for power and ground planes as well as at the signal layer.
2. Provide a stable power supply voltage source for the MPC8260.
3. Provide a proper filtering for PLL power supply input pins.
4. Provide reference clock clear from frequency noise allowed within the AC requirements of the system.
5. Use recommended XFC capacitor value (refer to Chapter 10, Clocks,” in the *MPC8260 PowerQUICC II Family Reference Manual.*
6. Place the XFC capacitor as close as possible to the XFC pin on the MPC8260.
7. On systems where clock jitter is beyond the acceptable AC requirements of the system, add a series RC circuit (R_{xfc} + C_{xfc}) to the XFC pin to provide a PLL noise rejections, thus allowing quick recovery of PLL lock condition for wider frequency bandwidth. Refer to Section 4.2, “XFC RC Filter.”

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