FM IF IC

FEATURES

- **Input Frequency (~22 MHz)**
- **Low Voltage Operation (2.3 to 5.5 V)**
- **Battery Save Function**
- **Wide Band Demodulator (~1 MHz)**
- **High Speed Data Comparator (~2 Mbps)**
- **Very Small Package (TSSOP-16)**

APPLICATIONS

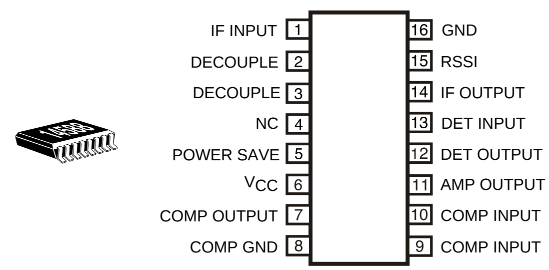
- **Communications Equipment**
- **Wireless LAN**
- **Keyless Entry Systems**

DESCRIPTION

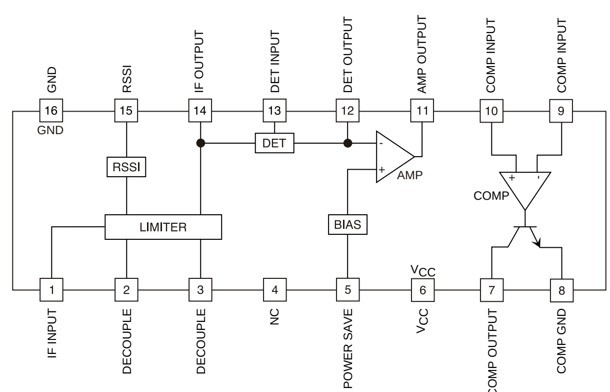
The TK14588V is a standard function general purpose IF IC capable of operating up to 22 MHz. The TK14588V contains a high-speed data comparator for base band processing. The TK14588V has a unique function that allows establishing the demodulation characteristics by changing the external RC time constant, and not changing the phase shifter constant. The RSSI output is individually trimmed, resulting in excellent accuracy, good linearity, and stable temperature characteristics. The TK14588V was developed for high-speed data communication, DECT, wireless LAN, keyless entry systems, etc.

The TK14588V is available in the very small TSSOP-16 surface mount package.

TK14588V



BLOCK DIAGRAM



ORDERING INFORMATION

TK14588V □□

Tape/Reel Code

TAPE/REEL CODE
TL: Tape Left

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... 6 V
Operating Voltage Range .... 2.3 to 5.5 V
Power Dissipation (Note 1) .... 160 mW
Storage Temperature Range .... -55 to +150 °C
Operating Temperature Range ....-30 to +85 °C
Operating Frequency Range (IF) .... 6 to 22 MHz
Operating Frequecy Range (Demodulation) ..... to 1 MHz

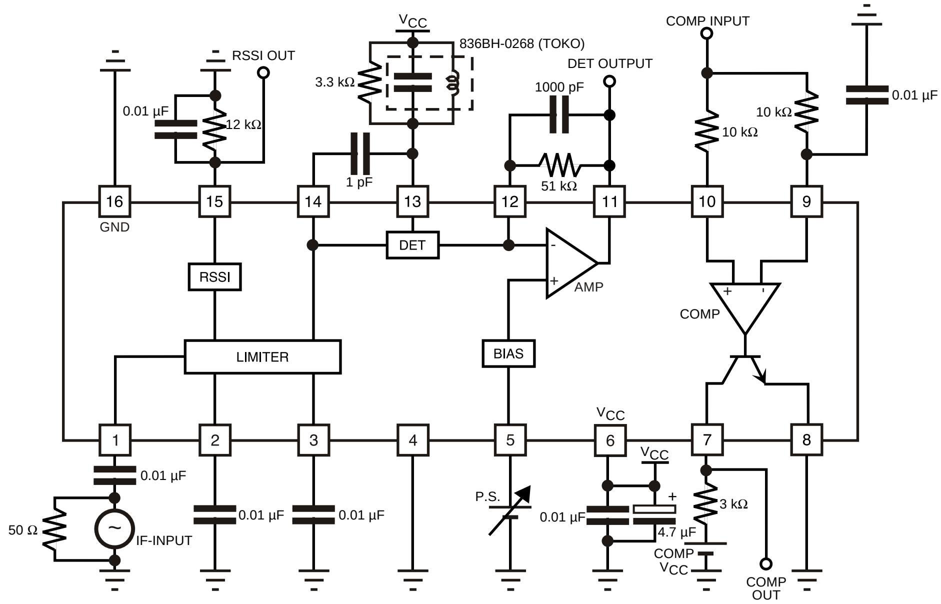
TK14588V ELECTRICAL CHARACTERISTICS

Test conditions: V_{CC} = 3 V, f_{IN} = 10.7 MHz, fm = 1 kHz, Modulation = ±50 kHz, T_A = 25 °C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Supply Current	No input		3.5	5.0	mA
		Power Save = ON, No input		0.2	5.0	µA
IF						
V_{OUT}	Output Voltage	-30 dBm input	120	200	360	mVrms
THD	Total Harmonic Distortion	-30 dBm input		0.5	2.0	%
S/N	Signal to Noise Ratio	-30 dBm input	60	70		dB
SINAD	12 dB SINAD			-89	-83	dBm
$R_{IF(IN)}$	Limiter Input Resistance		1.4	1.8	2.2	kΩ
G	Gain		69	75		dB
RSSI						
V_{RSSI}	RSSI Output Voltage	No input	0.00	0.20	0.30	V
		-60 dBm non-modulated input	0.40	0.55	0.70	V
		-30 dBm non-modulated input	1.05	1.20	1.40	V
		0 dBm non-modulated input	1.50	1.70	1.95	V
COMPARATOR						
D_R	Duty Ratio		45	50	55	%
I_{OUT}	Output Current			1		mA

Note 1: Power dissipation is 160 mW when mounted as recommended. Derate at 1.28 mW/°C for operation above 25°C.

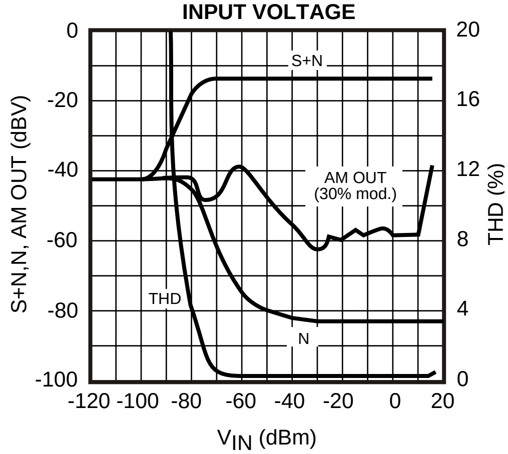
TEST CIRCUIT



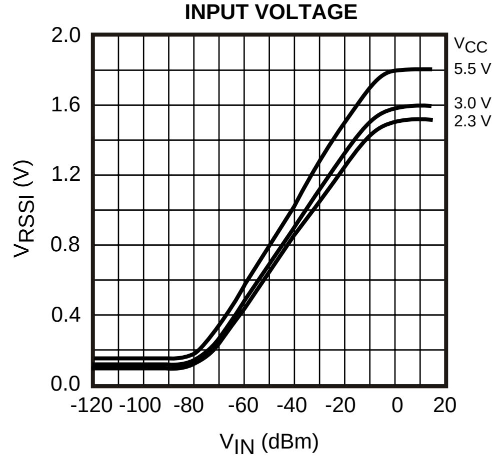
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25 °C, unless otherwise specified.

S+N, N, AM OUT, TOTAL HARMONIC DISTORTION vs. INPUT VOLTAGE



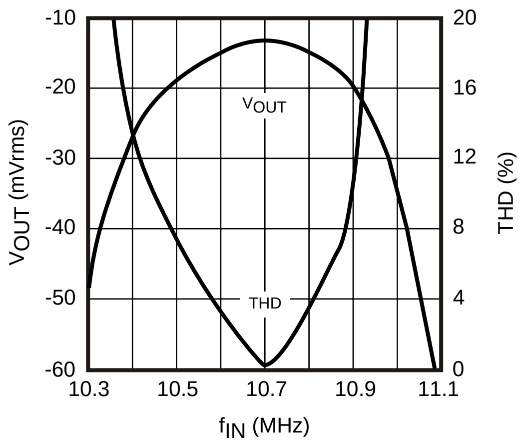
RSSI OUTPUT VOLTAGE vs. INPUT VOLTAGE



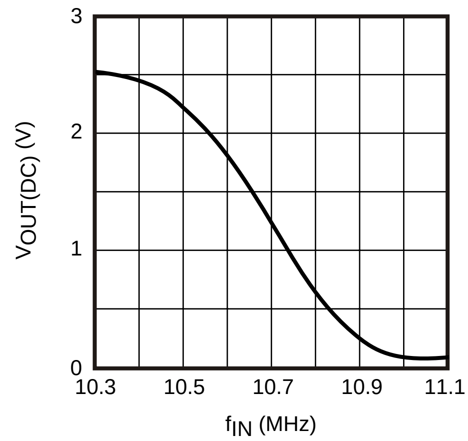
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25 °C, unless otherwise specified.

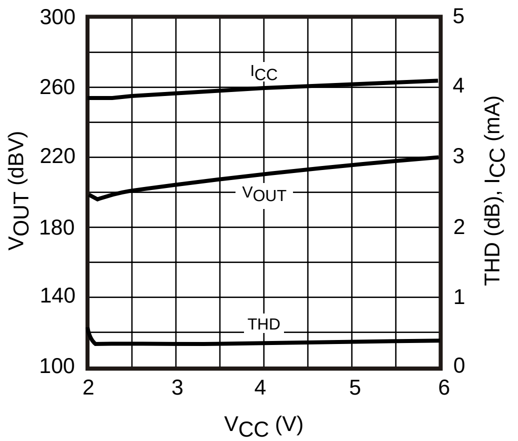
DETUNE CHARACTERISTICS



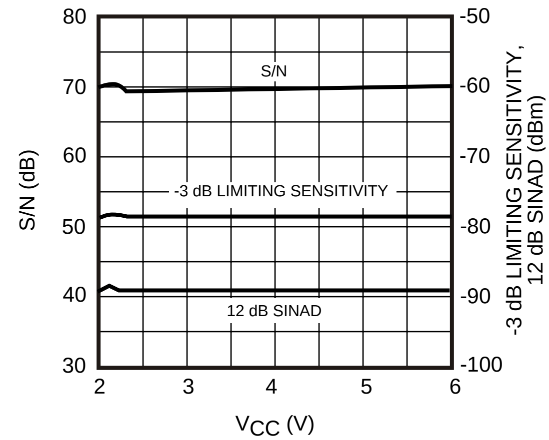
S CURVE



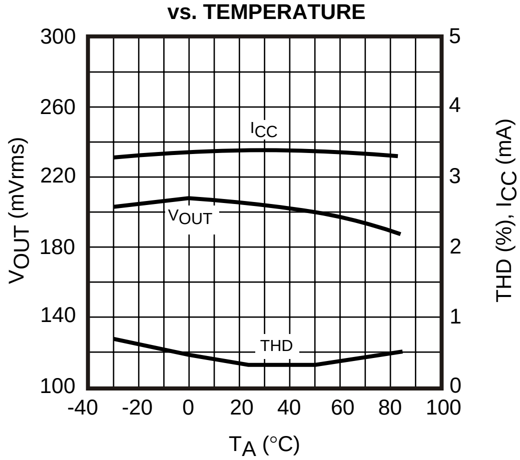
SUPPLY CURRENT, OUTPUT VOLTAGE, TOTAL HARMONIC DISTORTION vs. SUPPLY VOLTAGE



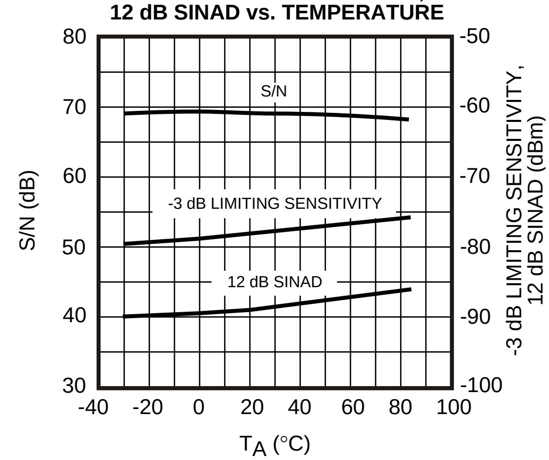
SIGNAL TO NOISE RATIO, -3 dB LIMITING SENSITIVITY, 12 dB SINAD vs. SUPPLY VOLTAGE



SUPPLY VOLTAGE, OUTPUT VOLTAGE, TOTAL HARMONIC DISTORTION vs. TEMPERATURE



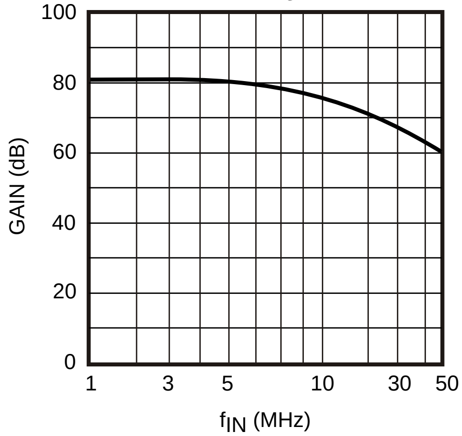
SIGNAL TO NOISE RATIO, -3 dB LIMITING SENSITIVITY, 12 dB SINAD vs. TEMPERATURE



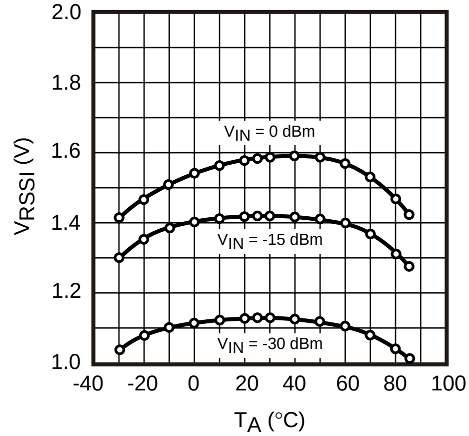
TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

T_A = 25 °C, unless otherwise specified.

LIMITER GAIN vs. INPUT FREQUENCY

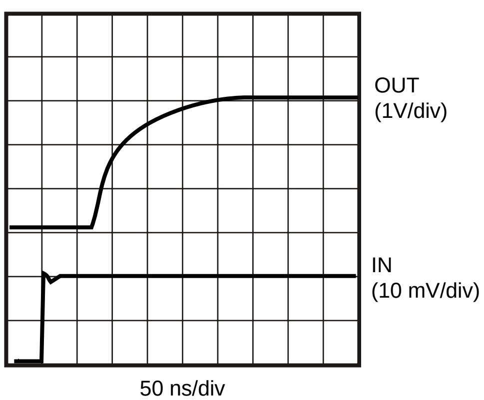


RSSI OUTPUT VOLTAGE vs. TEMPERATURE

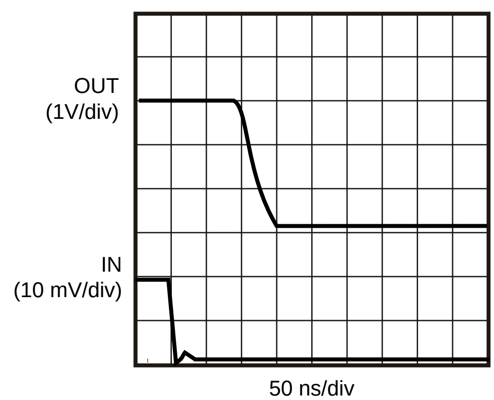


Data Comparator Output Voltage Transient Response

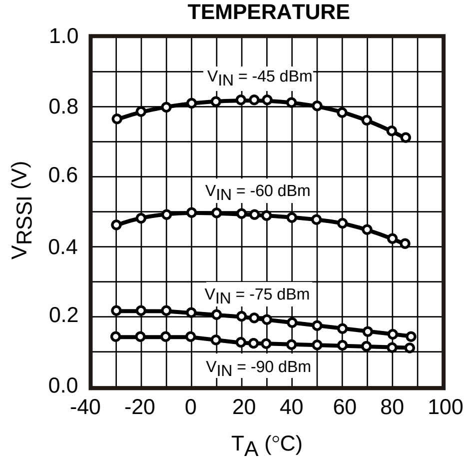
(Rise)



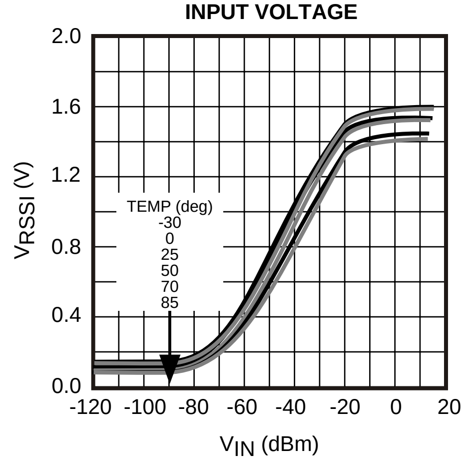
(Fall)



RSSI OUTPUT VOLTAGE vs. TEMPERATURE



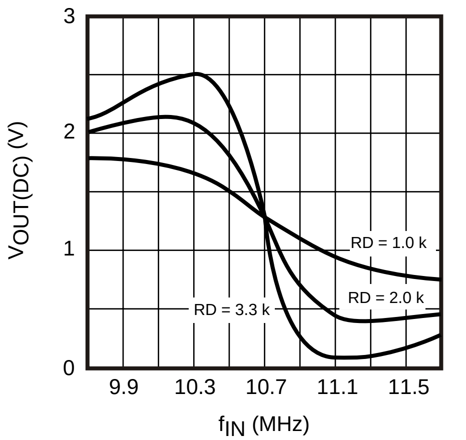
RSSI OUTPUT VOLTAGE vs. INPUT VOLTAGE

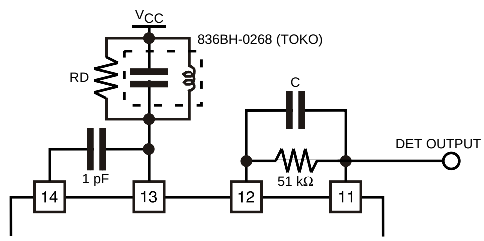


TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

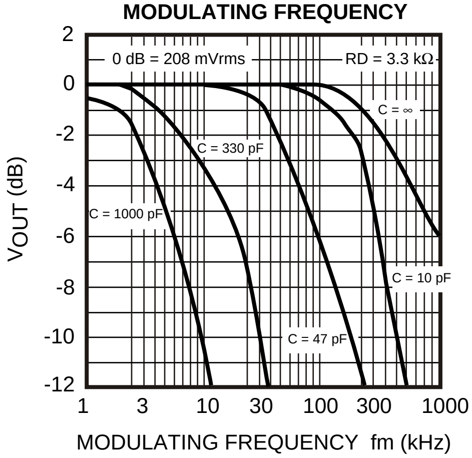
T_A = 25 °C, unless otherwise specified.

S CURVE

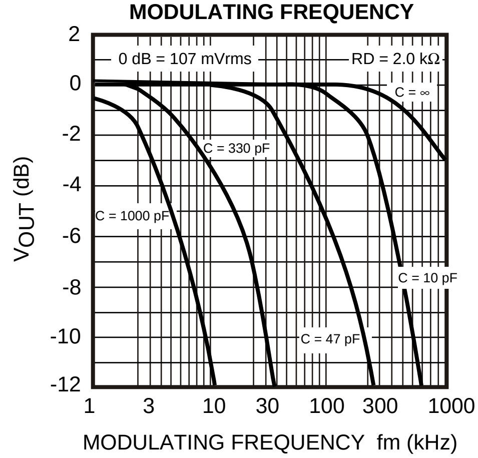




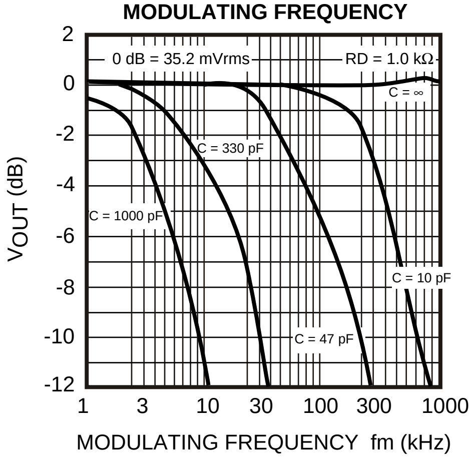
OUTPUT VOLTAGE vs. MODULATING FREQUENCY



OUTPUT VOLTAGE vs. MODULATING FREQUENCY



OUTPUT VOLTAGE vs. MODULATING FREQUENCY

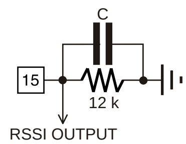


TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

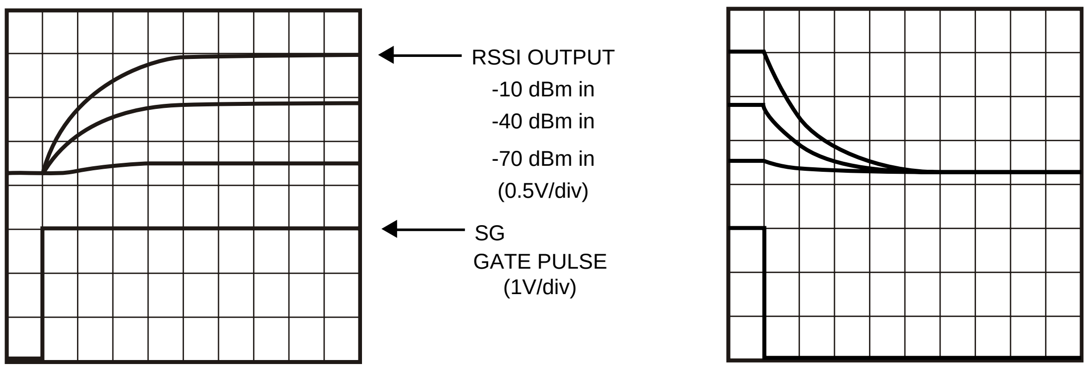
T_A = 25 °C, unless otherwise specified.

RSSI Output Voltage Transient Response (IF Input ON/OFF)

IF INPUT VOLTAGE
= -10, -40, -70 dBm

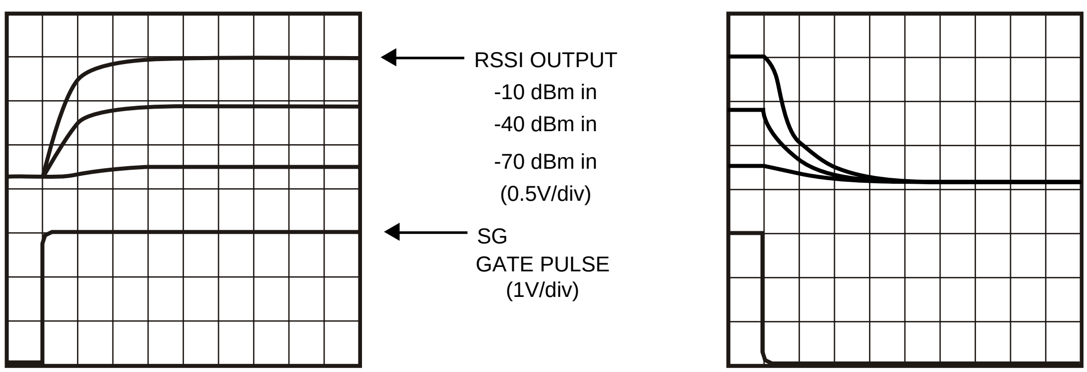


C = 0.01 µF



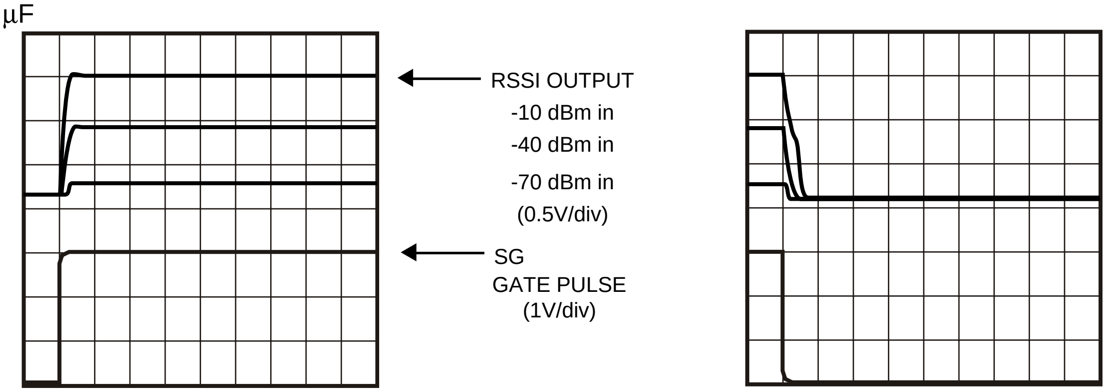
0.1 ms/div   0.1 ms/div

C = 0.001 µF



20 µs/div   20 µs/div

C = 0.0001 µF



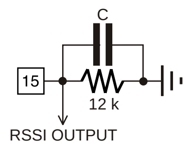
20 µs/div   20 µs/div

TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

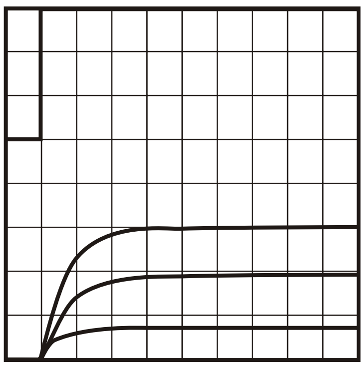
T_A = 25 °C, unless otherwise specified.

RSSI Output Voltage Transient Response (Power Save ON/OFF)

IF INPUT VOLTAGE
= -10, -40, -70 dBm



C = 0.01 µF



0.2 ms/div

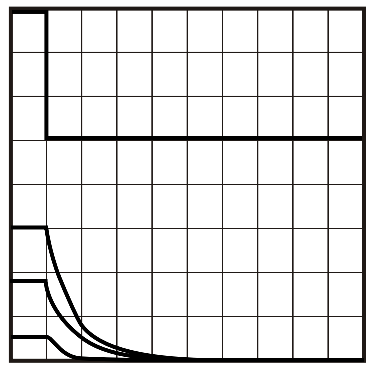
POWER SAVE
(1V/div)

RSSI OUTPUT

-10 dBm in

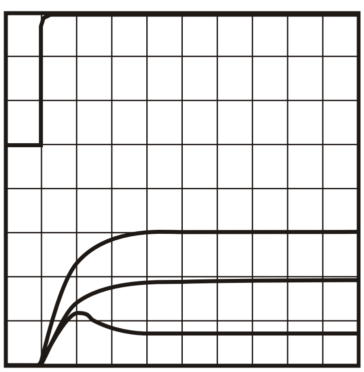
-40 dBm in

-70 dBm in
(0.5V/div)



0.2 ms/div

C = 0.001 µF



20 µs/div

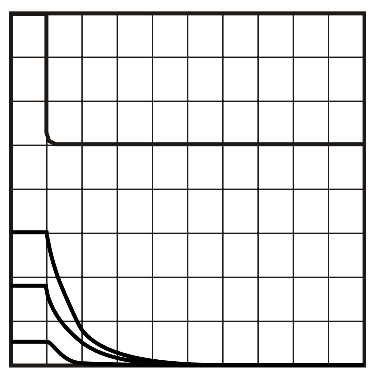
POWER SAVE
(1V/div)

RSSI OUTPUT

-10 dBm in

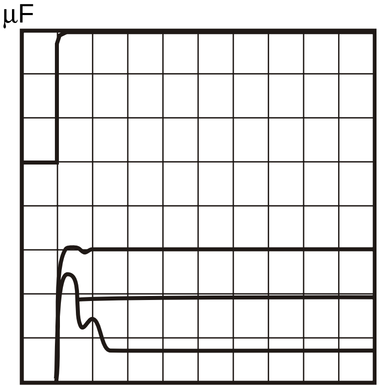
-40 dBm in

-70 dBm in
(0.5V/div)



20 µs/div

C = 0.0001 µF



20 µs/div

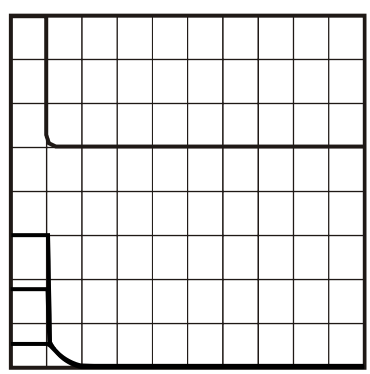
POWER SAVE
(1V/div)

RSSI OUTPUT

-10 dBm in

-40 dBm in

-70 dBm in
(0.5V/div)



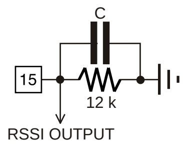
20 µs/div

TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

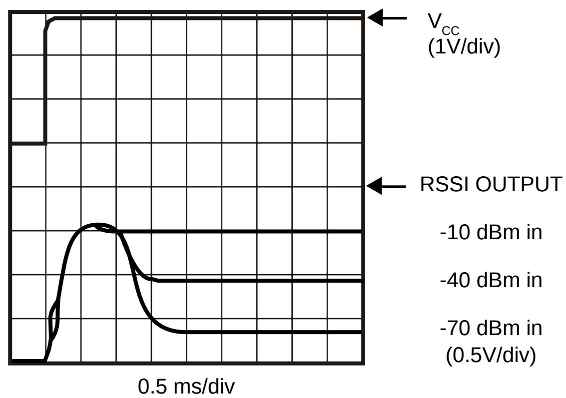
T_A = 25 °C, unless otherwise specified.

RSSI Output Voltage Transient Response (Supply Voltage ON)

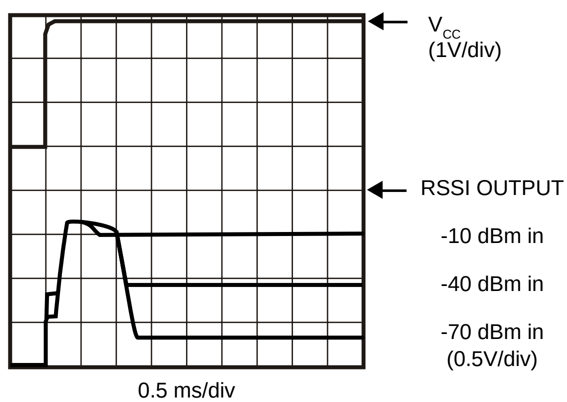
IF INPUT VOLTAGE
= -10, -40, -70 dBm



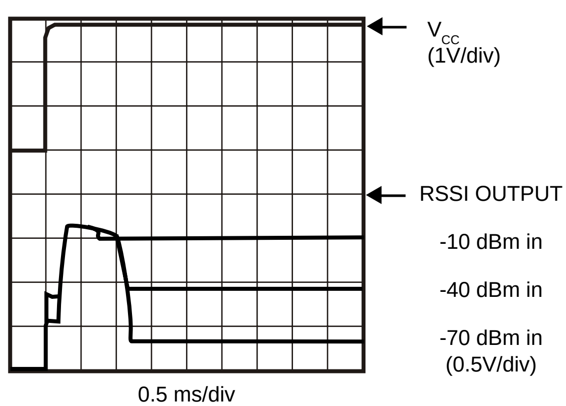
C = 0.01 µF



C = 0.001 µF



C = 0.0001 µF



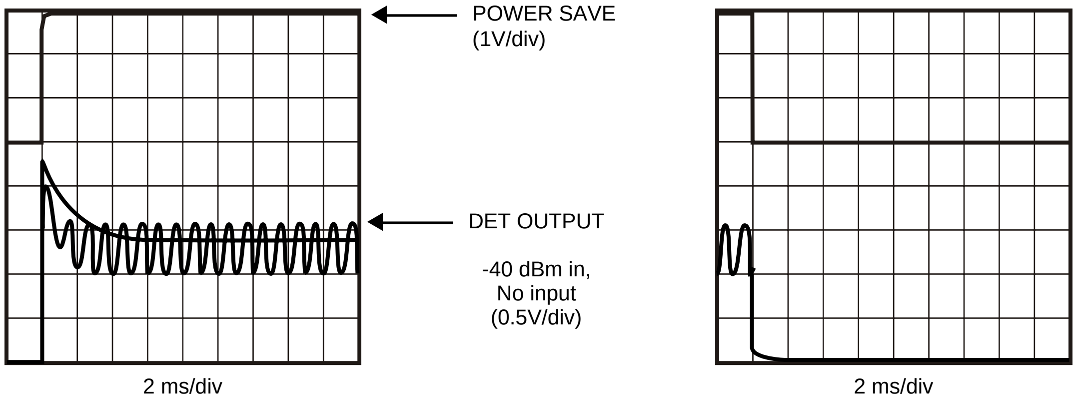
TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

T_A = 25 °C, unless otherwise specified.

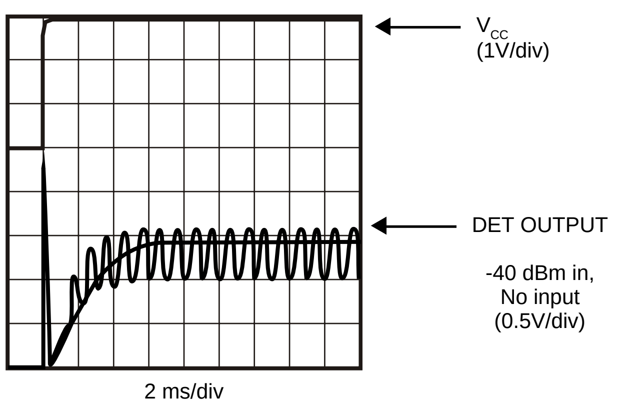
Detector Output Voltage Transient Response (Power Save ON/OFF,Supply Voltage ON)

IF INPUT VOLTAGE
= -40 dBm, No input

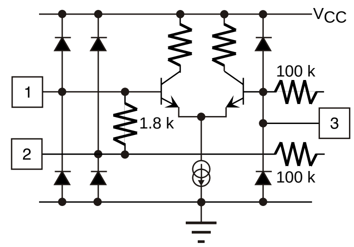
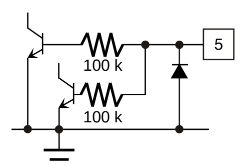
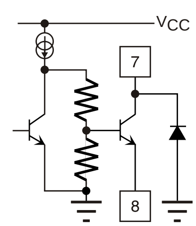
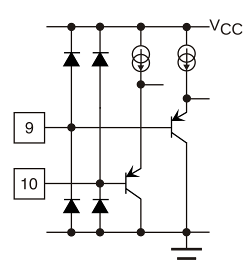
POWER SAVE ON/OFF



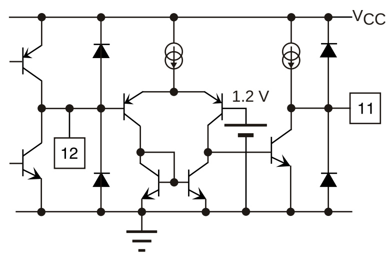
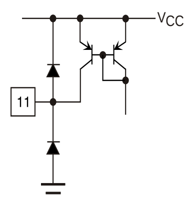
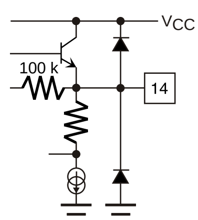
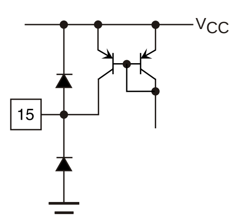
SUPPLY VOLTAGE ON



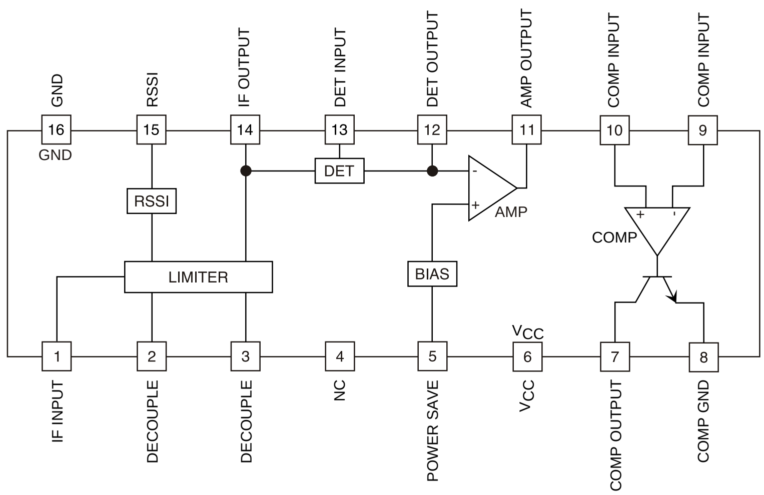
PIN FUNCTION DESCRIPTION

TERMINAL			INTERNAL EQUIVALENT CIRCUIT	DESCRIPTION
PIN NO.	**SYMBOL**	**VOLTAGE**		
1 2 3	IF INPUT DECOUPLE DECOUPLE	1.9 V 1.9 V 1.9 V		1: Limiting Amplifier INPUT 2,3: Limiting Amplifier Decoupling
4	NC			No internal connection. However, this pin must be connected to GND for noise reduction.
5	POWER SAVE	V_S		Power Save On: $V_S < 0.3$ V Power Save Off: $V_S = 1.5$ V to V_{CC}
6	V_{CC}	3.0 V		
7 8	COMP OUT COMP GND	0 V		7: Data Comparator Output 8: Data Comparator GND
9 10	COMP INPUT COMP INPUT			9,10: Data Comparator Input

PIN FUNCTION DESCRIPTION

TERMINAL			INTERNAL EQUIVALENT CIRCUIT	DESCRIPTION
PIN NO.	SYMBOL	VOLTAGE		
11 12	AMP OUTPUT DET OUTPUT	1.2 V 1.2 V		11: Amplifier Output 12: Detector Output
13	DET INPUT	3.0 V		Detector Input
14	IF OUTPUT	1.9 V		IF Limiter Output
15	RSSI			RSSI Output
16	GND	0 V		

CIRCUIT DESCRIPTION



IF Limiter Amplifier, RSSI:

The IF limiter amplifier is composed of five differential gain stages. The total gain of the IF limiter amplifier is 80 dB. The output signal of the IF limiter amplifier is provided at Pin 14 through the emitter-follower output stage. The IF limiter amplifier output level is 0.5 V_{P-P}.

The input resistance of the IF limiter amplifier is 1.8 kΩ (see Figure 1A). If the impedance of the filter is lower than 1.8 kΩ, connect an external resistor between Pin 1 and Pin 2 in parallel to provide the equivalent load impedance of the filter. Figure 1A shows the case that the impedance of the filter is 330 Ω.

The operating current of the emitter-follower of the IF limiter amplifier output is 200 µA. If the capacitive load is heavy, the negative half cycle of the output waveform may be distorted. This distortion can be reduced by connecting an external resistor between Pin 14 to GND to increase the operating current. The increased operating current by an external resistor is calculated as follows (see Figure 1B):

The increased operating current I_e (mA) = (V_{CC} - 1.0) / R_e (kΩ)

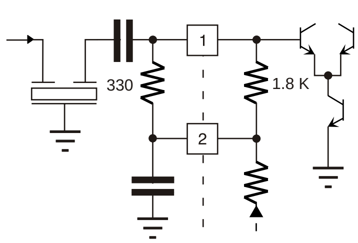


FIGURE 1A

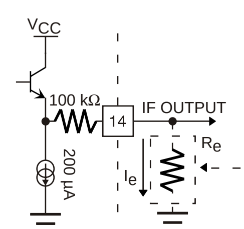


FIGURE 1B

CIRCUIT DESCRIPTION (CONT.)

The RSSI output is a current output. It converts to a voltage by an external resistor between Pin 15 and GND. The time constant of the RSSI output is determined by the product of the external converting resistance and parallel capacitance. When the time constant is longer, the RSSI output is less likely to be influenced by a disturbance or the component of amplitude modulation, but the RSSI output response is slower. Determine the external resistance and capacitance by the application.

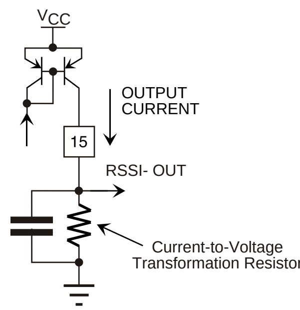


FIGURE 2 - RSSI OUTPUT STAGE

The slope of the RSSI curve characteristic can be modified by changing the external resistance. In this case, the maximum range of converted RSSI output voltage is GND level to about V_{CC} - 0.2 V (the supply voltage minus the collector saturation voltage of the output transistor).

In addition, the temperature characteristic of the RSSI output voltage can be modified by changing the temperature characteristic of the external resistor. Normally, the temperature characteristic of the RSSI output voltage is very stable when using a carbon resistor or metal film resistor with a temperature characteristic is 0 to 200 ppm/ °C.

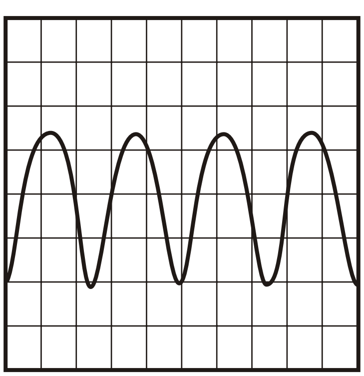
This product is very accurate, because the RSSI characteristic is trimmed individually.

AM Demodulation by Using the RSSI Output:

Although the distortion of the RSSI output is high because it is a logarithmic detection of the envelope to the IF input, AM can be demodulated simply by using the RSSI output. In this case, the input dynamic range that can demodulate AM is the inside of the linear portion of the RSSI curve characteristic (see Figure 3B).

This method does not have a feedback loop to control the gain because an AGC amplifier is not necessary (unlike the popularly used AM demodulation method). Therefore, it is a very useful application for some uses because it does not have the response time problem.

Figure 3A shows the AM demodulated waveform.



Operating Condition
V_{CC} = 3 V, f_{IN} = 10.7 MHz,
fm = 40 kHz, Mod = 80%,
V_{IN} = 40 dBm

100mV/div
100µs/div

FIGURE 3A - AM DEMODULATED WAVEFORM

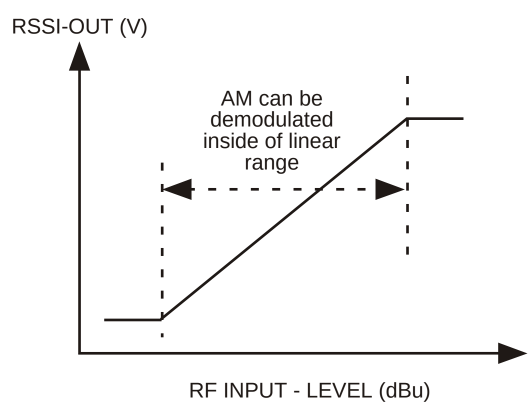


FIGURE 3B

CIRCUIT DESCRIPTION (CONT.)

FM Detector:

The FM detector is included in the quadrature FM detector using a Gilbert multiplier.

It is suitable for high speed data communication because the demodulation bandwidth is over 1 MHz.

The phase shifter is connected between Pin 14 (IF limiter output) and Pin 13 (input detector). Any available phase shifter can be used: a LC resonance circuit, a ceramic discriminator, a delay line, etc.

Figure 4 shows the internal equivalent circuit of the detector.

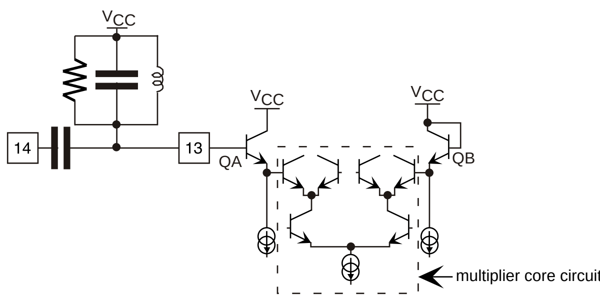


FIGURE 4

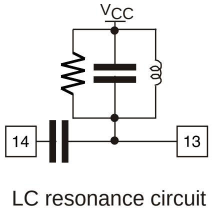
The signal from the phase shifter is applied to the multiplier (in the dotted line) through emitter-follower stage QA. When the phase shifter is connected between Pin 14 and Pin 13, note that the bias voltage to Pin 13 should be provided from an external source because Pin 13 is only connected to the base of QA.

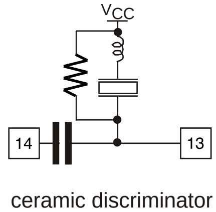
Because the base of QB (at the opposite side) is connected with the supply voltage, Pin 13 has to be biased with the equivalent voltage.

Using an LC resonance circuit is not a problem (see Figure 5). However, when using a ceramic discriminator, it is necessary to pay attention to bias. If there is a difference of the base voltages, the DC voltages of the multiplier do not balance. It alters the DC zero point or worsens the distortion of demodulation output.

The Pin 13 input level should be saturated at the multiplier; if this level is lower, it is easy to disperse the modulation output. Therefore, to have stable operation, Pin 13 should be higher than 100 mV_{P-P}.

The following figures show examples of the phase shifter.





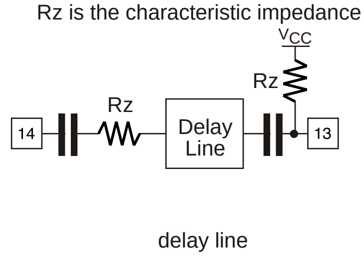


FIGURE 5 - EXAMPLES OF PHASE SHIFTER

CIRCUIT DESCRIPTION (CONT.)

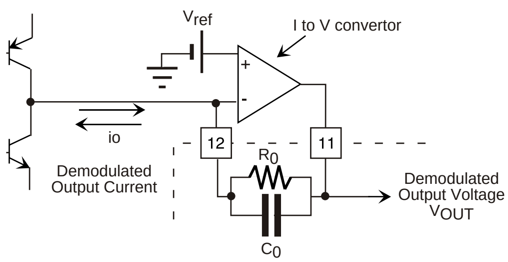
Establishing Demodulation Characteristics:

Generally, demodulation characteristics of FM detectors are determined by the external phase shifter. However, this product has a unique function which can optionally establish the demodulation characteristics by the time constant of the circuit parts after demodulation. The following explains this concept.

Figure 6 shows the internal equivalent circuit of the detector output stage.

The multiplier output current of the detector is converted to a the voltage by the internal OP AMP. The characteristic of this stage is determined by converting the current to voltage with resistor R_O and the capacitor C_O connected between Pin 11 and Pin 12 (see Figure 6).

In other words, the slope of the S-curve characteristic can be established optionally with resistor R_O without changing the constant of the phase shifter. The demodulated bandwidth can be established optionally by the time constant of this external resistor R_O and capacitor C_O inside of a bandwidth of the IF-filter and phase shifter. Figure 7 shows an example of this characteristic.



The -3 dB frequency Fc is calculated by the following:

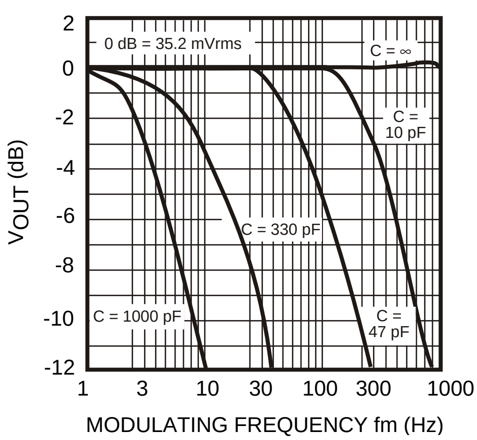
$$Fc = \frac{1}{2 \pi C_0 R_0}$$

The S-curve output voltage is calculated by the following as centering around the internal reference voltage V_{ref}:

$$V_{OUT} = V_{ref} \pm io \times R_0$$

Where V_{ref} = 1.4 V, maximum of current io = ±100 µA

FIGURE 6 - INTERNAL EQUIVALENT CIRCUIT OF DETECTOR OUTPUT STAGE



Operating Condition:

Measured by the standard test circuit.
Parallel resistor to phase shift coil = 1 kΩ.
f_{IN} = 10.7 MHz, modulation = ±100 kHz.
External capacitance C_O = 0~1000 pF.

FIGURE 7 - EXAMPLE: BANDWIDTH OF DEMODULATION VS. TIME CONSTANT CHARACTERISTIC

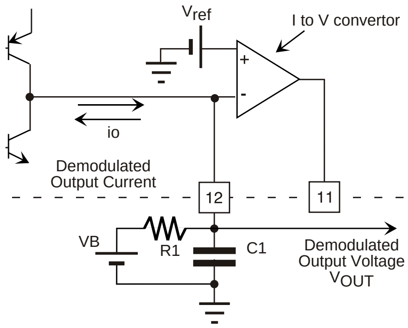
Center Voltage of Detector DC Output:

The center voltage of the detector DC output is determined by the internal reference voltage source. It is impossible to change this internal reference voltage source, but it is possible to change the center voltage by the following method.

As illustrated in Figure 8, the demodulated output current at Pin 12 is converted to the voltage by an external resistor R1 without using the internal OP AMP.

Figure 9 shows an example of a simple circuit that divides the supply voltage into halves using resistors. Since both circuits have a high output impedance, an external buffer amplifier should be connected.

CIRCUIT DESCRIPTION (CONT.)



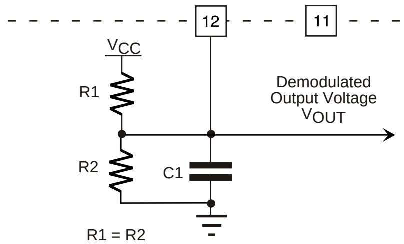
Demodulated Output Voltage V_{OUT} = VB ± R1 x io

Demodulated Bandwidth $Fc = \frac{1}{2\pi C1(1/gm)}$

1/gm is about 50 kΩ that is the output resistance of the multiplier.

Pin 11 is disconnected.

FIGURE 8 - EXAMPLE OF USING EXTERNAL REFERENCE SOURCE



Demodulated Output Voltage $V_{OUT} = V_{CC}/2$ ± R1 x io

Demodulated Bandwidth $Fc = \frac{1}{2\pi C1(1/gm)}$

1/gm is about 50 kΩ that is the output resistance of the multiplier.

Pin 11 is disconnected.

FIGURE 9 - EXAMPLE OF DIVIDING SUPPLY VOLTAGE INTO HALVES BY THE RESISTORS

Comparator:

The TK14588V contains a general purpose high-speed data comparator for the base band processing. Because the input stage is composed of PNP transistors, it is possible to operate from a minimum voltage of 0.2 V to the supply voltage minus 0.9 V (see Figure 10).

Moreover, as the HFE of this PNP transistor is over 100, the bias current is below 0.01 µA (this is below 10% of the value of the general products on the market using lateral PNP transistor at input stage).

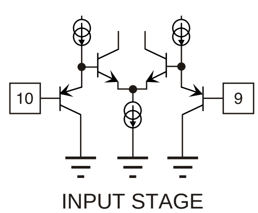


FIGURE 10 - COMPARATOR INPUT STAGE

CIRCUIT DESCRIPTION (CONT.)

Comparator (cont.):

Figure 11 shows the internal equivalent circuit of the comparator output stage. Because the comparator output is an open collector, it is suitable for many interface levels. This open collector output is connected with an electrostatic discharge protection diode at the GND side only; it is not connected with it at the power supply side in consideration of operating the voltage over the supply voltage of this IC.

When the collector pull-up resistor value is low, high operating currents result. To prevent interference to the other circuitry, the emitter of the output transistor is brought out independently at Pin 8.

Pin 8 is not connected with the substrate and other GND internal to the IC. Therefore, when operating this comparator, this terminal must be connected to GND.

When the comparator is operating at high speed, the etch pattern of Pins 7 and 8 (comparator output stage) should not be run close to the etch pattern of Pin 1 (IF input). The switching waveform of the comparator output may have an effect on the IF input and may add noise to the zero crossing of the demodulated waveform, resulting in cross over distortion.

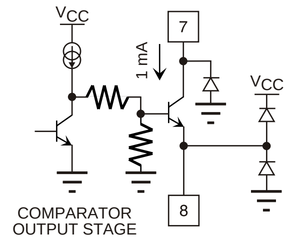


FIGURE 11 - COMPARATOR OUTPUT STAGE

Power Save Function:

Pin 5 is the control terminal for the battery save function. The ON/OFF operation of the whole IC can be switched by controlling the DC voltage at this terminal. Figure 12 shows the internal equivalent circuit of Pin 5.

Because it switches the bias circuit of the whole IC using the transistor in standby mode, it reduces the supply current to near zero. As the input terminal is connected with an electrostatic discharge protection diode at GND side only, it is possible to control the voltage above the supply voltage. It is possible to go into standby mode by disconnecting Pin 5, but it is not recommended because Pin 5 is a high impedance and may malfunction by an external disturbance.

When Pin 5 is disconnected, a suitable capacitor should be connected between Pin 5 and GND.

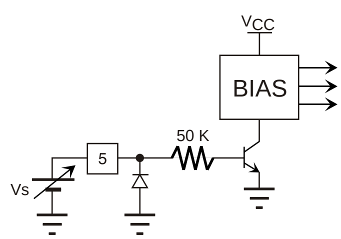
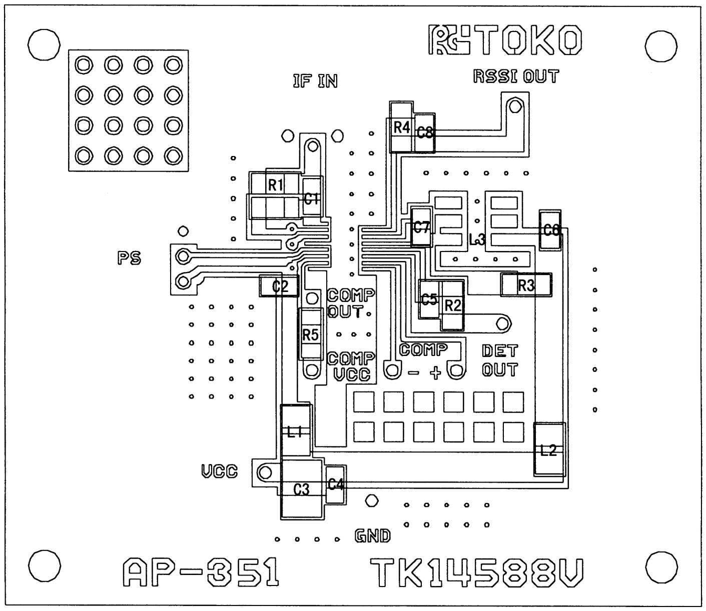


FIGURE 12

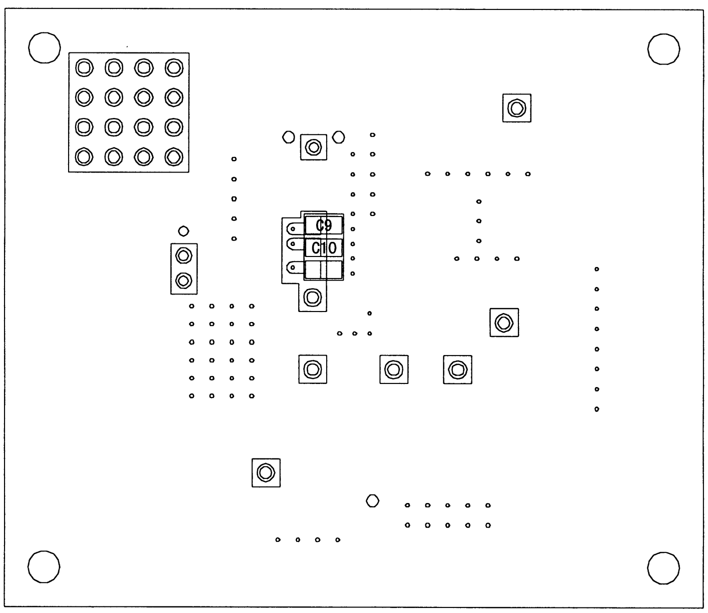
TEST BOARD

TK14588V Test Board

(THE SURFACE)



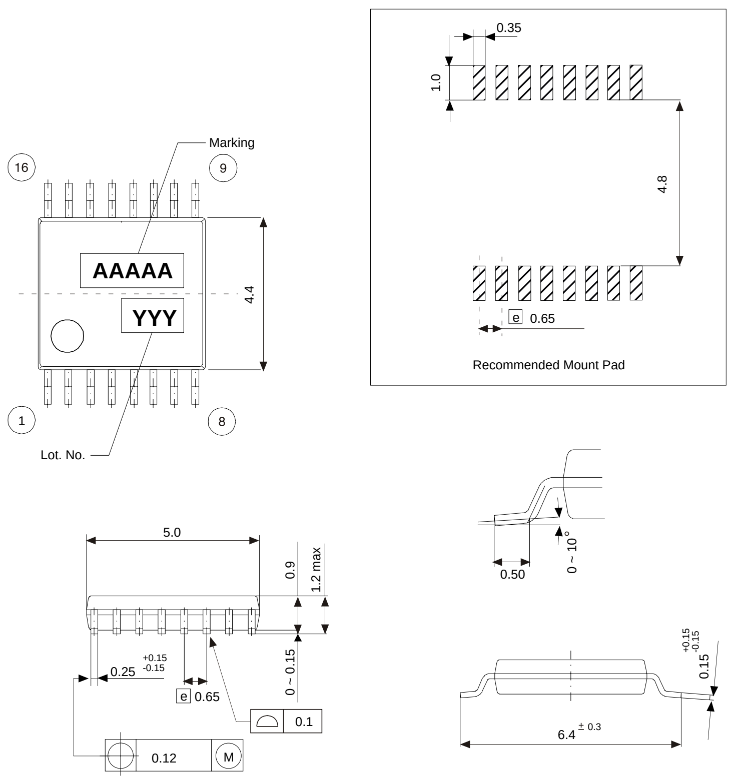
(THE REVERSE)



C1 = C2 = C4 = C6 = C8 = C9 = C10 = 0.01 µF
C3 = 4.7 µF, C5 = 1000 pF, C7 = 1 pF
R1 = 51 Ω, R2 = 51 kΩ, R3 = 3.3 kΩ, R4 = 12 kΩ, R5 = 3 kΩ
L1 = L2 = 10 µH
L3 = 836BH-0268 (TOKO)

PACKAGE OUTLINE

TSSOP-16



Dimensions are shown in millimeters
Tolerance: x.x = ± 0.2 mm (unless otherwise specified)

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