MSC8102 Asynchronous DSI Throughput

by Jason Streeter

The Freescale MSC8102 DSP device has a parallel slave peripheral port by which host processors can read and write directly to the MSC8102 internal memory, either synchronously or asynchronously. This direct slave interface (DSI) port allows fast data transfers to the internal SRAM (M1 or M2) without interrupting the SC140 core data. For applications using the DSI, it is important to know the performance capabilities and limitations of the MSC8102 peripherals. This application note examines the bandwidth capabilities of the MSC8102 DSI peripheral in asynchronous mode.

CONTENTS

1 DSI Basics

The DSI can operate as either a 32-bit or a 64-bit data bus slave peripheral. Because 32 of the data lines are shared with the 60x-compatible system bus, using the DSI is used in 64-bit mode requires the 60x bus to operate in 32-bit mode. In addition to the data lines, there are 19 DSI address signals that allow the host to access the entire range of MSC8102 memory and registers.

The DSI is a flexible interface that supports a variety of host processors. The host can use a dual- or single-strobe access to communicate with the DSI. The DSI sliding window addressing mode allows the host processor to communicate with the DSI using only 16 address signals instead of 19. Finally, the DSI supports host processors that are byte ordered in Big Endian, Little Endian, or Munged Little-Endian formats.

The DSI operates in either asynchronous or synchronous mode. In asynchronous mode, the DSI functions in an SRAM-like mode that does not require the host to supply a clock to the slave MSC8102. In synchronous mode, the DSI functions as an SSRAM-like interface and operates with a host-supplied clock. This application note focuses on the throughput for the asynchronous DSI mode. Asynchronous mode does not support burst transfers. However, the DSI has a write buffer and a read buffer to help increase the overall throughput because they allow the host to perform successive accesses without the overhead of wait states.

The DSI asynchronous throughput is affected by many parameters and conditions. First, the DSI shares external buses with other MSC8102 resources, such as the DMA controller and the TDMs. If the MSC8102 device uses these resources at the same time as the DSI, the DSI may have to wait to be granted access to the bus, which affects overall throughput. In addition, the DSI drives an acknowledge signal to indicate when it has completed a read or write transaction. The host must wait until the DSI stops driving the transfer acknowledge before the next access.

In most cases, the host processor needs to synchronize the transfer acknowledge with an internal clock, which adds latency to the access and reduces the throughput. The host processor memory controller timings also affect the throughput. Relaxing the timings greatly limits DSI performance. On the other hand, optimizing the host timings can result in improved DSI performance. Also, the DSI throughput depends on the MSC8102 local bus frequency. For example, if the local bus operates at 50 MHz, the throughput is less than if the local bus operates at 100 MHz. However, the DSI limits the DSI operational frequency to 70 MHz even if the local bus operates at 100 MHz.

2 Asynchronous DSI Connections and Timings

The throughput calculations discussed here are based on DSI timings on a logic analyzer. To understand the throughput calculations, the asynchronous connections and timings must be considered.

2.1 MSC8101 to MSC8102 DSI Connection

The asynchronous throughput performance measurements are taken using an MSC8102 Application Development System (ADS) board. This board has an MSC8101 host processor that connects to the MSC8102 slave device as shown in **Figure 1**. The system bus on the MSC8101 host processor connects to the DSI on the MSC8102 slave as if it were an external memory.

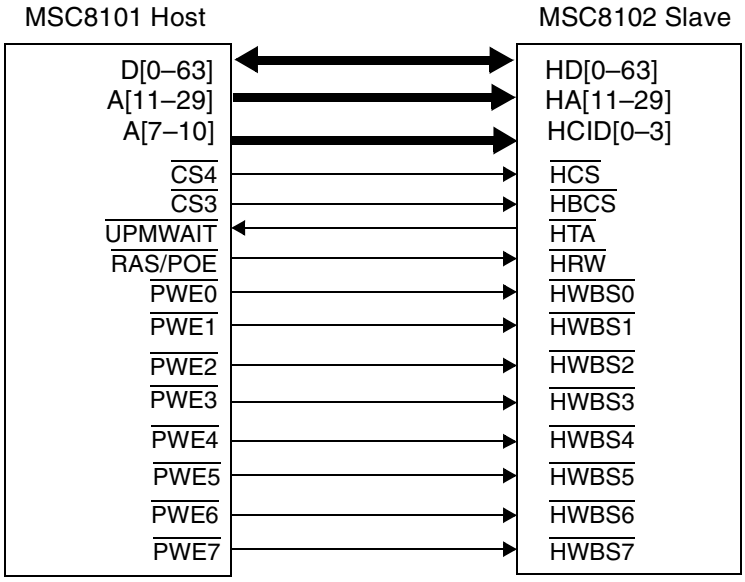

Figure 1. MSC8101 to MSC8102 Physical Connection

2.2 MSC8102 DSI Timings

The DSI timings are different, depending on whether the host processor reads from the DSI, writes to the DSI, or broadcasts data to multiple DSIs on multiple DSPs. The DSI communicates via a dual-strobe or a single-strobe method. The timings for each method are similar. This application note references only dual-strobe mode since this is the mode used to collect the throughput data for the DSI. This section illustrates the differences between reads, writes, and broadcast writes for dual-strobe accesses.

2.2.1 DSI Read Timings

Figure 2 illustrates the timings for an asynchronous DSI read as indicated in the *MSC8102 Technical Data* sheet. When the memory controller on the host processor is programmed, the MSC8102 DSI read timing specifications must be met to complete the transaction properly. For a read transaction, the address of the memory location or register must be driven first. Then, the host issues a chip select to enable the MSC8102 DSI. Since multiple MSC8102 devices can be connected, the MSC8102 samples the HCID[0–3] signals to determine which MSC8102 DSI is selected. If the HCID[0–3] signals match the CHIPID value that is located in DCIR internal register, the DSI is accessed. The host continues the transaction by asserting the $\overline{\text{HRDS}}$ signal and then later deasserting the signal. Meanwhile, the data becomes available for the MSC8101. The typical handshaking procedure is complete when the MSC8102 drives the $\overline{\text{HTA}}$ signal to notify the host processor that the data transfer is acknowledged.

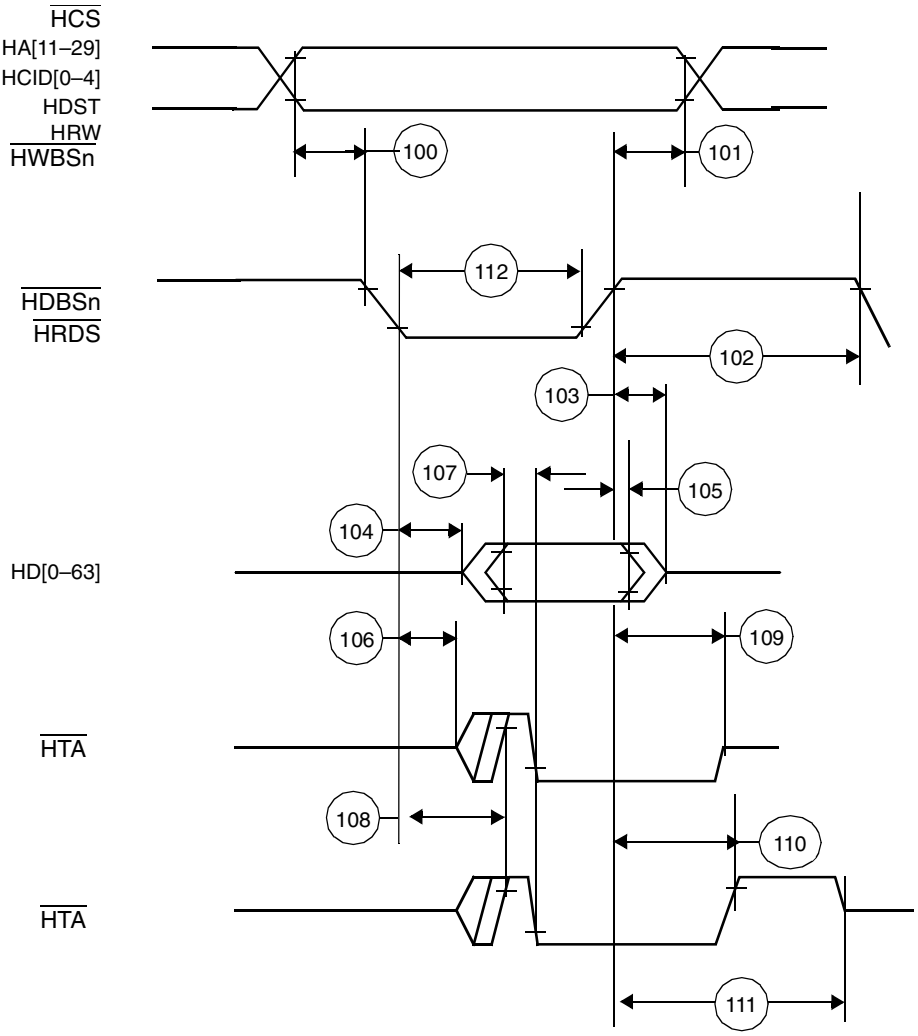

Figure 2. DSI Asynchronous Read Timings

2.2.2 DSI Write Timings

Figure 3 shows the timings for an asynchronous DSI write transaction as indicated in the *MSC8102 Technical Data* sheet. When the memory controller on the host processor is programmed, the MSC8102 write timing specifications must be met to implement the write transaction properly. A write transaction is almost exactly the same as a read transaction. For a write transaction, the address of the memory location or register must be driven first. Then, the host issues a chip select to enable the MSC8102 DSI. As with the read transaction, the HCID[0–3] signals are sampled to determine which MSC8102 DSI is selected. When the HCID[0–3] signals match the CHIPID value in the DCIR register, the DSI is accessed. The host continues the transaction by asserting the $\overline{\text{HWBS}}$ signal and then later deasserting the signal. Meanwhile, the data can be sampled by the MSC8102 DSI. The typical handshaking process is complete when the MSC8102 drives the $\overline{\text{HTA}}$ signal to notify the host processor that the data transfer is complete.

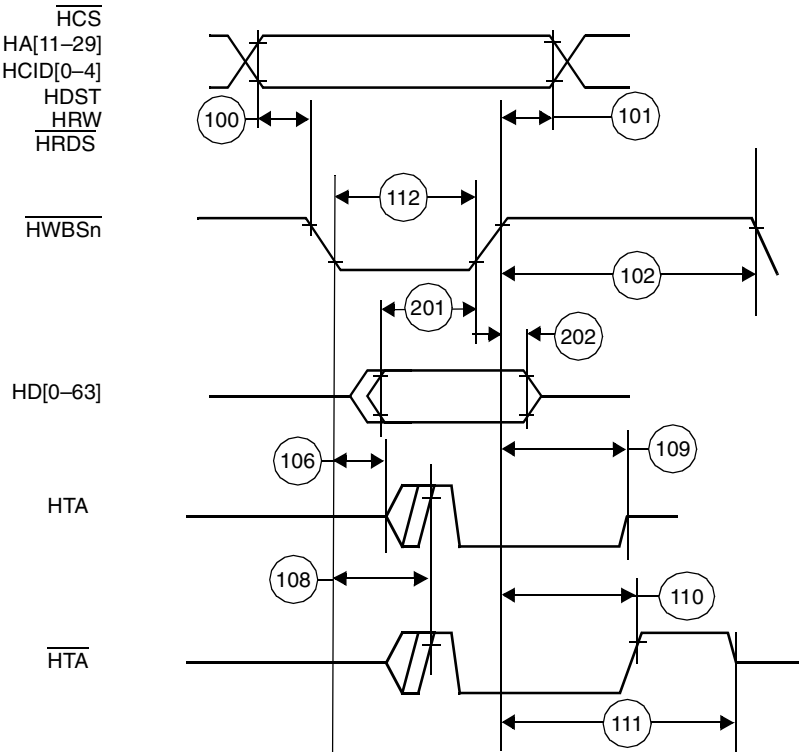

Figure 3. DSI Asynchronous Write Timings

2.2.3 DSI Broadcast Write Timings

Figure 4 illustrates the timings for an asynchronous DSI broadcast write transaction as indicated in the *MSC8102 Technical Data* sheet. The host processor memory controller timings must meet the MSC8102 broadcast write timings in the *MSC8102 Technical Data* sheet. A broadcast write is a write to multiple DSPs at the same time. The timings are the same as for a normal write transaction except that the $\overline{\text{HTA}}$ signal is not needed because multiple DSPs share the same signals. If the host processor broadcasts data to each DSP and the DSI from one DSP drives the $\overline{\text{HTA}}$ signal, the host processor cannot determine which DSP drove the $\overline{\text{HTA}}$ signal. The absence of an $\overline{\text{HTA}}$ signal increases DSI throughput for broadcast writes because the host processor does not have to wait to synchronize the transfer acknowledge signal internally. The rest of the broadcast write transaction is the same as a normal write transaction to the DSI.

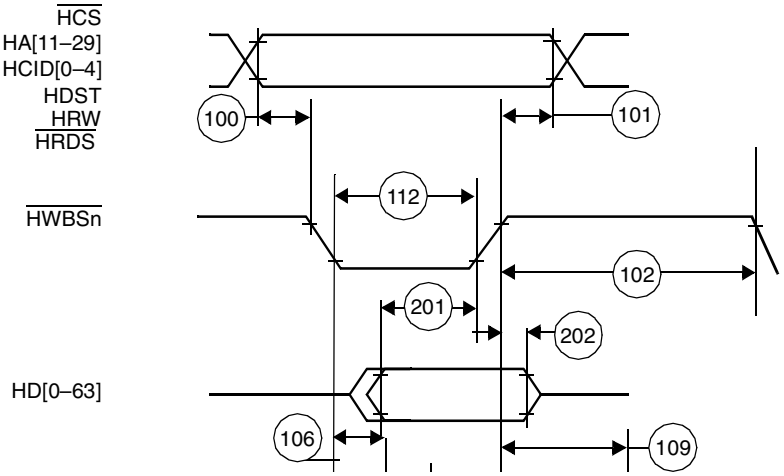

Figure 4. DSI Asynchronous Broadcast Write Timings

2.2.4 DSI Timing Values

The timing values associated with the preceding diagrams are listed in **Table 1**. These values are directly from the *MSC8102 Technical Data* sheet and are based on T_{REFCLK}, which is the local bus frequency. These timing values are used to generate the theoretical throughput value in **Section 3**.

Table 1. DSI Asynchronous Mode Timing

No.	Characteristics	Min	Max	Unit
100	Attributes[1] setup time before strobe ($\overline{\text{HWBS[n]}}$) assertion	3.6	—	ns
101	Attributes[1] hold time after data strobe deassertion	2.4	—	ns
102	Read/Write data strobe deassertion width[2] • DCR[HTAAD] = 1 — Consecutive access to the same DSI — Different device with DCR[HTADT] = 01 — Different device with DCR[HTADT] = 10 — Different device with DCR[HTADT] = 11 • DCR[HTAAD] = 0	 $1.8 + T_{REFCLK}$ $5 + T_{REFCLK}$ $5 + (1.5 \times T_{REFCLK})$ $5 + (2.5 \times T_{REFCLK})$ $1.8 + T_{REFCLK}$	—	 ns ns ns ns ns
103	Read data strobe deassertion to output data high impedance	—	7.8	ns
104	Read data strobe assertion to output data active from high impedance	3.8	—	ns
105	Output data hold time after read data strobe deassertion	2.2	—	ns
106	Read/Write data strobe assertion to $\overline{\text{HTA}}$ active from high impedance	3.9	—	ns
107	Output data valid to $\overline{\text{HTA}}$ assertion	1	—	ns
108	Read/Write data strobe assertion to $\overline{\text{HTA}}$ valid	—	9.8	ns
109	Read/Write data strobe deassertion to output $\overline{\text{HTA}}$ high impedance. (DCR[HTAAD] = 0, $\overline{\text{HTA}}$ at end of access released at logic 0)	—	6.5	ns
110	Read/Write data strobe deassertion to output $\overline{\text{HTA}}$ deassertion. (DCR[HTAAD] = 1, $\overline{\text{HTA}}$ at end of access released at logic 1)	—	9.2	ns

Table 1. DSI Asynchronous Mode Timing (Continued)

No.	Characteristics	Min	Max	Unit
111	Read/Write data strobe deassertion to output $\overline{\text{HTA}}$ high impedance. (DCR[HTAAD] = 1, $\overline{\text{HTA}}$ at end of access released at logic 1 • DCR[HTADT] = 01 • DCR[HTADT] = 10 • DCR[HTADT] = 11	—	 $5 + T_{REFCLK}$ $5 + (1.5 \times T_{REFCLK})$ $5 + (2.5 \times T_{REFCLK})$	 ns ns ns
112	Read/Write data strobe assertion width	$1.8 + T_{REFCLK}$	—	ns
201	Host data input setup time before write data strobe deassertion	2	—	ns
202	Host data input hold time after write data strobe deassertion	1.3	—	ns
NOTES: 1."Attributes" refers to the following signals: $\overline{\text{HCS}}$, HA[11–29], HCID[0–4], HDST, HRW, $\overline{\text{HRDS}}$, and $\overline{\text{HWBSn}}$.				

3 Theoretical Throughput

When actual throughput measurements are obtained, it is good practice to have a theoretical value for comparison. Most throughput measurements quoted by DSP manufacturers are based on timing values and timing diagrams similar to those illustrated in **Section 2**, which do not necessarily represent what happens in the DSP. The throughput measurements based on timings in a data sheet illustrate the performance the DSP can achieve, but host processors typically cannot support this type of performance. For example, completing an asynchronous DSI read transaction requires a minimum of 38.96 ns if the MSC8102 DSI operates at 70 MHz. This value comes from adding the following timing values from **Figure 2** and **Figure 5**:

- *Timing 100*. Set-up time before strobe assertion (3.6 ns).
- *Timing 111*. Read/Write data strobe deassertion to output $\overline{\text{HTA}}$ high impedance where DCR[HTADT] = 01 (5 ns + 14.28 ns).
- *Timing 112*. Read/Write data strobe assertion width (1.8 ns + 14.28 ns).

The throughput is calculated by the following equation in terms of MB/second.

$$T = (N) / (t \times M) \qquad \textbf{Equation 1}$$

T = Throughput

N = Number of bytes transferred

t = Time of transaction

$M = 2^{20} = 1, 048, 576$

If N = 8 bytes for one 64-bit transfer and t = 38.96 ns as calculated from the timings, the throughput is 195.83 MB/s. This is a large number for an asynchronous read transfer and is not representative of reality. Host processors operating asynchronously generally do not meet this level of performance. What really happens during the read transaction is that the MSC8102 device sends an $\overline{\text{HTA}}$ signal to acknowledge the transaction. On the MSC8102ADS, the MSC8101 host must synchronize the $\overline{\text{HTA}}$ signal with the SIU, which may add one or two MSC8101 system bus clock cycles. The same synchronization must also occur for the deassertion of the $\overline{\text{HTA}}$ signal, which may increase the cycle count by one or two cycles.

The DSI asynchronous read transaction, which is programmed into the MSC8101 UPM memory controller as a single read, requires 5 cycles with a system bus clock of 66 MHz. The throughput is calculated by adding the cycles of the UPM and synchronization of the $\overline{\text{HTA}}$ signal and applying the result to **Equation 1**. If the MSC8101 system bus operates at 66 MHz, the cycle time is 15.15 ns. If we assume 5 cycles for the UPM read and 4 cycles for the $\overline{\text{HTA}}$ synchronization, the throughput is 55.95 MB/s. This throughput is more representative of the observed behavior for a MSC8102 DSI read transaction on the MSC8102ADS. **Table 2** shows the distinction between the theoretical throughput based on the timings versus the theoretical throughput based on the host programming and synchronization.

Table 2. Theoretical DSI Throughput

Type Of Transaction	DSI Theoretical Throughput Based On Timings	DSI Theoretical Throughput Based On Host Programming And Synchronization
Single Read	195.83 MB/s	55.95 MB/s
Single Write	195.83 MB/s	55.95 MB/s
Broadcast Single Write	213.35 MB/s	62.95 MB/s
Host DMA Read	195.83 MB/s	62.95 MB/s
Host DMA Write	195.83 MB/s	71.94 MB/s
Broadcast Host DMA Write	213.35 MB/s	100.71 MB/s

4 Actual Throughput

The actual throughput measurements for the DSI asynchronous mode greatly depend on such conditions as DSI data bus width, mode of operation, load on the MSC8102 local bus, load on the MSC8101 system bus, single or host DMA accesses, and local bus frequency.

4.1 Asynchronous Throughput Measurements

The conditions, modes and register settings used to obtain the DSI throughput performance measurements discussed in this section are as follows:

- MSC8102ADS Board set-up includes an MSC8101 host processor.
- The DSI operates in 64-bit mode and in Dual-Strobe mode.
- The DCR register value is 0x28A00000 so that read prefetch is on and the $\overline{\text{HTA}}$ signal drive time is between 0.5 and 1 internal MSC8102 bus clock cycles.
- The MSC8102 local bus is handling no other activities.
- The MSC8102 device operates between 0 and 70 MHz.
- The MSC8101 system bus operates at 66 MHz.
- Read and write accesses are back-to-back and to consecutive MSC8102 memory locations (0x0100000–M2 memory).
- Host DMA means that the MSC8101 uses its DMA controller to transfer data with better performance for back-to-back memory transfers.
- The pipeline maximum depth bit has a value of 0 in the MSC8101 BCR for a pipeline depth of 1.
- Single reads and writes are issued using the MSC8101 SC140 core **move** instructions.

- Throughput measurements for host DMA accesses are taken over an average of four transactions.
- Throughput measurements for single reads and writes are taken over an average of four transactions.

4.2 Single Read Throughput

The maximum DSI single read performance is based on accesses to the MSC8102 M2 memory. **Figure 5** shows the timings obtained from the logic analyzer. The host clock for reference is the MSC8101 system bus clock by which the UPM controls the external memory accesses. The figure illustrates the address lines, chip select, read enable signal, and transfer acknowledge signal as it pertains to the read transaction—all in accordance with the timing diagram illustrated in **Section 2.2.1**, *DSI Read Timings,* on page 3. The throughput for consecutive read accesses is calculated to be 48.65 MB/s. This value translates into approximately 10.3 MSC8101 bus clock cycles and is averaged over four consecutive read transactions. Since the MSC8101 core issues the transactions with a **move** instruction, the SC140 core stalls for the duration of the transaction. If the SC140 core operates three times faster than the system bus clock, the SC140 core stalls for $10.3 \times 3 = 30.9$ core clock cycles.

Note: The system bus clock is not connected to the MSC8102 but is illustrated in **Figure 5** because the memory controller signals are based on this clock.

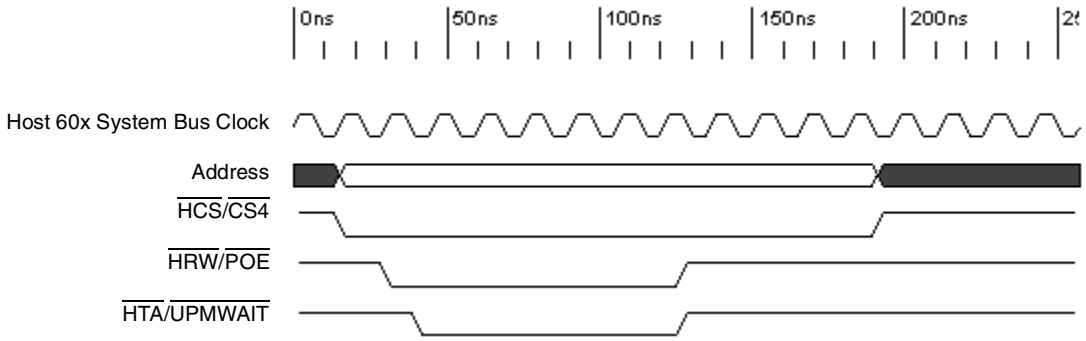

Figure 5. Asynchronous Single Read

4.3 Single Write Throughput

The maximum DSI single write performance is based on timings obtained using a logic analyzer after writing to consecutive memory addresses. **Figure 6** shows the results obtained from the logic analyzer, with the host clock operating at 66 MHz. The figure illustrates the address lines, chip select, write enable strobe, and transfer acknowledge signal as it pertains to the timing diagram in **Section 2.2.2**, *DSI Write Timings,* on page 4. The throughput for consecutive write accesses is calculated to be 45.96 MB/s. This value translates into approximately 10.95 MSC8101 bus clock cycles and is averaged over four consecutive write transactions to the MSC8102 M2 memory. As with the read transaction, the MSC8101 core issues the transaction with a **move** instruction. The SC140 core stalls for the duration of the transaction. If the SC140 core operates three times faster than the system bus clock, the SC140 core stalls for $10.95 \times 3 = 32.85$ core clock cycles.

Note: The $\overline{\text{HTA}}$ signal is connected to the MSC8101 $\overline{\text{UPMWAIT}}$ signal. The transfer acknowledge is used to extend the MSC8101 read and write accesses until the MSC8102 DSI can complete the transaction. The time between the deassertion of the chip select and the next address is representative of the host transfer acknowledge extending the write transaction.

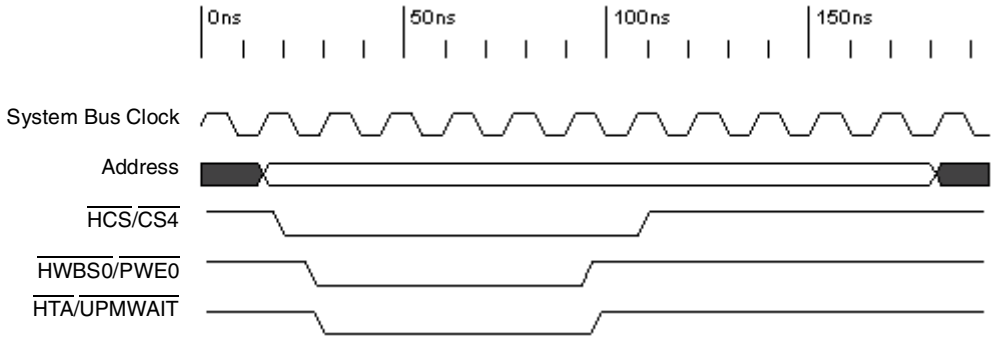

Figure 6. Asynchronous Single Write

4.4 Broadcast Single Write Throughput

The maximum DSI single broadcast write performance is based on consecutive writes to MSC8102 M2 memory. **Figure 7** shows one broadcast write transaction obtained from the logic analyzer. The figure shows the host clock, address lines, chip select, and write enable signal. The throughput for consecutive broadcast write accesses is calculated to be 55.93 MB/s, which translates into approximately nine MSC8101 bus clock cycles. This value is averaged over four consecutive broadcast write transactions. As for the DSI read and writes, the MSC8101 core stalls for the duration of the transaction. If the SC140 core operates three times faster than the 60x-compatible bus clock, the SC140 core stalls for 9× 3 = 27 core clock cycles. The broadcast write is clearly faster than the single write transaction because the transfer acknowledge is not necessary since the host cannot determine which DSP drove the $\overline{\text{HTA}}$ signal.

Note: The DSI broadcast write mode is used to broadcast data to the multiple MSC8102s. In this type of configuration, the $\overline{\text{HTA}}$ signal is shared between the MSC8102s. The $\overline{\text{HTA}}$ is not needed for broadcast mode because there would be contention between these devices.

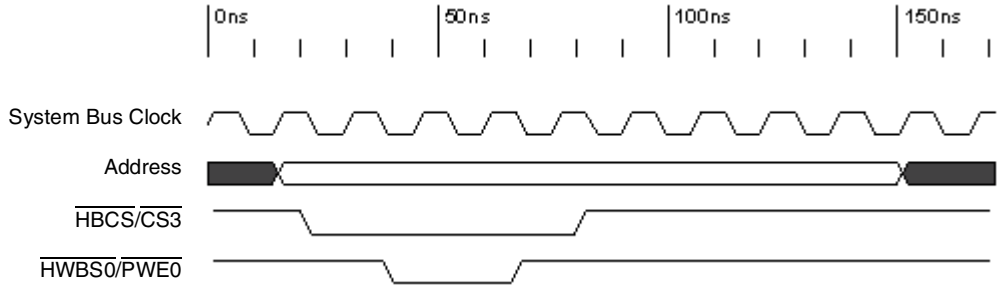

Figure 7. Asynchronous Broadcast Single Write

4.5 Host DMA Read Throughput

The maximum host DMA read performance is based on timings illustrated in **Figure 8**. The figure shows the host clock, which is the MSC8101 system bus clock by which the UPM controls the external memory accesses. The figure also illustrates the address lines, chip select, read enable signal, and transfer acknowledge signal. The throughput for consecutive read accesses is calculated to be 61.28 MB/s, which translates into approximately 8.21 MSC8101 bus clock cycles averaged over four consecutive host DMA read transactions. DMA reduces the latency when reading from consecutive memory locations, thus increasing the throughput beyond that obtained in a single read transaction.

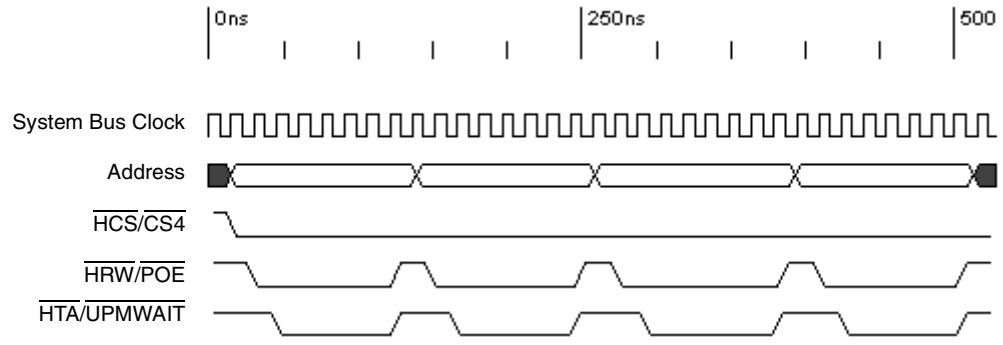

Figure 8. Asynchronous Host DMA Read

4.6 Host DMA Write Throughput

The maximum DSI host DMA write performance is calculated from the timing results shown in **Figure 9**. The figure shows the host clock, address lines, chip select, write enable strobe, and the transfer acknowledge signal. The throughput for consecutive host DMA write accesses is calculated to be 71.98 MB/s, which translates into approximately 6.99 MSC8101 bus clock cycles with a 66 MHz clock. This value is averaged over four consecutive write transactions. As for the host DMA read transactions, the host DMA write accesses reduce the latency when writing to consecutive memory locations.

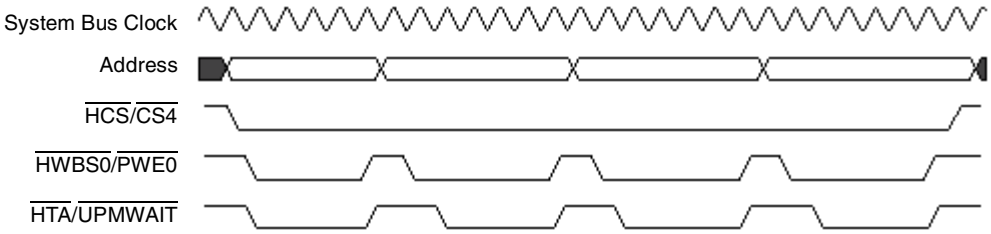

Figure 9. Asynchronous Host DMA Write

4.7 Broadcast Host DMA Write Throughput

The maximum host DMA broadcast write performance measurements are based on timings obtained using a logic analyzer. **Figure 10** shows the results from the logic analyzer during consecutive accesses to M2 memory. The host clock runs at 66 MHz and is the MSC8101 system bus clock by which the UPM controls the external memory accesses. In addition, the figure illustrates the address lines, chip select, and write enable signal. The UPMWAIT signal is not needed in the broadcast write as it was in the normal host DMA read and write transactions. The throughput for consecutive broadcast host DMA write accesses is calculated to be 91.37 MB/s, which translates into approximately 5.5 MSC8101 bus clock cycles, which is averaged over four consecutive write transactions. The broadcast host DMA write is clearly faster than the normal host DMA write transaction because a transfer acknowledge is not necessary.

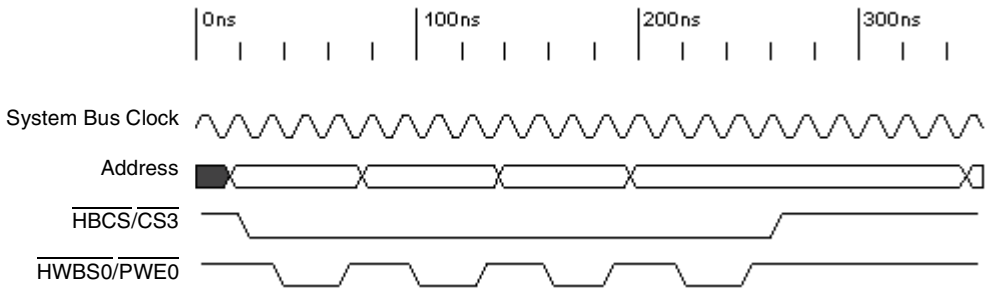

Figure 10. Asynchronous Broadcast Host DMA Write

5 Actual Throughput Versus Frequency

The observed maximum throughput for the asynchronous DSI reads and writes on the MSC8102ADS are given in **Section 4**. These numbers are based on the maximum frequency of the MSC8102 DSI, which is 70 MHz. Of course, the DSI does not have to operate at that frequency. In a system in which power is a consideration, the MSC8102 may be required to operate at a lower core and bus frequency. This section provides graphs based on observed data that illustrate the throughput obtained when the frequency of the MSC8102 local bus is changed.

5.1 Single Read Versus Local Bus Frequency

Figure 11 illustrates the DSI throughput for a single read transaction versus the local bus frequency of the MSC8102. The DSI operates on the basis of the local bus frequency.The maximum throughput occurs when the local bus frequency is 70 MHz or higher. Furthermore, the throughput drops by 30 percent when the frequency is reduced to 20 MHz.

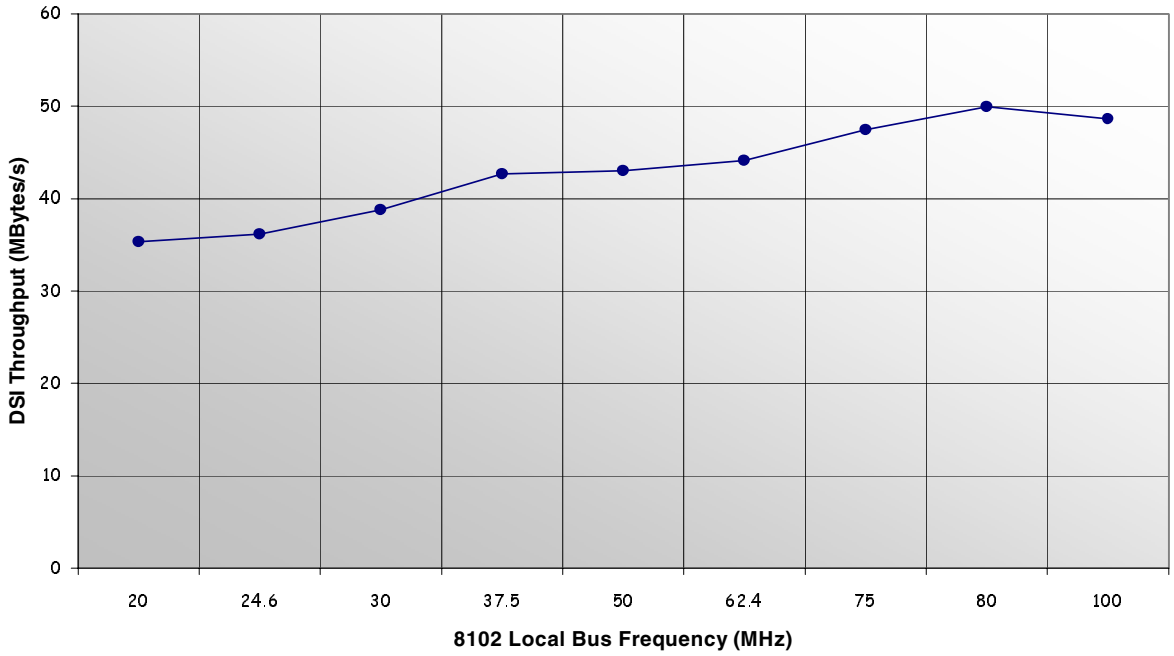

Figure 11. DSI Single Read Throughput Versus MSC8102 Local Bus Frequency

5.2 Single Write Versus Local Bus Frequency

Figure 12 illustrates the DSI throughput for a single write transaction versus the local bus frequency of the MSC8102. The DSI operates on the basis of the local bus frequency. The maximum observed throughput occurs when the local bus frequency is 70 MHz or higher. The throughput versus frequency for a single write is much different than for a single read. The single write throughput stays constant until the frequency drops below 30 MHz. At 20 MHz the throughput drops about 15 MB/s from the maximum throughput, which is a 33 percent decrease. The single write at 20 MHz is clearly lower than the single read at 20 MHz. This is in accordance with the 70 MHz data in which the single write throughput is less than the single read throughput. The single read data shows a 30 percent decrease over the entire frequency range, whereas the single write data falls off sharply at 30 MHz and shows a 33 percent decrease.

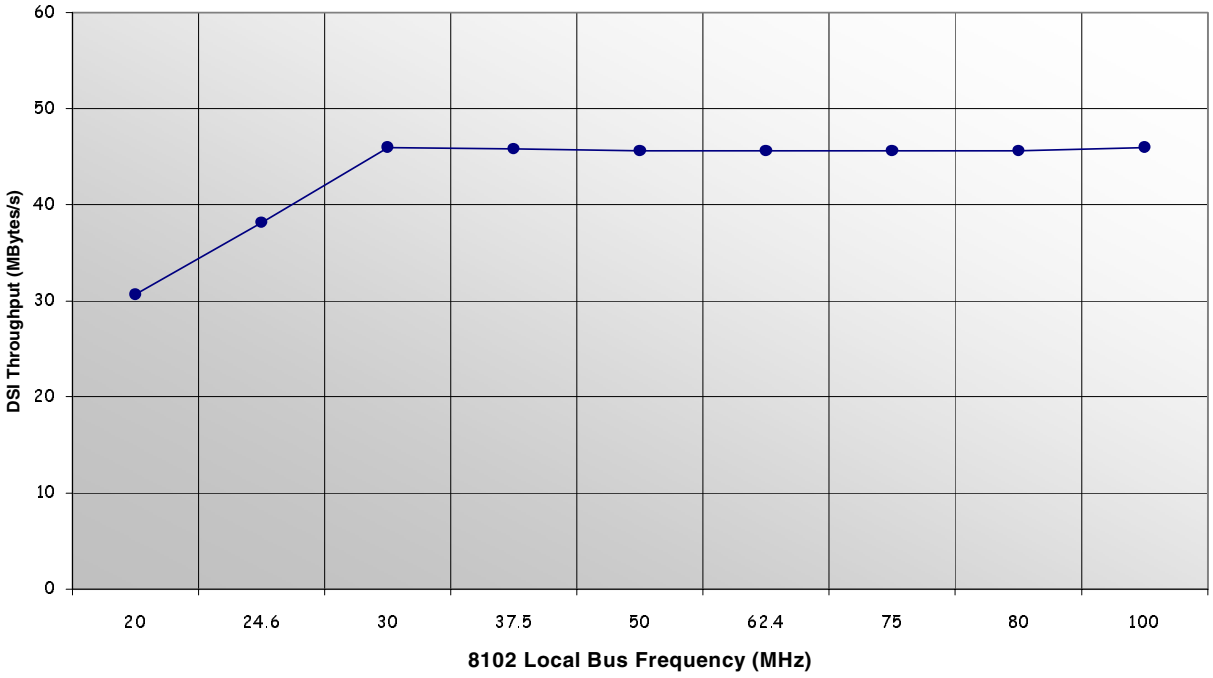

Figure 12. DSI Single Write Throughput Versus MSC8102 Local Bus Frequency

5.3 Host DMA Read Versus Local Bus Frequency

Figure 13 illustrates the DSI throughput for a host DMA read transaction versus the local bus frequency of the MSC8102. This chart illustrates that the observed maximum throughput occurs when the local bus frequency is 70 MHz or higher. Notice that at 20 MHz, the host DMA read is only 3 MB/s more than for a single read transaction. The reduction in MSC8102 local bus frequency affects the advantages gained by the MSC8101 DMA controller over the single read transactions. However, the DMA controller is still preferable since it does not stall the MSC8101 core, as a normal **move** instruction does.

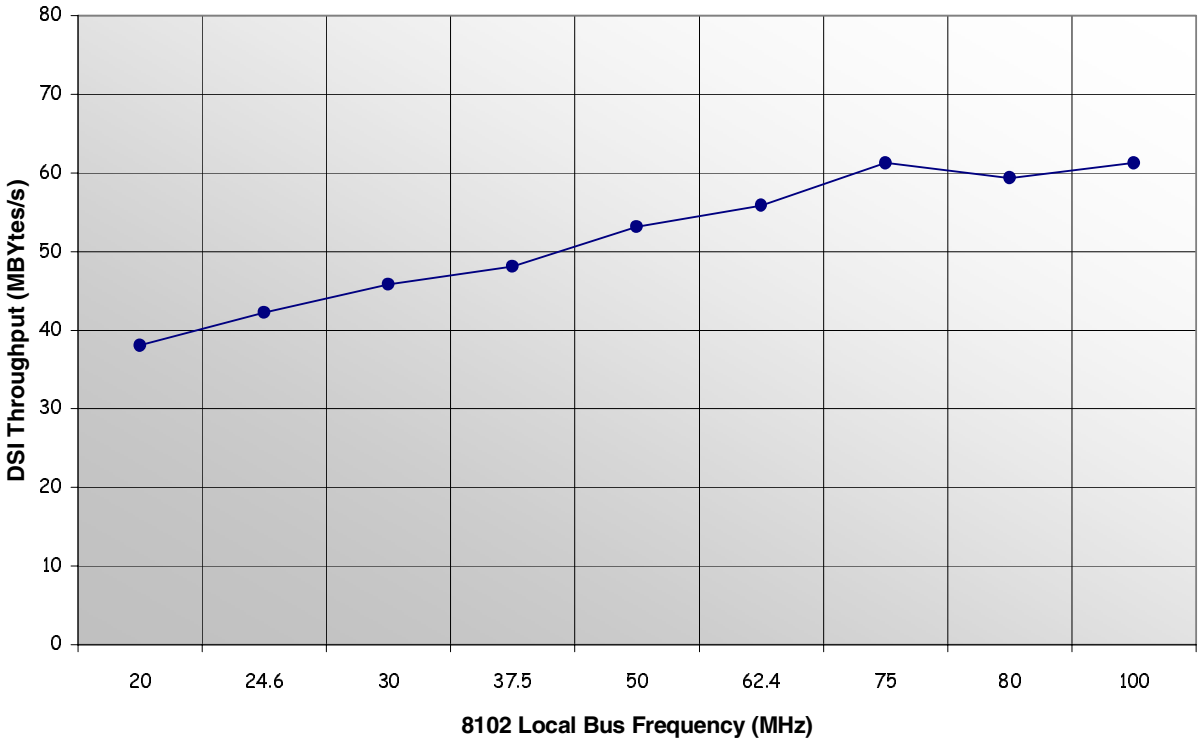

Figure 13. DSI Host DMA Read Throughput Versus MSC8102 Local Bus Frequency

5.4 Host DMA Write Versus Local Bus Frequency

Figure 14 illustrates the DSI throughput for a host DMA write transaction versus the local bus frequency of the MSC8102. This chart illustrates that the observed maximum throughput occurs when the local bus frequency is 70 MHz or higher. Notice that at 20 MHz, the host DMA write is about the same for a single write transaction. This is exactly what happened with the host DMA read transaction. The reduction in MSC8102 local bus frequency affects the advantages that the MSC8101 DMA controller gains over the single write transactions. However, the DMA controller is still preferable since it does not stall the MSC8101 core as a normal **move** instruction does. Also, the host DMA write throughput at 20 MHZ is less than the host DMA read throughput at 20 MHz. This is contrary to what the 70 MHz data suggested, in which the throughput of the host DMA write dominated the host DMA read. The host DMA write performance numbers decrease at a faster rate than the host DMA read performance numbers. this characteristic is also seen with the single read and write data discussed in **Section 5.1** and **Section 5.2**.

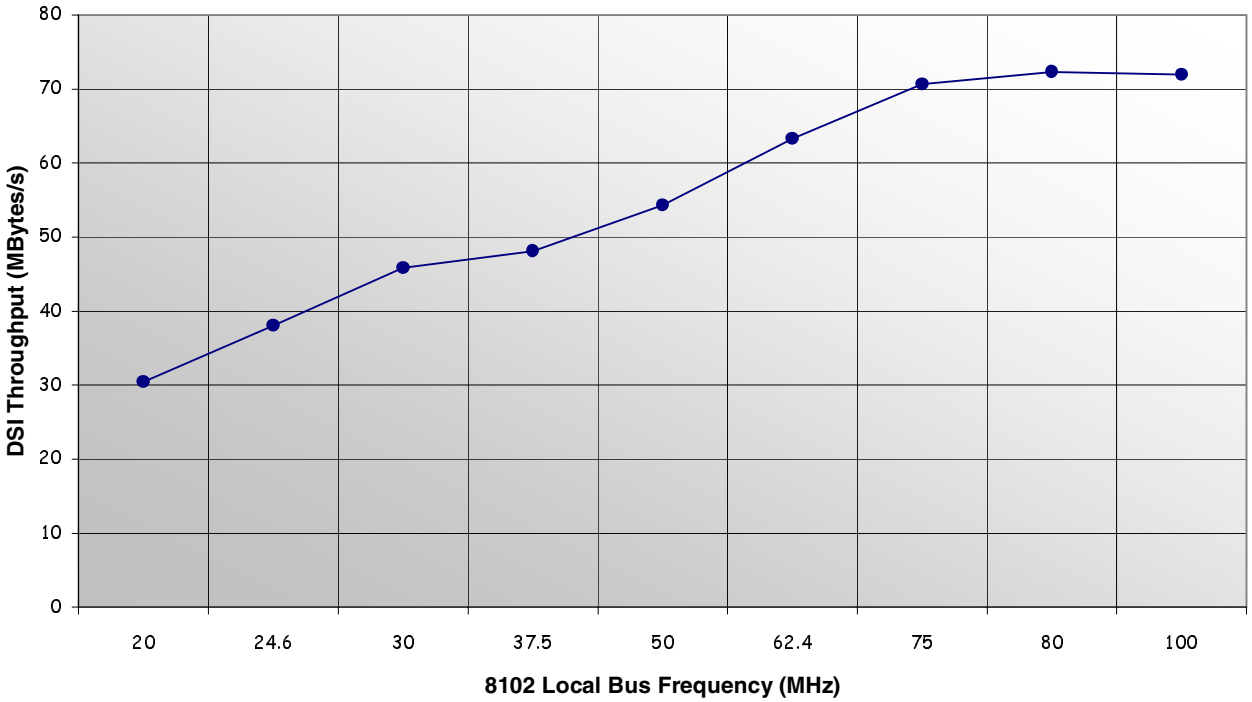

Figure 14. DSI Host DMA Write Throughput Versus MSC8102 Local Bus Frequency

6 Summary

The throughput for the MSC8102 DSI asynchronous 64-bit mode is obtained by examining the signals for single core reads/writes, host DMA reads/writes, broadcast single core writes, and broadcast host DMA writes:

- Single reads and writes have much lower performance numbers than the host DMA throughput results. The throughput numbers suggest that the MSC8101 core or host processor should use only single reads/writes when accessing a DSI register or very few memory addresses due to the lower performance.
- Since the throughput numbers are larger for host DMA reads and writes, it makes sense to use the DMA controller for reading and writing large amounts of data from the DSI.
- Broadcasting data in single transfers or host DMA transfers is much faster than not broadcasting. Therefore, it is important to broadcast data to the MSC8102 devices as much as possible. If there is only one MSC8102 in the system, broadcasting should be used all the time for maximum DSI performance.

The numbers provided in this application note are for one MSC8102 operating in asynchronous mode. The effects of capacitive loading when multiple MSC8102 devices are present lowers the throughput. It is assumed that other internal resources sharing the local bus are not in use on the MSC8102. If these modules are used, they require access to the local bus, adversely affecting DSI performance numbers.

The MSC8102 supports an extremely fast synchronous mode of operation, which accommodates bursting. In synchronous mode, the throughput of the MSC8102 DSI peripheral increases significantly. If the application requires more throughput than is indicated in this application note, synchronous DSI mode should be implemented.

7 References

The following Freescale documents are available at the web site listed on the back cover of this document.

- *MSC8102 Reference Manual*
- *MSC8102 Technical Data* sheet
- *MSC8101 Reference Manual*
- *MSC8101 Technical Data* sheet
- *MSC8102 Application Development System (MSC8102ADS) User's Manual*

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