Application Note

AN2414/D
Rev. 0, 04/2003

MC9328MX1/MXL CMOS Signal Interface (CSI) Module Supplementary Information

By Cliff Wong

1 Introduction

This document provides information on the architecture of the CSI module in addition to the datasheet. Programmers should read about this before they write software drivers for sensors.

There are 3 main topics being in concern. (1) Operation of FIFO Clear, (2) Sensor Interface Operation, (3) Sensor Interface Timing Details & (4) Principles of Statistical Block.

The design changes from rev1.0 to rev2.0 are also described.

2 Operation of FIFOs Clear

The RXFIFO & STATFIFO need to be reset and clear for every frame before the real data comes in. This is usually done with respect to the Start Of Frame (SOF) interrupt. However certain degree of control is provided for the user, through setting the FIFO Clear Control (FCC) bit in the CSI Control Register 1. There are 2 different modes.

2.1 Synchronous FIFO Clear

"SYNC Clear" means FIFO is being reset and cleared at the time when SOF arrives. There is a bug in MX1 rev1.0. It has been fixed in MX1 v2.0, but the mechanism is a little bit different.

MX1 v1.0

SYNC Clear works according to the settings of FCC, CLR_RXFIFO & CLR_STATFIFO bits. Sync mode is selected by setting FCC = '1'. However FIFO clear would not take place until CLR_RXFIFO & CLR _STATFIFO bits are set to '1'. Then FIFO clear operation will be effective on next SOF. After the operation has been completed, CLR_RXFIFO & CLR_STATFIFO bits are reset by interal logic, software needs to set them again before next frame arrives.

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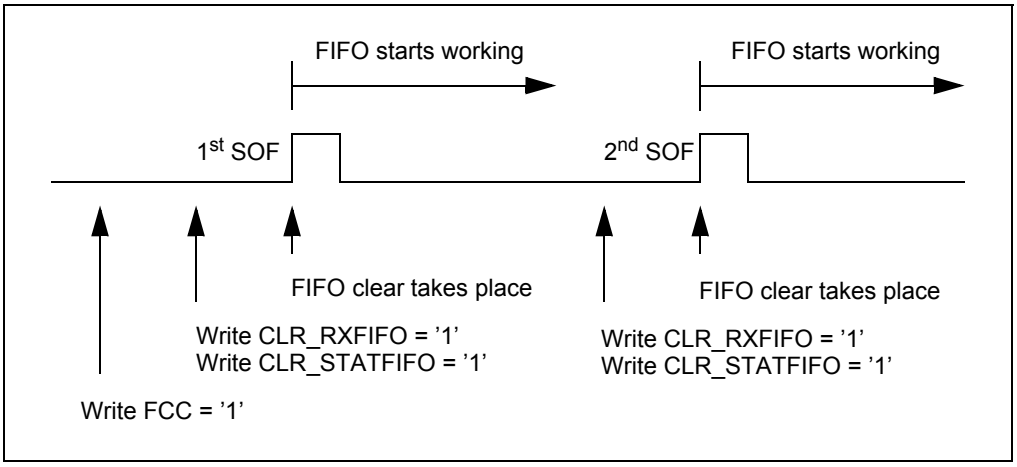

Figure 1.

MX1 v2.0

SYNC FIFO Clear is selected by setting FCC bit to '1'. This bit only needs to be set in the init code. Once it's set, CLR_RXFIFO & CLR_STATFIFO bits are ignored. FIFO clear operation will take place automatically on every SOF.

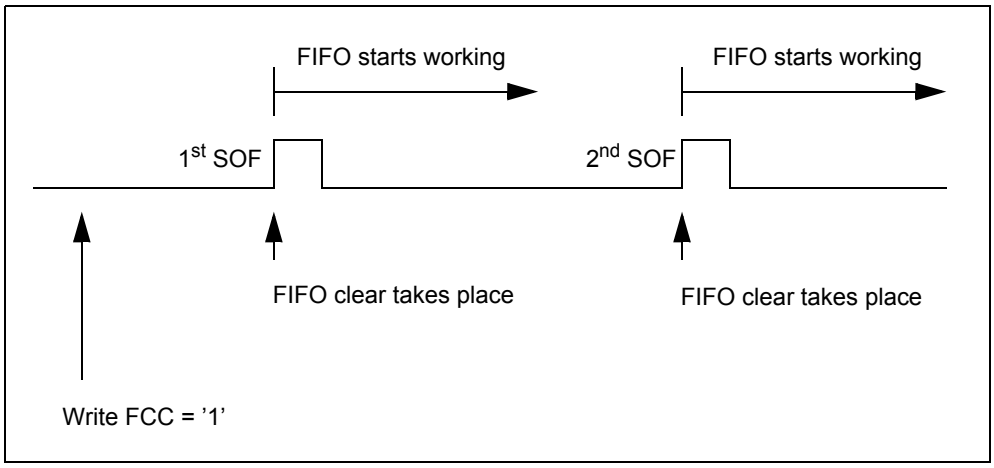

Figure 2.

2.2 Asynchronous FIFO Clear

MX1 v1.0 & v2.0

There is no change from MX1 v1.0 to v2.0 for this part.

"ASYNC Clear" means that FIFOs are cleared immediately at the time when CLR_RXFIFO and CLR_STATFIFO bits are set. For RXFIFO, it stars to work ASAP after reset. For STATFIFO, it is kept at the reste state until next SOF arrives.

Proper usage should be :

1. In the int code, clear FCC bit to '0' to select ASYNC clear mode.

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2. Set CLR_STATFIFO to ’1’, then STAT FIFO is cleared immediately & kept at reset state.
3. When SOF arrives, STAT FIFO is released from reset state and starts working.
4. Set CLR_RXFIFO to ’1’, then RX FIFO is cleared immediately & re-enter work mode at the same time.
5. After the arrival of SOF, CLR_STATFIFO & CLR_RXFIFO are both reset to ’0’ by internal logic.
6. For next frame, need to repeat 2 - 6.

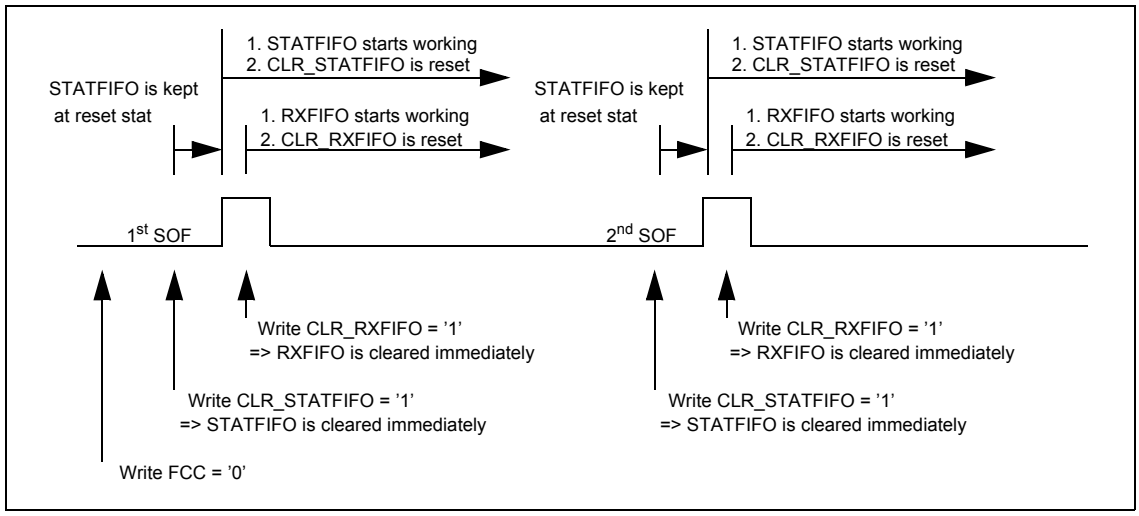

Figure 3.

3 Sensor Interface Operation

3.1 Gate Clock Mode

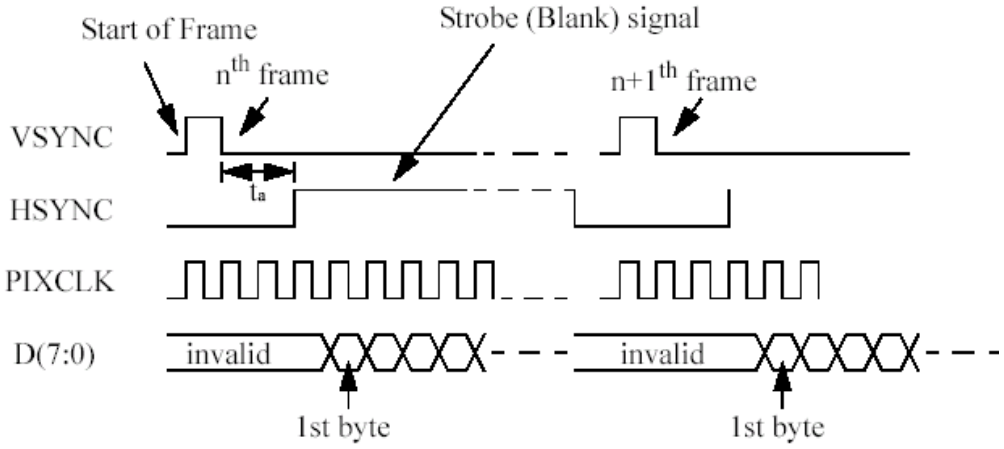

Figure 4.

Frame starts with a positive pulse on VSYNC. This triggers a SOF interrupt and resets the internal logic at the same time. The polarity of SOF is programmable, i.e. triggered by rising or falling edge.

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HSYNC is an active high signal that encapsulates valid pixel clocks. HSYNC & PIXCLK are passed through a logical-AND operation to generate valid pixel clocks.

HSYNC & PIXCLK => Valid PIXCLK
So, data is latched on every valid pixel clock.

3.2 Non-Gated Clock Mode

Frame starts with a pulse on VSYNC. This triggers a SOF interrupt and resets the internal logic at the same time. The polarity of SOF is programmable, i.e. triggered by rising or falling edge.

HSYNC is ignored in this case. Every incoming pixel clock is treated as valid and leading to a data-latch operation.

Motorola sensors fall into this category.

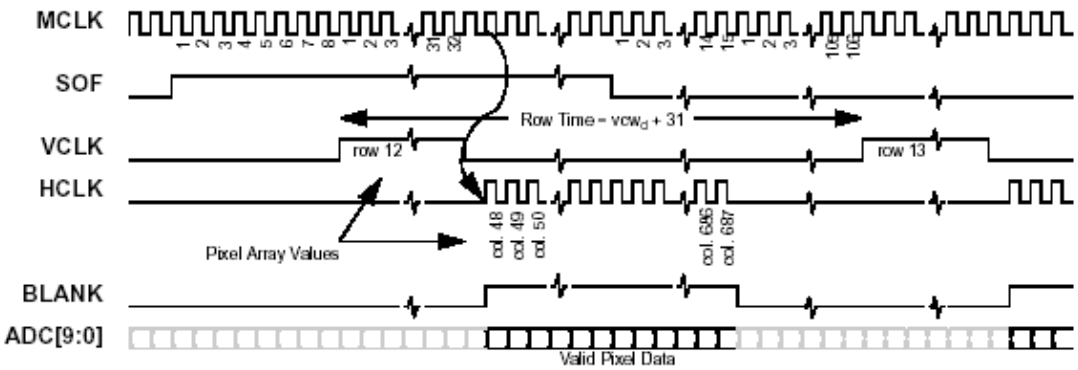

Figure 5.

Typical pin connection for Motorola sensor is:

Table 1.

Pin Name	Sensor	MX1
Start Of Frame	SOF	VSYNC
Horizontal Sync	BLANK	HSYNC (Ignored)
Bayer Data	ADC[9..2]	D[7..0]
	ADC[1..0]	Ignored

In this case, BLANK signal on sensor is exactly matching with what we expect to have on HSYNC. However, since there is no dummy pixel clock, i.e all pixel clocks going from sensor are valid, there is no need to enable Gated-clock mode, although it is not harmful to have this mode enabled.

3.3 CCIR656 Mode

There is no direct support on CCIR656 interface. The CSI is only able to receive raw data stream but not to do any decoding. Decoding should rely on software, in expense of computing loading.

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4 Sensor Interface Timing

4.1 Gated Clock Mode, Pixel Clock Rising-Edge Active

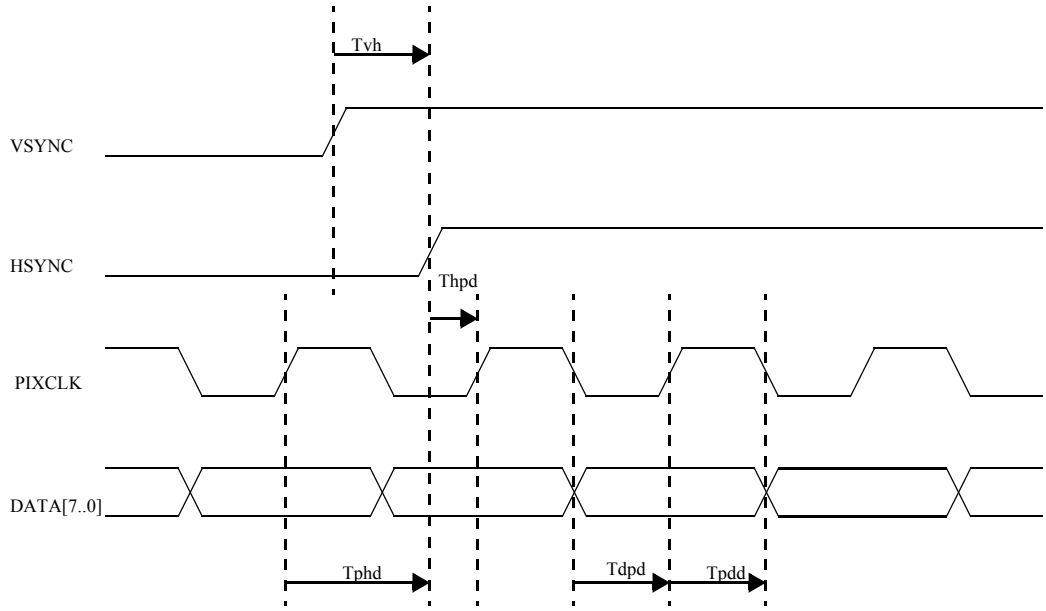

Figure 6.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
PIXCLK Freq		0	-	48	MHz
PIXCLK High Time	Tph	10.42	-	-	ns
PIXCLK Low Time	Tpl	10.42	-	-	ns
Data Valid to PIXCLK High	Tdpd (Setup Time)	3	-	-	ns
PIXCLK High to Data Invalid	Tpdd (Hold Time)	2	-	-	ns
HSYNC Valid to PIXCLK High	Thpd (Setup Time)	3	-	-	ns
PIXCLK High to HSYNC Invalid	Tphd (Hold Time)	Tph / 2	-	-	ns
VSYNC Valid to HSYNC Valid	Tvh	200	-	-	ns

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4.2 Gate-Clock Mode, Pixel Clock Falling-Edge Active

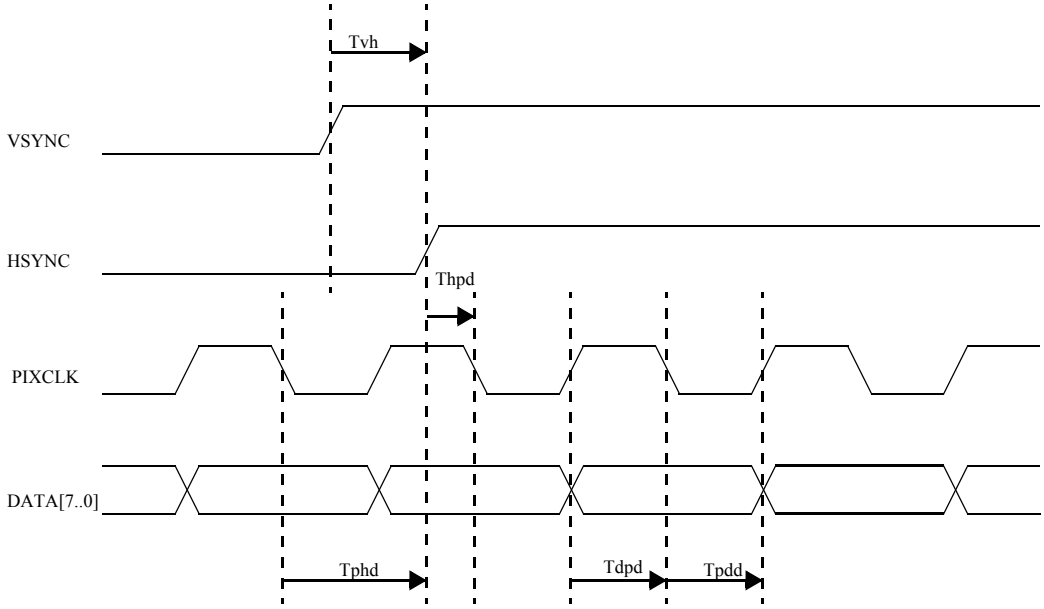

Figure 7.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
PIXCLK Freq		0	-	48	MHz
PIXCLK High Time	Tph	10.42	-	-	ns
PIXCLK Low Time	Tpl	10.42	-	-	ns
Data Valid to PIXCLK Low	Tdpd (Setup Time)	3	-	-	ns
PIXCLK Low to Data Invalid	Tpdd (Hold Time)	2	-	-	ns
HSYNC Valid to PIXCLK Low	Thpd (Setup Time)	3	-	-	ns
PIXCLK Low to HSYNC Invalid	Tpld (Hold Time)	Tpl / 2	-	-	ns
VSYNC Valid to HSYNC Valid	Tvh	200	-	-	ns

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4.3 Non-Gated Clock Mode, Pixel Clock Rising-Edge Active

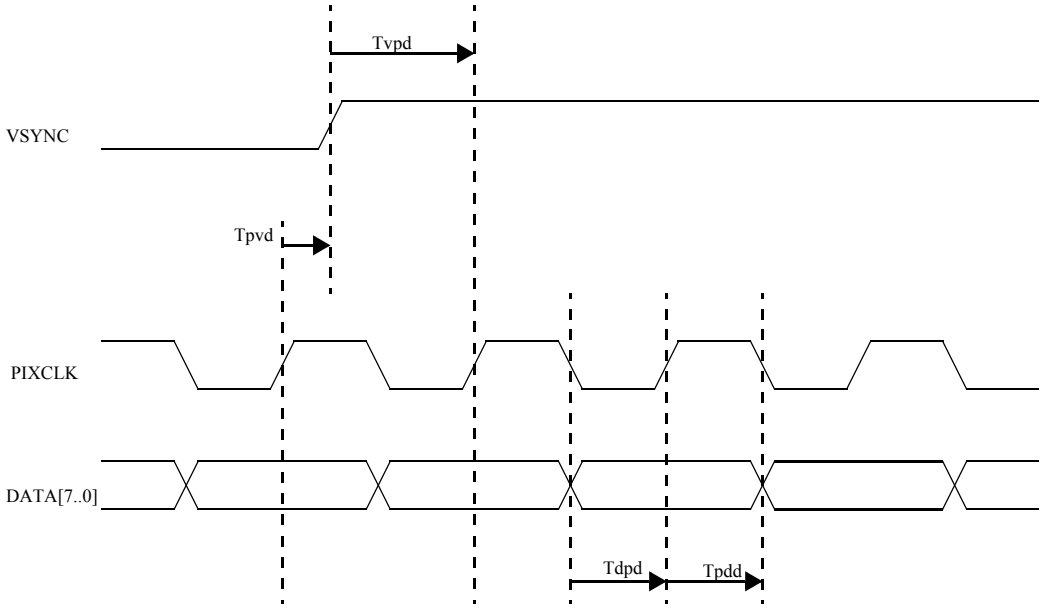

Figure 8.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
PIXCLK Freq		0	-	48	MHz
PIXCLK High Time	Tph	10.42	-	-	ns
PIXCLK Low Time	Tpl	10.42	-	-	ns
Data Valid to PIXCLK High	Tdpd (Setup Time)	3	-	-	ns
PIXCLK High to Data Invalid	Tpdd (Hold Time)	2	-	-	ns
VSYNC Valid to PIXCLK High	Tvpd (Setup Time)	3	-	-	ns
PIXCLK High to VSYNC Invalid	Tpvd (Hold Time)	2	-	-	ns

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4.4 (4) Non-Gated Clock Mode, Pixel Clock Falling-Edge Active

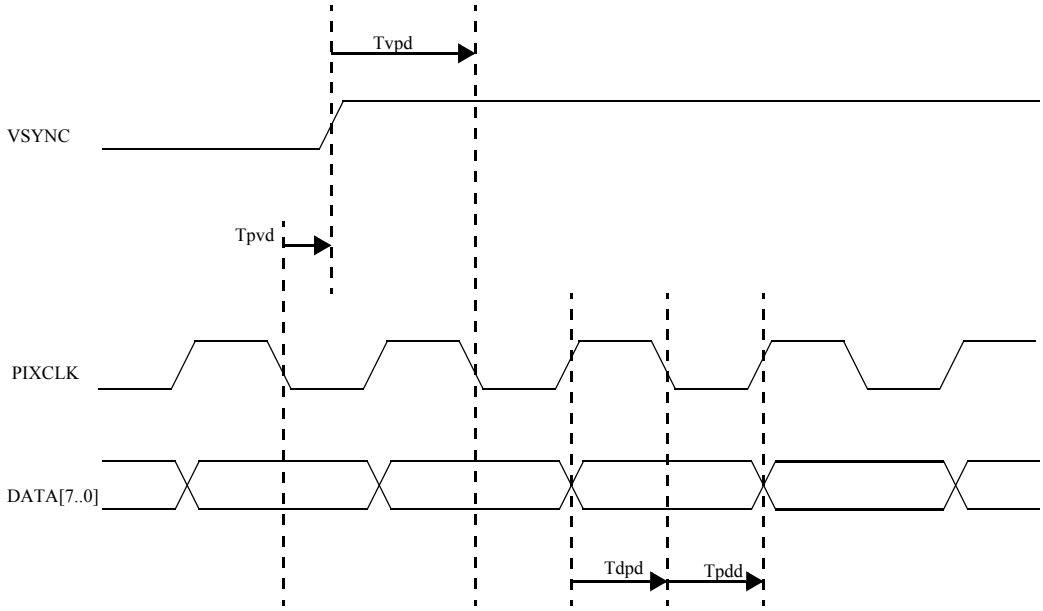

Figure 9.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit
PIXCLK Freq		0	-	48	MHz
PIXCLK High Time	Tph	10.42	-	-	ns
PIXCLK Low Time	Tpl	10.42	-	-	ns
Data Valid to PIXCLK Low	Tdpd (Setup Time)	3	-	-	ns
PIXCLK Low to Data Invalid	Tpdd (Hold Time)	2	-	-	ns
VSYNC Valid to PIXCLK Low	Tvpd (Setup Time)	3	-	-	ns
PIXCLK Low to VSYNC Invalid	Tpvd (Hold Time)	2	-	-	ns

5 Statistics

Statistics block computes the Sum of each color component and the Sum Of Absolute Difference (SOAD) of green. It works on Bayer pattern only.

Sum of color reflects the exposure time; in general longer exposure time results in higher pixel values. The sums are usually used in the Auto Exposure Control Loop (AEC). On the other hand Sum of Absolute Difference reflects the sharpness of focus. When the picture is in focus, the value of SOAD should reach the maximum. It is used in the Auto Focus Control loop in case the optics is mechanically movable by means of stepping motor.

Statistics is done in a frame-by-frame manner and is initiated by a rising edge on the SOF. This is fixed by design and cannot be changed. The settings of the SOF_POL bit in the CSI control register 1 has no effect to the statistics block.

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5.1 Live Veiw Resolution Mode (LVRM)

The image is divided into square blocks, according to the choice made on the Live View Resolution Mode (LVRM). Statistic data is generated per each block. The output includes 4 16-bit numbers:

Sum of Red
Sum of Blue
Sume of Green
SOAD of Green

Each of the sum and SOAD data are pre-divided by a divisor.

For DRM = 0, divisor = 4.
For DRM = 1, divisor = 2.

Data is packed into 32-bit words before putting into the STAT FIFO. The endian is selectable by user setting BIG_ENDIAN bit in the CSI control register 1.

5.2 Skip Count Enable (SCE)

In order to support a variety of image resolutions, the LVRM can be set together with a line skipping scheme, either in horizontal (HSC) or vertical (VSC) direction. Skipping can be enabled or disabled. When it is enabled, lines between adjacent blocks are ignored, virtually supporting an image size larger than that of the current LVRM.

Taken 640x480 (VGA size) as an example, the method to calculate HSC & VSC is:

1. Choose the smaller closest LVRM

   => LVRM Mode 0 = 512 x 384 (8 x 6 blocks)
2. Divide image height & width by the no. of statistical blocks

   => Horizontal : 640 / 8 = 80

   => Vertical : 480 / 6 = 80
3. Subtract the statistic block size from the above

   => Horizontal : 80 - 64 = 16

   => Vertical : 80 - 64 = 16
4. Offset the above numbers by 1 giving the HSC & VSC

   => HSC : 16 - 1 = 15

   => VSC : 16 - 1 = 15

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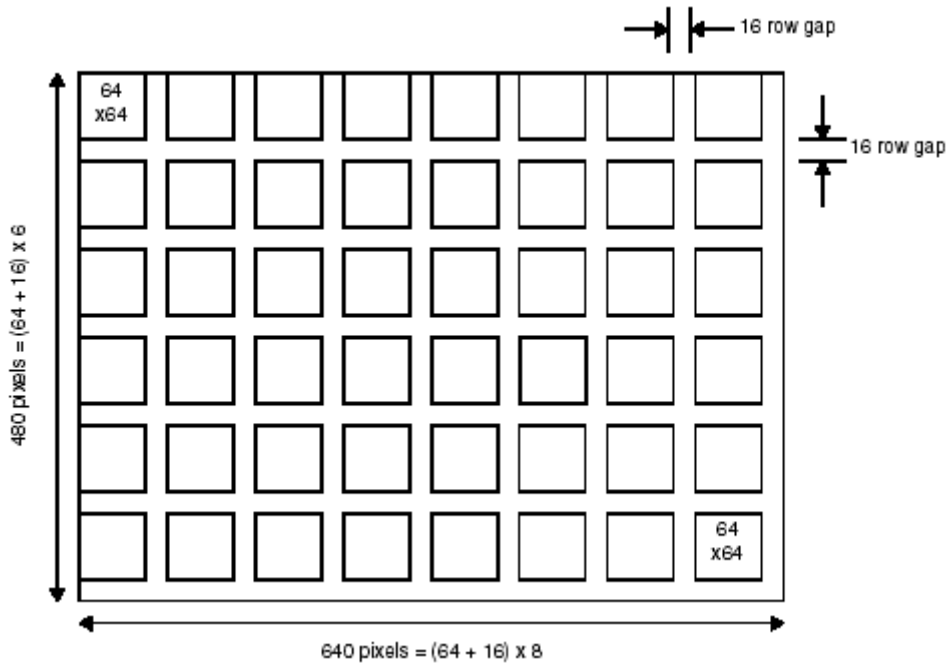

Figure 10.

5.3 Double Resolution Mode (DRM)

Double Resolution Mode allows the vertical resolution of image to be enhanced, without increasing the complexity of hardware. User may find this useful when they fine tune the algorithm of white balance.

In the DRM mode, The number of rows of blocks are doubled, generating twice amount of statistical data.

However for each block, the height, and so the number of pixels, has been reduced to half, resulting in the magnitude of statistical data being halved. This is already compensated by internal logic. So for the same input pattern, suppose every pixel having the same value, enabling / disabling DRM mode would not affect the magnitude of the statistical data in FIFO.

In case line skipping is enabled, the calculation for HSC & VSC would require a little change. Take the case of VGA as an example:

1. Choose the smaller closest LVRM

   => LVRM Mode 0 = 512 x 384 (8 x 6 blocks, each 64 x 64 pixels)
2. Enable DRM

   => 8 x 12 blocks (Each 64 x 32 pixels)
3. Divide image height & width by the no. of statistical blocks

   => Horizontal : 640 / 8 = 80

   => Vertical : 480 / 12 = 80
4. Subtract the statistic block size from the above

   => Horizontal : 80 - 64 = 16

   => Vertical : 40 - 32 = 8
5. Offset the above numbers by 1 giving the HSC & VSC

   => HSC : 16 - 1 = 15

   => VSC : 8 - 1 = 7

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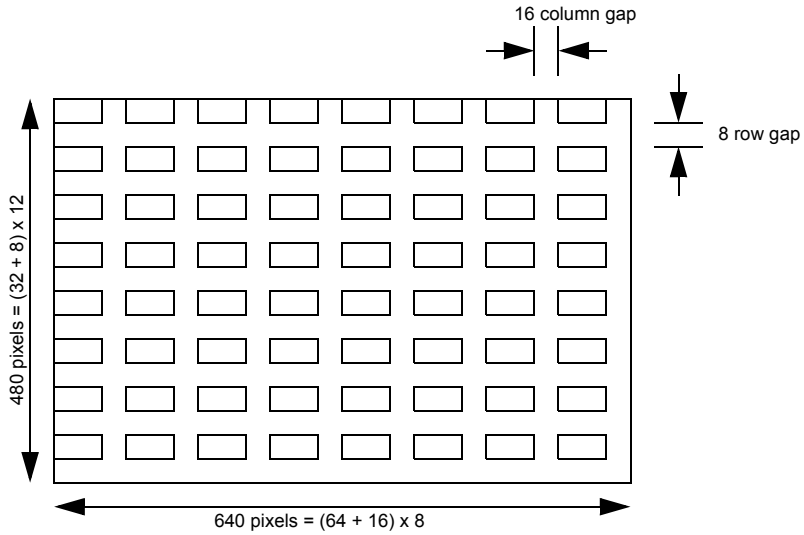

Figure 11.

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