Freescale Semiconductor
Application Note

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i.MX Supplemental Information for LCD Interfacing

MC9328MX1 & MC9328MXL

This application note provides supplementary information to the *MC9328MX1 and MC9328MXL (i.MX) Integrated Portable System Processor Reference Manuals* (order numbers: MC9328MX1RM/D and MC9328MXL/D), LCD Controller chapters:

- Features and supported panel types
- LCD pins and signals
- LCD interface clock settings
- Timings
- Interfacing to Sharp TFT panels
- Other considerations

For the latest errata and addenda to the i.MX reference manual please reference the web site: www.freescale.com/semiconductors.

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1 Features and Supported Panels

Table 1 on page 2 summarizes the panels supported by the i.MX processor with the ARM® core based system.

Table 1. i.MX Processor Panel Support

Panel Type	BPP	Panel Interface (bits)	Number of Levels	Max. Panel Size (pixels)	Palette Ram Usage
Mono chrome	1	1,2,4,8	2 level black and white	640 x 480* 640 x 480**	1. Palette RAM is not used.
	2	1,2,4,8	4 gray scale levels	640 x 480* 640 x 480**	1. Palette RAM is not used. 2. Black is one shade, white is one shade, two remaining shades are programmable in LGPMR LCD Gray Palette Mapping Register.
	4	1,2,4,8	16 gray scale levels	640 x 480* 320 x 240 or 240 x 320**	1. Palette RAM is used. 2. 16 four-bit values are programmed into the first 16 entries of the palette RAM.
CSTN	4	8	16 color levels	320 x 240 or 240 x 320**	1. Palette RAM is used. 2. 16 colors can be selected out of a palette of 4096 different colors. 3. 16 twelve-bit values are programmed into first 16 entries of the palette RAM.
	8	8	256 color levels	320 x 240 or 240 x 320**	1. Palette RAM is used. 2. 256 colors can be selected out of a palette of 4096 different colors. 3. 256 twelve-bit values are programmed into the palette RAM.
	12	8	4096 color levels	320 x 240 or 240 x 320**	1. Palette RAM is not used.
TFT	4	12	16 color levels	640 x 480* 320 x 240 or 240 x 320**	1. Palette RAM is used. 2. 16 colors can be selected out of a palette of 4096 different colors. 3. 16 twelve-bit values are programmed into first 16 entries of the palette RAM.
	8	12	256 color levels	640 x 480* 320 x 240 or 240 x 320**	1. Palette RAM is used. 2. 256 colors can be selected out of a palette of 4096 different colors. 3. 256 twelve-bit values are programmed into the palette RAM.
	12	12	4096 color levels	640 x 480* 240 x 160 or 160 x 240**	1. Palette RAM is not used.
	16	16	65,536 color levels	640 x 480* 240 x 160 or 160 x 240**	1. Palette RAM is not used.

Note: * Using external memory, actual panel size depends on system bandwidth use. Also take into consideration erratums 7 and 11 since the usage of higher resolution panels augments the chance of incidence of these erratums

Note: ** Using internal memory, eSRAM

Note: *** BPP = Bits Per Pixel

2 LCDC Pins and Signals

The i.MX interface pins for the LCDC are 3.0V +/- 10% capable. Refer to the i.MX reference manual and your panel's specifications regarding electrical compatibility with the i.MX processor's interface pins. The Figure 1 shows the i.MX processor's LCD pins and signal name assignments.

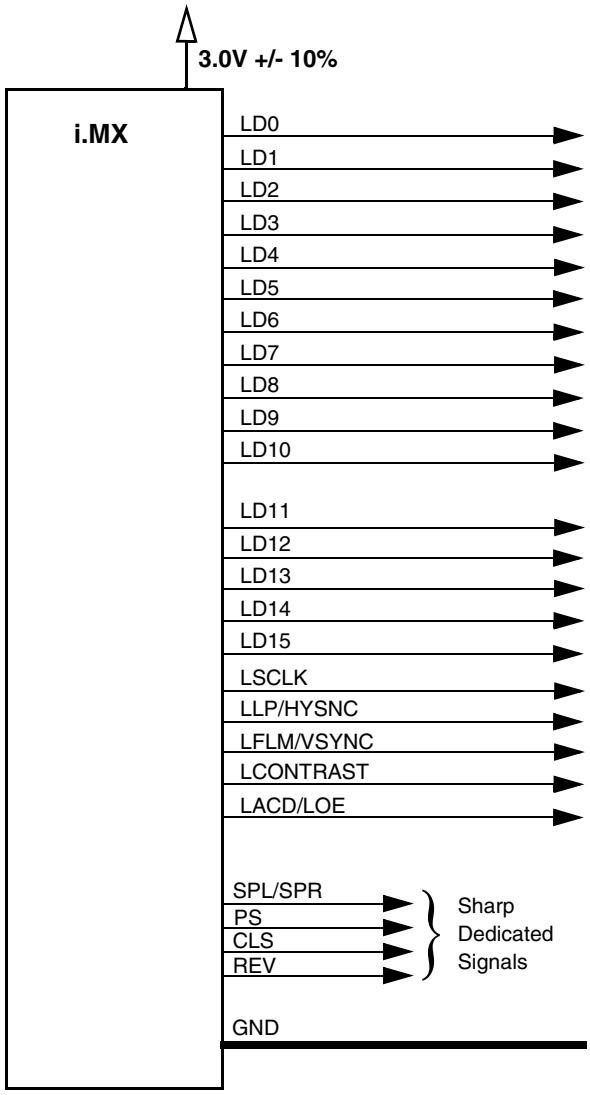

Figure 1. LCDC Pins and Signals

3 LCD Interface Clock Settings

The frequency setting of the interface clock, LSCLK, is determined by the panel specifications. To avoid flicker on the screen set LSCLK to be within the panel specifications. Use an oscilloscope to probe LSCLK to ensure that the clock frequency is set correctly. If flicker problems occur, visually inspect the interface clock by probing even when the clock settings have been programmed correctly.

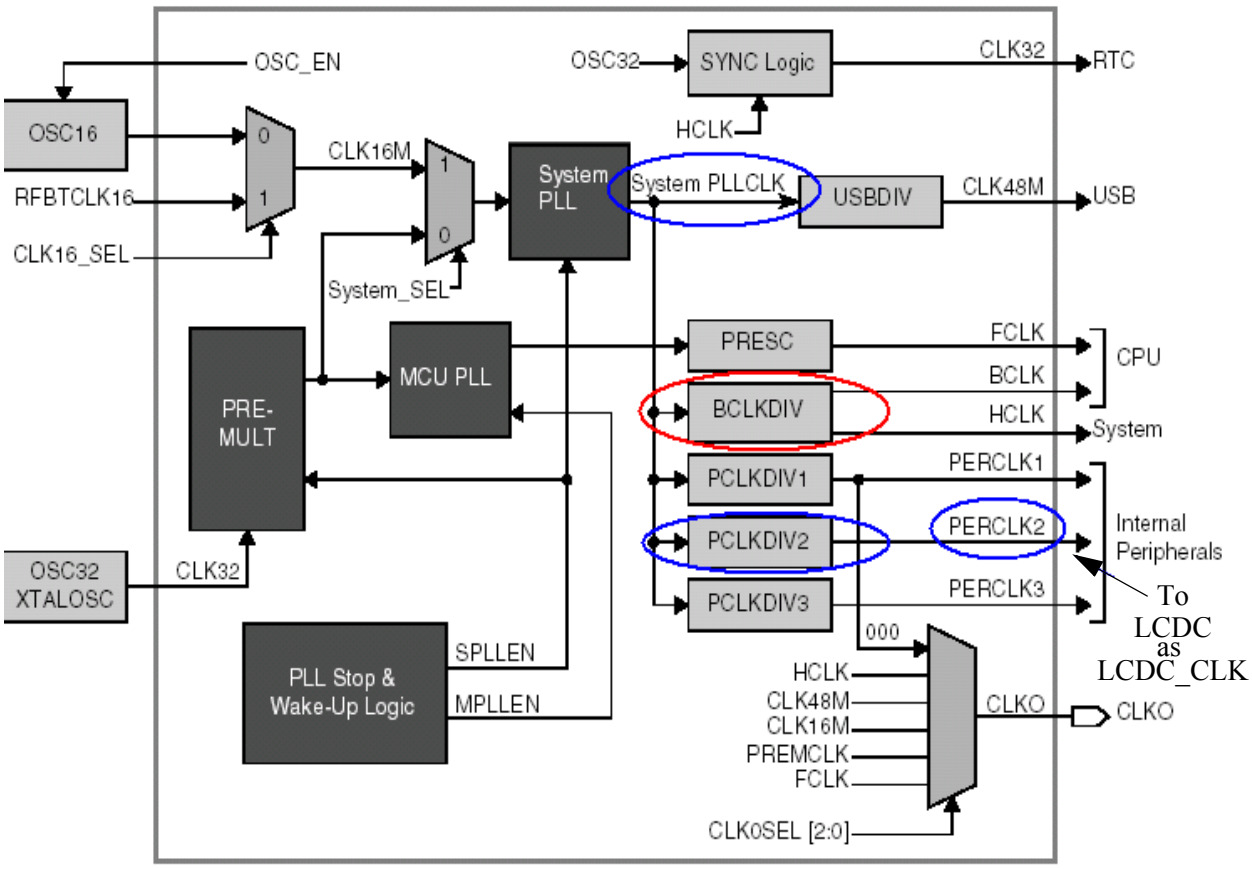

Figure 2. i.MX Clock Controller Module

Figure 2 shows that the LCD controller's clock input is PERCLK2. PERCLK2, with respect to the LCDC, is known as LCDC_CLK. Therefore, LCDC_CLK and HCLK are derived from the same clock source, the output of the System PLL (System PLLCLK).

WARNING:

HCLK and LCDC_CLK must follow the following relationship for the LCDC to work properly:

LCDC_CLK = PERCLK2 = (System PLLCLK) / (PCLKDIV2)

HCLK = (System PLLCLK) / (BCLKDIV)

However, when BCLKDIV = 1 (for example BCLK_DIV setting = 0x0) then HCLK = (System PLLCLK). In this case the divider PCLKDIV2 can be any value.

Also, when BCLK_DIV = 2 (for example BCLK_DIV setting = 0x1) then HCLK = (System PLLCLK) / 2. In this case, the divider PCLK_DIV2 must be 3, 7, or 15 and so on.

This method ensures the rising clock edge of LCDC_CLK is synchronized with the rising edge of HCLK, otherwise timing problems occur. Consequently, the output of the LCDC is unpredictable.

Please refer to the i.MX reference manual for PCLKDIV2 and BCLKDIV divider settings and programming.

4 Timing

The LCDC supports both non-TFT passive matrix panels as well as TFT active matrix panels. Timing for both panel types are discussed in this section. Figure 3 and Table 1 depict the LSCLK-to-display data (LD) relationship.

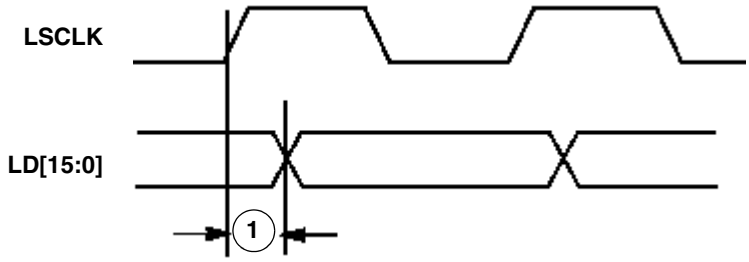

Figure 3. LSCLK to LD Timing Diagram

Table 2. LSCLK to LD Timing Parameters

Number	Characteristic	3.0 V +/- 10%		Unit
		Minimum	Maximum	
1	SCLK to LD valid	–	3	ns

4.1 Non-TFT Panel Timing (Passive Matrix)

The LCDC supports non-TFT panel interfaces for passive matrix LCD panels.

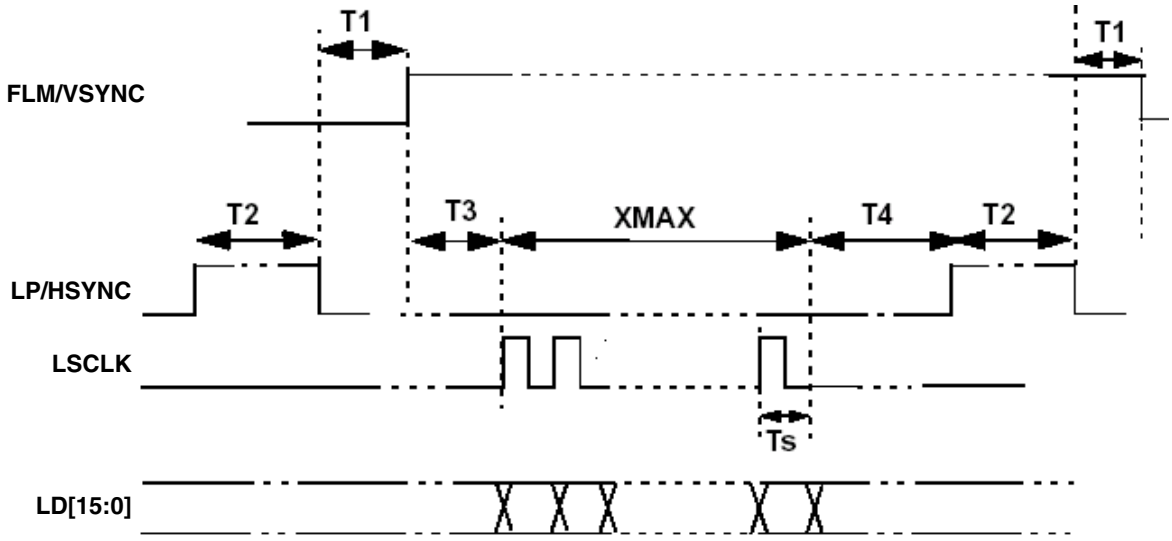

Figure 4. Non-TFT Panel Timing Waveform

Table 3. Non-TFT Panel Timing

Symbol	Parameter	Allowed Register Minimum Value	Actual Value	Unit
T1	HSYNC to VSYNC delay	0	HWAIT2+2	Tpix
T2	HSYNC pulse width	0	HWIDTH+1	Tpix
T3	VSYNC to SCLK	–	0≤ T3≤Ts	
T4	SCLK to HSYN	0	HWAIT1+1	Tpix

- VSYNC, HSYNC, and LSCLK can be programmed as active high or active low. In the timing diagram above, all 3 signals are active high.
- Ts is the shift clock period.
- Ts = Tpix * (panel data bus width).
- Tpix is the Pixel Clock Period (LSCLK) which equals $\frac{1}{8 \times (\mathrm{PCD} + 1)} \times \mathrm{LCDC\_CLK}$.
- To calculate the maximum frequency required for the LSCLK to operate on a passive LCD panel so that the LD output is correct, use the following formulas:
  LSCLK (12 bpp) < 1/9 HCLK
  LSCLK (8 bpp/4 bpp) < 1/15 HCLK

4.2 TFT Panel Timing

The LCDC supports TFT panel interfaces for active matrix LCD panels. The i.MX processor supports two types of TFT panels: the Sharp TFT panels that require the special timing signals SPL/SPR, CLS, PS, and REV and standard TFT interface panels. This sections discusses the latter type of panels.

4.2.1 TFT Timing for Display Region

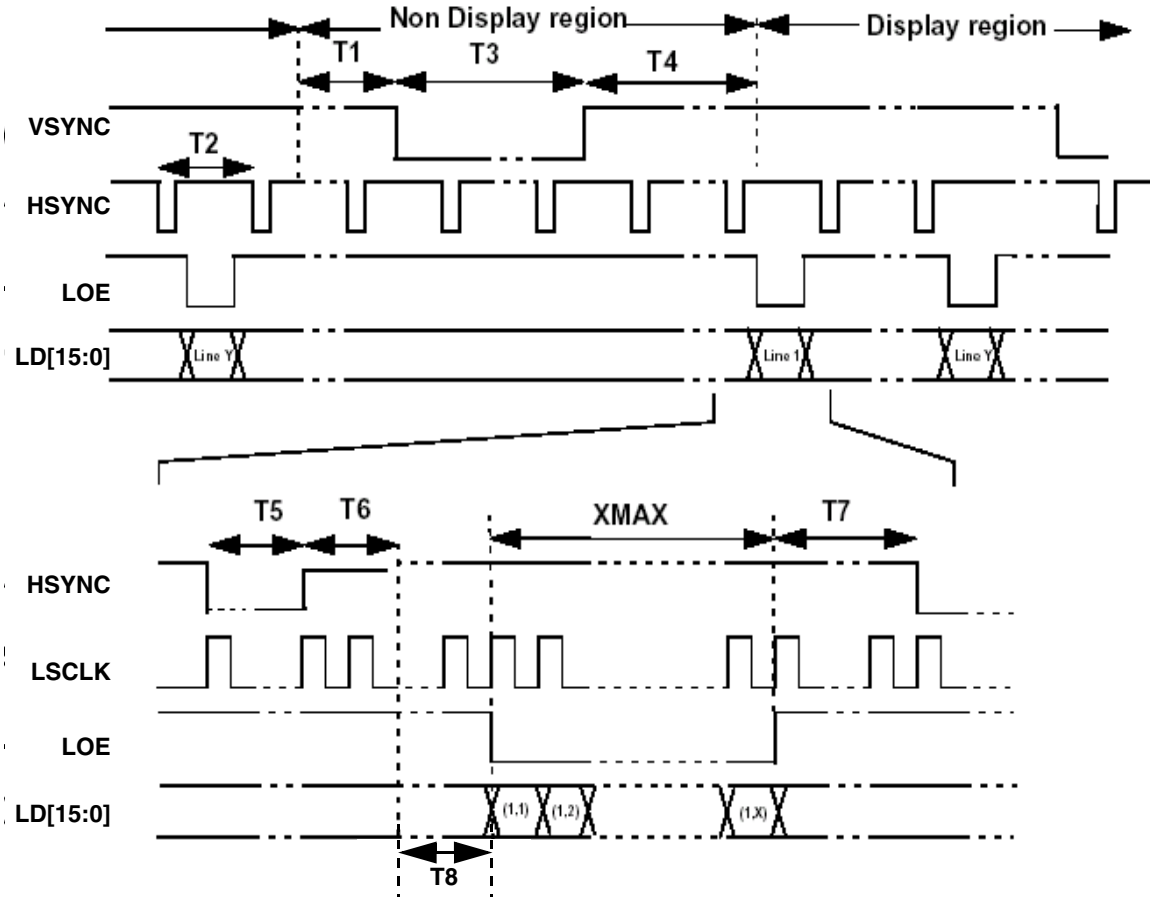

Figure 5. TFT Panel Timing Waveform for Display Region

Table 4. TFT Panel Timing for Display Region

Symbol	Parameter	Allowed Register Minimum Value	Actual Value	Unit
T1	Idle HSYNC period between last line and beginning of VSYNC	0	VWAIT1	T2
T2	HSYNC period	–	XMAX+T5+T6+T7+T8	Ts
T3	VSYNC pulse width	1	VWIDTH	T2
T4	Idle HSYNC period between End of VSYNC to first line	0	VWAIT2	T2
T5	HSYNC pulse width	0	HWIDTH+1	Ts
T6	End of HSYNC to T8	0	HWAIT2+1	Ts
T7	End of OE to beginning of HSYNC	0	HWAIT1+1	Ts
T8	Dummy idle state (Sharp = 0)	–	2	Ts

Table 4. TFT Panel Timing for Display Region (continued)

Symbol	Parameter	Allowed Register Minimum Value	Actual Value	Unit
T8	Dummy idle state (Sharp = 1)	–	3	Ts

Ts is the LSCLK period which equals LCDC_CLK / (PCD + 1).

- VSYNC, HSYNC and LOE can be programmed as active high or active low. In the above timing diagram, all these 3 signals are active low.
- The polarity of LSCLK and LD[15:0] can also be programmed.
- By default, LSCLK is idle when LOE is non-active.
- If register bit sclk_idle equals 1, LSCLK is active when LOE is non-active, excluding the HYSNC idle period and dummy state, for example T5, T6, T7, and T8.
- If register bit sclk_sel equals 1, LSCLK is always active.
- XMAX is defined in unit of pixel.
- Formula for period of VSYNC = T2 * YMAX + T1+T3+T4

4.2.2 TFT Timing for Non-Display Region

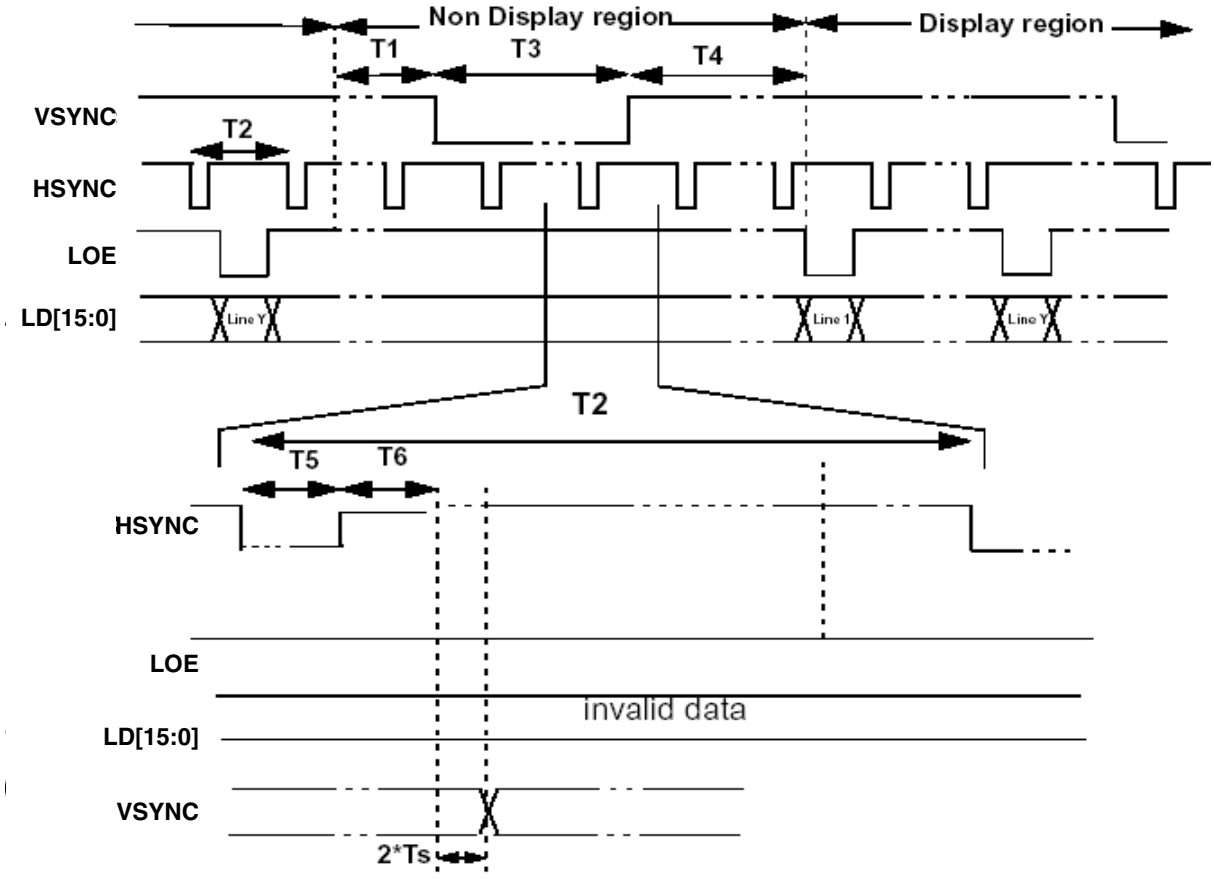

Figure 6. TFT Panel Timing Waveform for Non-Display Region

Within the non-display period, the position of VSYNC relative to the HSYNC is the same in each HSYNC period. This applies for both positive and negative going edge of VSYNC.

5 Interfacing to Sharp TFT Panels

The i.MX processor's LCDC can directly interface with Sharp HR-TFT panels that require Sharp dedicated signals. Figure 7 shows how to connect the LCDC interface signals to a 18 bpp TFT panel. The two LSBs of the blue (B0) and red (R0) component are tied to B1 and R1, respectively. The diagram shows a panel that does not require Sharp dedicated signals, therefore, they are shown not connected (nc).

5.1 Connections and Signals

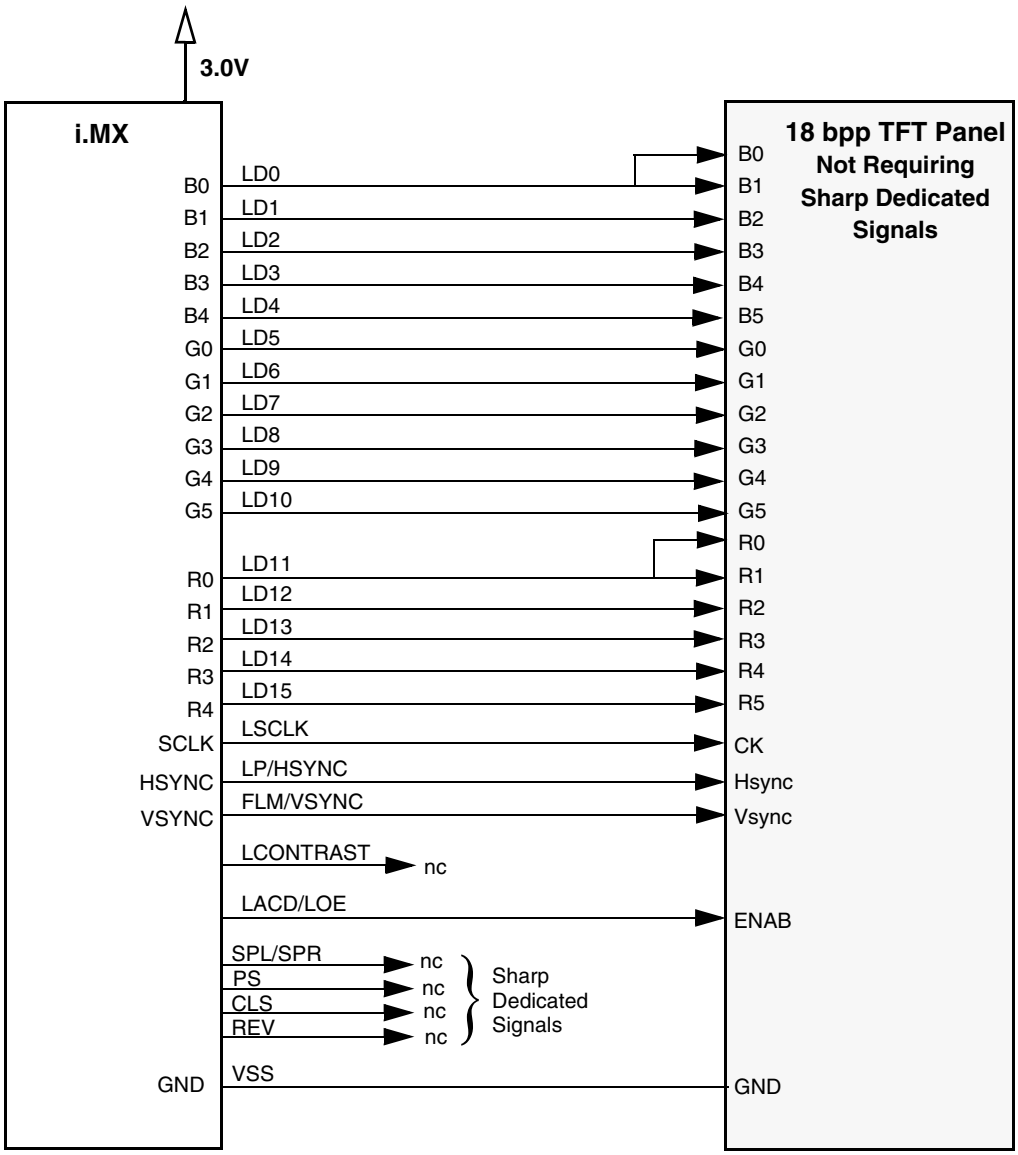

Figure 7. TFT Panel Interface Not Requiring Sharp Dedicated Signals

If the panel illustrated in Figure 7 required Sharp dedicated signals—that is, it was a Sharp panel and the timing ASIC for the dedicated signals was not provided—the i.MX processor could be used to directly drive the panel by making direct connections to those signals. The four signals dedicated to Sharp panels are identified in Table 5 on page 10.

Table 5. Sharp Dedicated Signals

Signal Name	Description
SPL/SPR	Sampling Start Signal
CLS[1]	Clock Signal for Gate Driver
PS	Power Save Signal
REV[1]	Reverse Control

[1]Both the rising and falling edge of CLS and transition edge of REV are programmable.

5.2 Sharp Dedicated Signal Timing

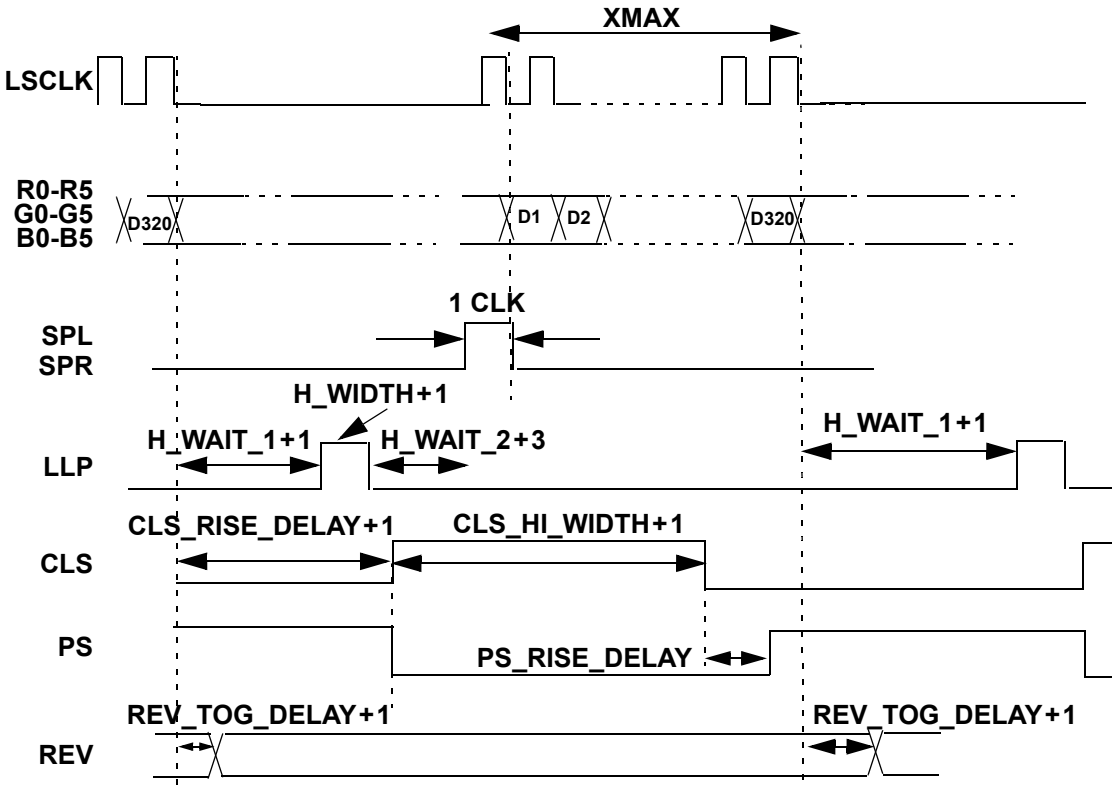

Figure 8. i.MX Version 2.0 Sharp Dedicated Signal Timing Waveform

Additional information regarding Figure 8 follows:

- Falling edge of PS aligns with rising edge of CLS.
- Delay of rising edge of PS is programmed by PS_RISE_DELAY.
- SPL/SPR pulse width is fixed and aligned to the first data of the line.
- REV toggles every LLP period.
- CLS_HI_WIDTH is programmable, PWMR [24:16].

6 Other Considerations

6.1 LCDC DMA Setting

For SDRAM access, a fixed burst length of 8 is preferred.

Table 6. Fixed Burst Length Settings

Item	DMA Register Setting
Fixed burst length	1
High mark	8
Low mark	4

For a heavily loaded bus and SDRAM access, a dynamic burst length is recommended.

Table 7. Dynamic Burst Length Settings

Item	DMA Register Setting
Fixed burst length	0
High mark	3
Low mark	8

6.2 Bandwidth and Detection of LCDC Under-Run

The LCDC output data rate is determined by:

- bit per pixel
- panel size

Refresh Rate—The refresh rate is determined by the panel specification. For a TFT panel typical refresh rates are around 60 frames/sec.

For example:

- 240 × 320 TFT panel 16 bpp color
- refresh rate at 60 Frame/sec.

The required data output rate:

$240 \times 320 \times 16 \times 60 = 73$ M bit/sec (approximately)

If HCLK (DMA CLOCK) is running at 96 MHz, then the maximum data rate is:

32×96 M = 3072 M bit /sec.

Therefore, the theoretic bandwidth used by the LCDC = 73 / 3072 = 0.023

In a customer's application data under-run may occur due to heavy bus loading as well as a priority issue with the memory controller. To detect a data under-run event, the user can perform the following:

- Read the Under-Run bit in the LCDC status register to see if it is set.
- Monitor the period of HSYNC/VSYNC to see if it is changing intermittently.

When an Under-Run occurs, the data output will be incorrect. When normal data service—that is, no more Under-Run, is restored the LCDC outputs data correctly. However, the LCD panel is a sequential device with no error checking protocol. Even though the LCDC returns to correct operation, the LCD panel will return to normal operation only after a VSYNC signal. This is to fully synchronize the data between LCDC and the LCD panel. Under-run errors will be more prone to occur on higher resolution panels such as VGA (640x480). Tests on the overall system must take place to make sure the usage of system bus does not trigger under-run errors.

6.3 Example Initializations

Code Example 1. Sharp TFT VGA Panel Not Requiring Dedicated Signals

```
comment ### Select CLKO mux to output HCLK(BCLK) ###
setmem 0x21B000 0x2F00AC03, 32

comment ### Change BCLK (CPUCLK) to 16MHz
comment setmem 0x21B000 0x2F009403, 32

comment ### Change BCLK (CPUCLK) to 24MHz
comment setmem 0x21B000 0x2F008C03, 32

comment ### Change BCLK (CPUCLK) to 32MHz
comment setmem 0x21B000 0x2F008803, 32

comment ### Change BCLK (CPUCLK) to 48MHz
comment setmem 0x21B000 0x2F008403, 32

comment ### Change BCLK (CPUCLK) to 96MHz
setmem 0x21B000 0x2F008003, 32

comment ### Change PerCLK2 (LCDCLK) to 96MHz
comment setmem 0x21B020 0x000B000B, 32

comment ### Change PerCLK2 (LCDCLK) to 48MHz
setmem 0x21B020 0x000B001B, 32

comment ### Change PerCLK2 (LCDCLK) to 32MHz
comment setmem 0x21B020 0x000B002B, 32

comment ### Change PerCLK2 (LCDCLK) to 16MHz
comment setmem 0x21B020 0x000B005B, 32

comment ### Change PerCLK2 (LCDCLK) to 8MHz
comment setmem 0x21B020 0x000B00BB, 32

comment ### CS0 - boot flash, 32 wait states, 8-bit ###
setmem 0x220000 0x00002000, 32
setmem 0x220004 0x11110301, 32

comment ### CS1 - SRAM, wait states, 32-bit ###
setmem 0x220008 0x00000300, 32
setmem 0x22000C 0x11110601, 32

comment ### CS4 - External UART, 10 wait states, 8-bit ###
setmem 0x220020 0x00000A00, 32
setmem 0x220024 0x11110301, 32


comment ##########################################
comment   INIT FILE FOR SHARP 640X480 LCD DISPLAY
comment ##########################################

comment LCD buffer point to external SRAM
setmem 0x00205000 0x12000000, 32

comment LCD buffer point to eSRAM
comment setmem 0x00205000 0x00300000, 32

comment set LCD display size 640x480
setmem 0x00205004 0x028001E0, 32
```

```
comment vpwC480(dec) for 8bpp  40 for 4bpp

comment set vpw to 640/2=320 => 0x140
setmem 0x00205008 0x00000140, 32

comment set cursor position & attributes
setmem 0x0020500C 0x40010001, 32
setmem 0x00205010 0x1F1F0000, 32
setmem 0x00205014 0x0000F800, 32

comment 16 bpp , tft , color,  div by 2
setmem 0x00205018 0xF8E00081, 32

comment h_width, h_wait1, h_wait2
setmem 0x0020501C 0x04001066, 32

comment v_width, v_wait1, v_wait2
setmem 0x00205020 0x04000022, 32

comment panning offset
setmem 0x00205034 0x00000000, 32

comment ##########################
comment   IO PORT INIT FOR LCD
comment   config PC16 to output port for LCD ON
comment   config PD to functional use for LCD signals
comment ########################################

comment PORT D GIUS
comment clear PORT D for LCD signal
setmem 0x0021C320 0x00000000, 32

comment PORT D GPR
setmem 0x0021C338 0x00000000, 32

comment PORT C GIUS
setmem 0x0021C220 0x00010000, 32

comment PORT C OCR2
setmem 0x0021C208 0x00000003, 32

comment PORT C DDIR
setmem 0x0021C200 0x00010000, 32

comment PORT C GPR
setmem 0x0021C238 0x00010000, 32

comment PORT C DR (data register)
comment set PC16 will turn off LCD
setmem 0x0021C21C 0x00010000, 32


comment ############
comment   LCD ON
comment ############

comment PORT C DR (data register)
comment set PC16 will turn off LCD
setmem 0x0021C21C 0x00010000, 32

comment LCD enabled
setmem 0x00205034 0x0F000002, 32
```

NOTE:

Code Example 2 provides a way to configure the internal clocks of the i.MX chip, however depending on the application and system requirements the clocks could be different.

Code Example 2. Sharp 320x480 TFT Requiring Dedicated Signals

```
comment ### Select CLKO mux to output HCLK(BCLK) ###
setmem 0x21B000 0x2F00AC03, 32

comment ### Change BCLK (CPUCLK) to 16MHz
comment setmem 0x21B000 0x2F009403, 32

comment ### Change BCLK (CPUCLK) to 24MHz
comment setmem 0x21B000 0x2F008C03, 32

comment ### Change BCLK (CPUCLK) to 32MHz
comment setmem 0x21B000 0x2F008803, 32

comment ### Change BCLK (CPUCLK) to 48MHz
comment setmem 0x21B000 0x2F008403, 32

comment ### Change BCLK (CPUCLK) to 96MHz
setmem 0x21B000 0x2F008003, 32

comment ### Change PerCLK2 (LCDCLK) to 96MHz
comment setmem 0x21B020 0x000B000B, 32

comment ### Change PerCLK2 (LCDCLK) to 48MHz
comment setmem 0x21B020 0x000B001B, 32

comment ### Change PerCLK2 (LCDCLK) to 32MHz
setmem 0x21B020 0x000B002B, 32

comment ### Change PerCLK2 (LCDCLK) to 16MHz
comment setmem 0x21B020 0x000B005B, 32

comment ### Change PerCLK2 (LCDCLK) to 8MHz
comment setmem 0x21B020 0x000B00BB, 32

comment ### CS0 - boot flash, 32 wait states, 8-bit ###
setmem 0x220000 0x00002000, 32
setmem 0x220004 0x11110301, 32

comment ### CS1 - SRAM, 10 wait states, 32-bit ###
setmem 0x220008 0x00000A00, 32
setmem 0x22000C 0x11110601, 32

comment ### CS4 - External UART, 10 wait states, 8-bit ###
setmem 0x220020 0x00000A00, 32
setmem 0x220024 0x11110301, 32

comment ##########################################
comment   INIT FILE FOR SHARP 320X480 LCD DISPLAY
comment ##########################################

comment LCD buffer point to external SRAM
setmem 0x00205000 0x12000000, 32

comment LCD buffer point to eSRAM
comment setmem 0x00205000 0x00300000, 32

comment set XMAX to 336 (0x150), YMAX to 480 (0x1E0)
setmem 0x00205004 0x015001E0, 32

comment   vpw=336/32=168 (0xA8) word where word = 32 bit and 16bpp
setmem 0x00205008 0x000000A8, 32
setmem 0x0020500C 0x40050001, 32
setmem 0x00205010 0x1F1F0000, 32
```

```
setmem 0x00205014 0x0000f800, 32

comment 16 bp , tft ,color, pos edge clock pol, LLP active high, LFLM active low
setmem 0x00205018 0xF8040042, 32

comment Sharp Configuration 1 Register
setmem 0x00205028 0x00090300, 32

comment hsyn width = 2 CLK  hsyn_wait 1 = 8 CLK (0x7) hsyn_wait2 = 4 CLK (0x1)
setmem 0x0020501C 0x4000701, 32

comment vsyn width = 2 lines vsyn_wait 1 = 7 lines (0x7)  vsyn_wait2 = 6 lines (0x6)
setmem 0x00205020 0x08000706, 32
comment setmem 0x00205034 0x00000000, 32

comment #########################
comment   IO PORT INIT FOR LCD
comment   config PC16 to output port for LCD ON
comment   config PD to functional use for LCD signals
comment ########################################

comment PORT D GIUS
comment clear PORT D for LCD signal
setmem 0x0021C320 0x00000000, 32

comment PORT D GPR
setmem 0x0021C338 0x00000000, 32

comment PORT C GIUS
setmem 0x0021C220 0x00010000, 32

comment PORT C OCR2
setmem 0x0021C208 0x00000003, 32

comment PORT C DDIR
setmem 0x0021C200 0x00010000, 32

comment PORT C GPR
setmem 0x0021C238 0x00010000, 32

comment PORT C DR (data register)
comment set PC16 will turn off LCD
setmem 0x0021C21C 0x00010000, 32

comment ############
comment   LCD ON
comment ############

comment PORT C DR (data register)
comment set PC16 will turn off LCD
setmem 0x0021C21C 0x00010000, 32

comment set SPL/SPR to CLS delay 316 clk (256 + 0x21)
setmem 0x0020502C 0x00A9033C, 32

comment Enable the LCD display
setmem 0x00205034 0x0F000002, 32
```

6.4 Testing the Display

The application note, *MC9328MX1 Reference Design for High Resolution Software Development*, (order number AN2309/D) provides details to test the display and create a proper test image (See Section 3.4).

7 Revision History

The changes from Revision 1 to revision 1.1 of this document follows:

- Updated URL from Motorola to Freescale Semiconductor.

NOTES

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