CY2XP31

312.5 MHz LVPECL Clock Generator

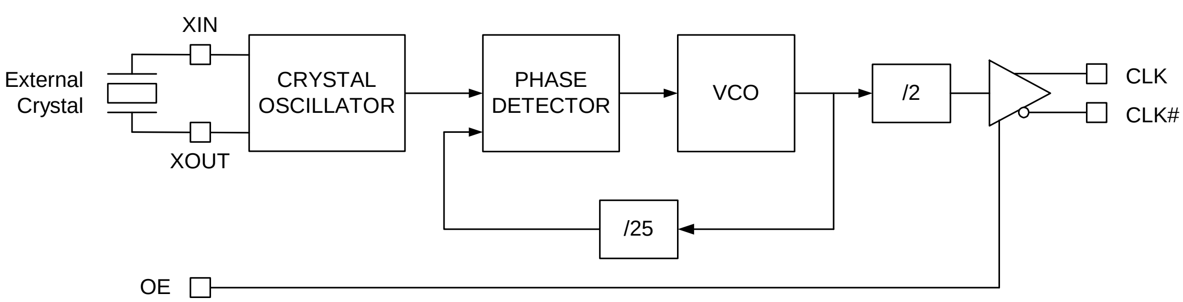
Features

- One LVPECL output pair
- Output frequency: 312.5 MHz
- External crystal frequency: 25 MHz
- Low RMS phase jitter at 312.5 MHz, using 25 MHz crystal (1.875 MHz to 20 MHz): 0.3 ps (typical)
- Pb-free 8-Pin TSSOP package
- Supply voltage: 3.3 V or 2.5 V
- Commercial and industrial temperature ranges

Functional Description

The CY2XP31 is a PLL (Phase Locked Loop) based high performance clock generator. It is optimized to generate 10 Gb Ethernet, SONET, and other high performance clock frequencies. It also produces an output frequency that is 12.5 times the crystal frequency. It uses Cypress's low noise VCO technology to achieve less than 1 ps typical RMS phase jitter, which meets both 10 Gb Ethernet and SONET jitter requirements. The CY2XP31 has a crystal oscillator interface input and one LVPECL output pair.

Logic Block Diagram



Pinouts

Figure 1. Pin Diagram – 8-Pin TSSOP

Table 1. Pin Definition – 8-Pin TSSOP

Pin Number	Pin Name	I/O Type	Description
1, 8	VDD	Power	3.3 V or 2.5 V power supply. All supply current flows through pin 1
2	VSS	Power	Ground
3, 4	XOUT, XIN	XTAL Output and Input	Parallel resonant crystal interface
5	OE	CMOS Input	Output enable. When HIGH, the output is enabled. When LOW, the output is high impedance
6,7	CLK#, CLK	LVPECL Output	Differential clock output

Frequency Table

Inputs		Output Frequency (MHz)
Crystal Frequency (MHz)	PLL Multiplier Value	
25	12.5	312.5

Absolute Maximum Conditions

Parameter	Description	Conditions	Min	Max	Unit
V_{DD}	Supply Voltage		–0.5	4.4	V
V_{IN}[1]	Input Voltage, DC	Relative to V_{SS}	–0.5	V_{DD} + 0.5	V
T_S	Temperature, Storage	Non operating	–65	150	°C
T_J	Temperature, Junction		–	135	°C
ESD_{HBM}	ESD Protection, Human Body Model	JEDEC STD 22-A114-B	2000	–	V
UL–94	Flammability Rating	At 1/8 in.	V–0		
Θ_{JA}[2]	Thermal Resistance, Junction to Ambient	0 m/s airflow	100		°C/W
		1 m/s airflow	91		
		2.5 m/s airflow	87		

Operating Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	3.3 V Supply Voltage	3.135	3.465	V
	2.5 V Supply Voltage	2.375	2.625	V
T_A	Ambient Temperature, Commercial	0	70	°C
	Ambient Temperature, Industrial	–40	85	°C
T_{PU}	Power-up time for all V_{DD} to reach minimum specified voltage (ensure power ramps is monotonic)	0.05	500	ms

Notes
1. The voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. Simulated using Apache Sentinel TI software. The board is derived from the JEDEC multilayer standard. It measures 76 x 114 x 1.6 mm and has 4-layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metalization. No vias are included in the model.

DC Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
I_{DD}	Operating Supply Current with Output Unterminated	V_{DD} = 3.465 V, OE = V_{DD}, output unterminated	–	–	125	mA
		V_{DD} = 2.625 V, OE = V_{DD}, output unterminated	–	–	120	mA
I_{DDT}	Operating Supply Current with Output Terminated	V_{DD} = 3.465 V, OE = V_{DD}, output terminated	–	–	150	mA
		V_{DD} = 2.625 V, OE = V_{DD}, output terminated	–	–	145	mA
V_{OH}	LVPECL Output High Voltage	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 50Ω to V_{DD} – 2.0 V	V_{DD} –1.15	–	V_{DD} –0.75	V
V_{OL}	LVPECL Output Low Voltage	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 50Ω to V_{DD} – 2.0 V	V_{DD} –2.0	–	V_{DD} –1.625	V
V_{OD1}	LVPECL Peak-to-Peak Output Voltage Swing	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 50Ω to V_{DD} – 2.0 V	600	–	1000	mV
V_{OD2}	LVPECL Output Voltage Swing (V_{OH} - V_{OL})	V_{DD} = 2.5 V, R_{TERM} = 50Ω to V_{DD} – 1.5 V	500	–	1000	mV
V_{OCM}	LVPECL Output Common Mode Voltage (V_{OH} + V_{OL})/2	V_{DD} = 2.5 V, R_{TERM} = 50Ω to V_{DD} – 1.5 V	1.2	–	–	V
I_{OZ}	LVPECL Output Leakage Current	Output off, OE = V_{SS}	–35	–	35	µA
V_{IH}	Input High Voltage, OE Pin		0.7*V_{DD}	–	V_{DD}+0.3	V
V_{IL}	Input Low Voltage, OE Pin		–0.3	–	0.3*V_{DD}	V
I_{IH}	Input High Current, OE Pin	OE = V_{DD}	–	–	115	µA
I_{IL}	Input Low Current, OE Pin	OE = V_{SS}	–50	–	–	µA
C_{IN}[5]	Input Capacitance, OE Pin		–	15	–	pF
C_{INX}[5]	Pin Capacitance, XIN & XOUT		–	4.5	–	pF

AC Electrical Characteristics[5]

Parameter	Description	Conditions	Min	Typ	Max	Unit
F_{OUT}	Output Frequency		–	312.5	–	MHz
T_R, T_F[3]	Output Rise or Fall Time	20% to 80% of full output swing	–	0.5	1.0	ns
$T_{Jitter(\phi)}$[6]	RMS Phase Jitter (Random)	312.5 MHz, (1.875 to 20 MHz)	–	0.3	–	ps
T_{DC}[7]	Output Duty Cycle	Measured at zero crossing point	45	–	55	%
T_{OHZ}	Output Disable Time	Time from falling edge on OE to stopped outputs (Asynchronous)	–	–	100	ns
T_{OE}	Output Enable Time	Time from rising edge on OE to outputs at a valid frequency (Asynchronous)	–	–	100	ns
T_{LOCK}	Startup Time	Time for CLK to reach valid frequency measured from the time V_{DD} = V_{DD}(min.)	–	–	5	ms

Recommended Crystal Specifications[4]

Parameter	Description	Min	Max	Unit
Mode	Mode of Oscillation	Fundamental		
F	Frequency	25	25	MHz
ESR	Equivalent Series Resistance	–	50	Ω
C_S	Shunt Capacitance	–	7	pF

Parameter Measurements

Figure 2. 3.3 V Output Load AC Test Circuit

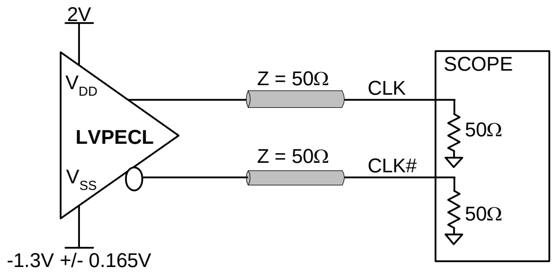


Figure 3. 2.5 V Output Load AC Test Circuit

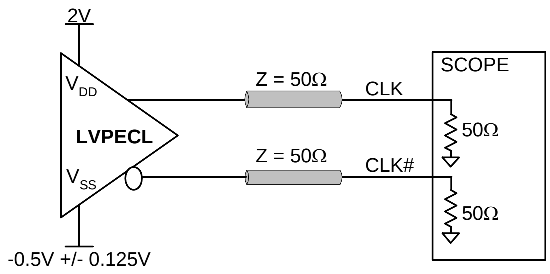


Figure 4. Output DC Parameters

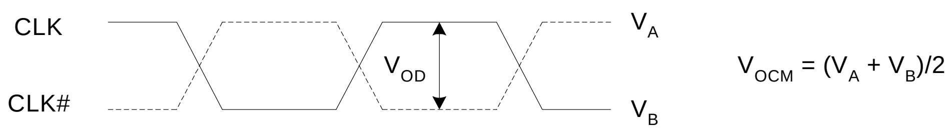
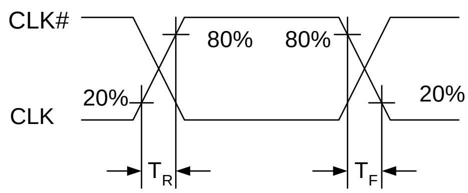


Figure 5. Output Rise and Fall Time



Notes

3. Refer to Figure 5 on page 4.
4. Characterized using an 18 pF parallel resonant crystal.
5. Not 100% tested, guaranteed by design and characterization.
6. Refer to Figure 6 on page 5.
7. Refer to Figure 7 on page 5.

Figure 6. RMS Phase Jitter

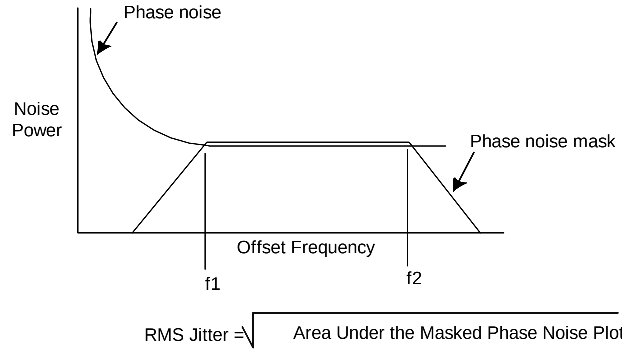


Figure 7. Output Duty Cycle

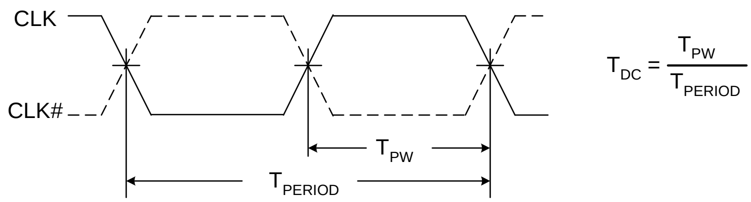
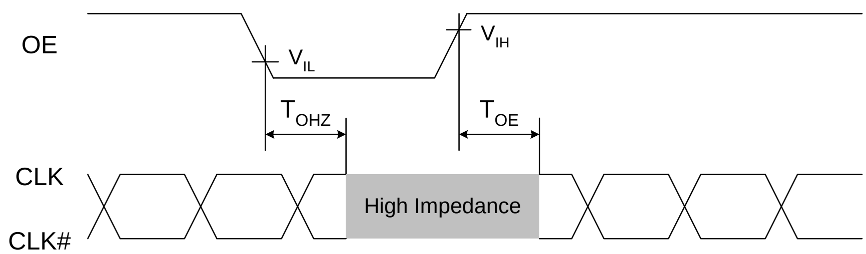


Figure 8. Output Enable Timing

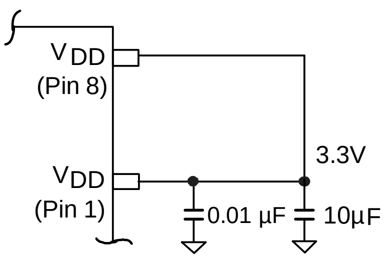


Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, noise at the power supply pins can degrade performance. To achieve optimum jitter performance, use good power supply isolation practices. Figure 9 illustrates a typical filtering scheme. Because all of the current flows through pin 1, the resistance and inductance between this pin and the supply is minimized. A 0.01 or 0.1 µF ceramic chip capacitor is also located close to this pin to provide a short and low impedance AC path to ground. A 1 to 10 µF ceramic or tantalum capacitor is located in the general vicinity of this device and may be shared with other devices.

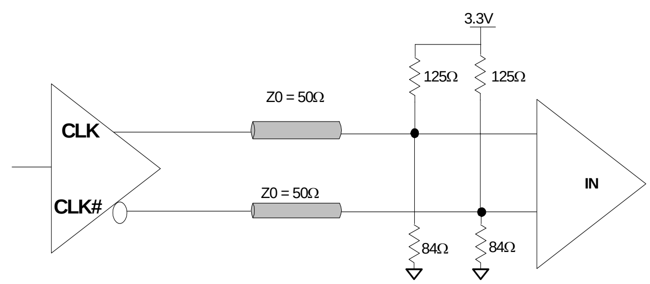
Figure 9. Power Supply Filtering



Termination for LVPECL Output

The CY2XP31 implements its LVPECL driver with a current steering design. For proper operation, it requires a 50 ohm dc termination on each of the two output signals. For 3.3 V operation, this data sheet specifies output levels for termination to V_{DD}–2.0 V. This same termination voltage can also be used for V_{DD} = 2.5 V operation, or it can be terminated to V_{DD}-1.5 V. Note that it is also possible to terminate with 50 ohms to ground (V_{SS}), but the high and low signal levels differ from the data sheet values. Termination resistors are best located close to the destination device. To avoid reflections, trace characteristic impedance (Z_0) should match the termination impedance. Figure 10 shows a standard termination scheme.

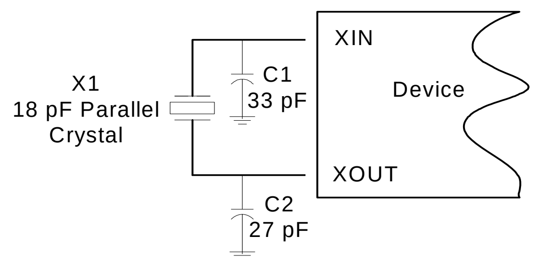
Figure 10. LVPECL Output Termination



Crystal Input Interface

The CY2XP31 is characterized with 18 pF parallel resonant crystals. The capacitor values shown in Figure 11 are determined using a 25 MHz 18 pF parallel resonant crystal and are chosen to minimize the ppm error. Note that the optimal values for C1 and C2 depend on the parasitic trace capacitance and are therefore layout dependent.

Figure 11. Crystal Input Interface



Ordering Information

Part Number	Package Type	Product Flow
CY2XP31ZXC	8-Pin TSSOP	Commercial, 0°C to 70°C
CY2XP31ZXCT	8-Pin TSSOP – Tape and Reel	Commercial, 0°C to 70°C
CY2XP31ZXI	8-Pin TSSOP	Industrial, -40°C to 85°C
CY2XP31ZXIT	8-Pin TSSOP – Tape and Reel	Industrial, -40°C to 85°C

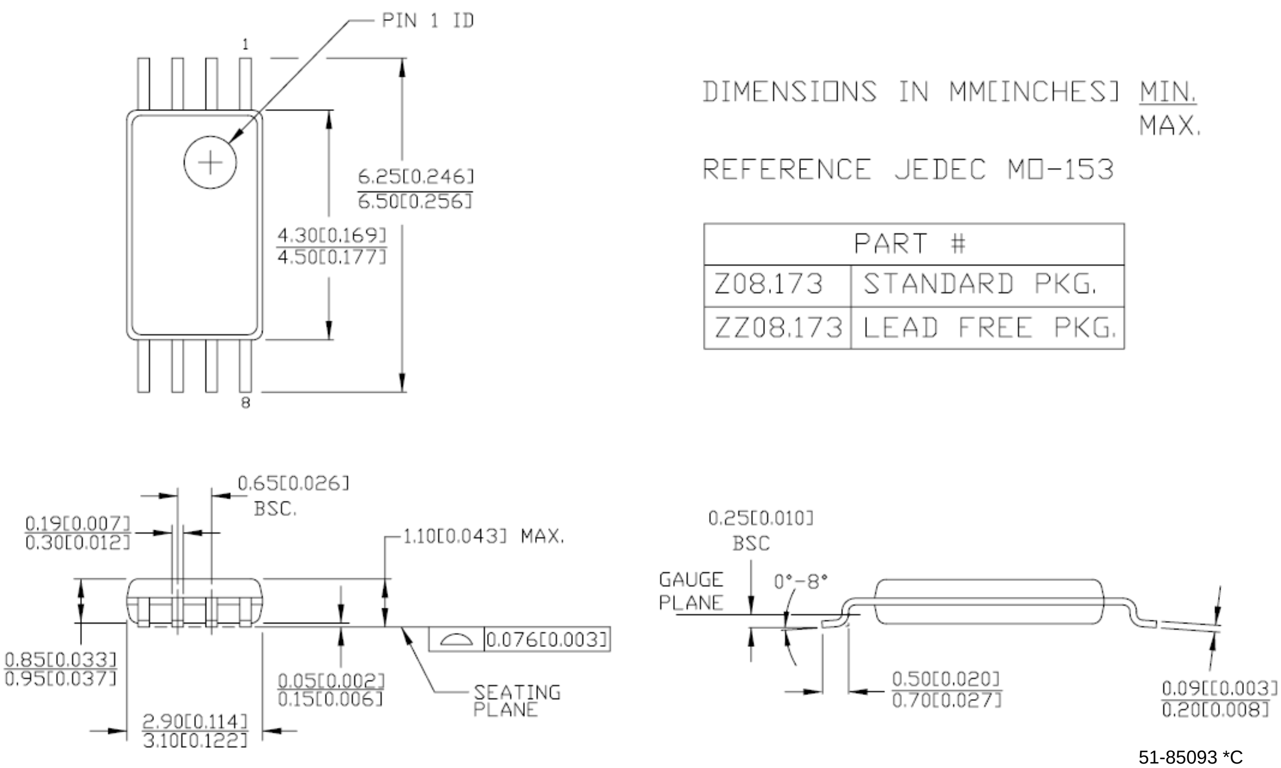
Ordering Code Definitions

CY xx xxx Z X C/I T

- **T** = Tape and Reel
- **Temperature Range**: C = Commercial, I = Industrial
- **Pb-free**
- **Package Type**
- **Part Identifier**
- **Family**
- **Company ID:** CY = Cypress

Package Drawing and Dimensions

Figure 12. 8-Pin Thin Shrunk Small Outline Package (4.40 MM Body) Z8



Acronyms

Table 2. Acronyms Used

Acronym	Description
CLKOUT	Clock output
CMOS	Complementary metal oxide semiconductor
DPM	Die pick map
EPROM	Erasable programmable read only memory
LVDS	Low-voltage differential signaling
LVPECL	Low voltage positive emitter coupled logic
NTSC	National television system committee
OE	Output enable
PAL	Phase alternate line
PD	Power-down
PLL	Phase locked loop
PPM	Parts per million
TTL	Transistor transistor logic

Document Conventions

Table 3. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
kHz	kilohertz
kΩ	kilohms
MHz	megahertz
MΩ	megaohms
µA	microamperes
µs	microseconds
µV	microvolts
µVrms	microvolts root-mean-square
mA	milliamperes
mm	millimeters
ms	milliseconds
mV	millivolts
nA	nanoamperes
ns	nanoseconds
nV	nanovolts
Ω	ohms

Document History Page

Document Title: CY2XP31 312.5 MHz LVPECL Clock Generator Document Number: 001-06385				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	422680	RGL	See ECN	New data sheet
*A	506198	RGL	See ECN	Supplied values in TBDs, Change status from Advance Information to Preliminary
*B	1337067	JWK / KVM /ARI	See ECN	Changed VCC* to VDD*, VEE to VSS, Gave pins 1 and 8 the same name (VDD), Added MSL and CIN specifications, Removed pull up from pin 5, Changed V_{IL}, V_{IH}, I_{IH}, I_{DD}, I_{DDA}, V_{OH}, V_{OL}, t_R and t_F specifications, Added commercial temperature, Changed supply filtering recommendations Removed alternate termination figure, Cleaned up several drawings Fixed cross references and edited data sheet for template compliance, Title change
*C	2669117	KVM/ AESA	03/05/2009	Changed crystal frequency to 25 MHz only; removed other frequencies; output frequencies adjusted accordingly, Changed phase jitter value, Removed MSL spec Changed IIL and IIH values, Changed rise / fall time value from 350 ps to 500 ps Changed max junction temp from 125°C to 135°C, Added thermal resistance Clarified that IDD is with outputs loaded, Changed Data Sheet Status to Final.
*D	2700242	KVM/PYRS	04/30/2009	Typos: changed VCC to VDD OE pin capacitance changed from 7pF to 15pF Changed IDD footnote Reformatted AC & DC tables Added specs CINX and IOZ Added OE timing, and startup timing Added OE waveforms Added IDD for 2.5 V Changed footnote about external power dissipation
*E	2718433	WWZ/HMT	06/12/2009	No change. Submit to ECN for product launch.
*F	2767308	KVM	09/22/2009	Add I_{DD} spec for unterminated outputs Change parameter name for I_{DD} (terminated outputs) from I_{DD} to I_{DDT} Remove I_{DD} footnote about externally dissipated current Add footnote reference to C_{IN} and C_{INX}:not 100% tested Add max limit for T_R, T_F: 1.0 ns Change T_{LOCK} max from 10 ms to 5 ms
*G	2896121	KVM	03/19/2010	Updated Package Diagram (Figure 12)
*H	3219081	BASH	04/07/2011	Template and style updates as per current Cypress standards. Added ordering code definitions, acronyms, and units of measure. Updated package diagram to *C.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 5