



# CYPRESS **PRELIMINARY**

## CY2SSTU877

### 1.8V, 500-MHz, 10-Output JEDEC-Compliant Zero Delay Buffer

#### Features

- Operating frequency: 125 MHz to 500 MHz
- Supports DDRII SDRAM
- Ten differential outputs from one differential input
- Spread-Spectrum-compatible
- Low jitter (cycle-to-cycle): < 40 ps
- Very low skew: < 40 ps
- Power management control input
- 1.8V operation
- Fully JEDEC-compliant
- 52-ball BGA and a 40-pin MLF (QFN)

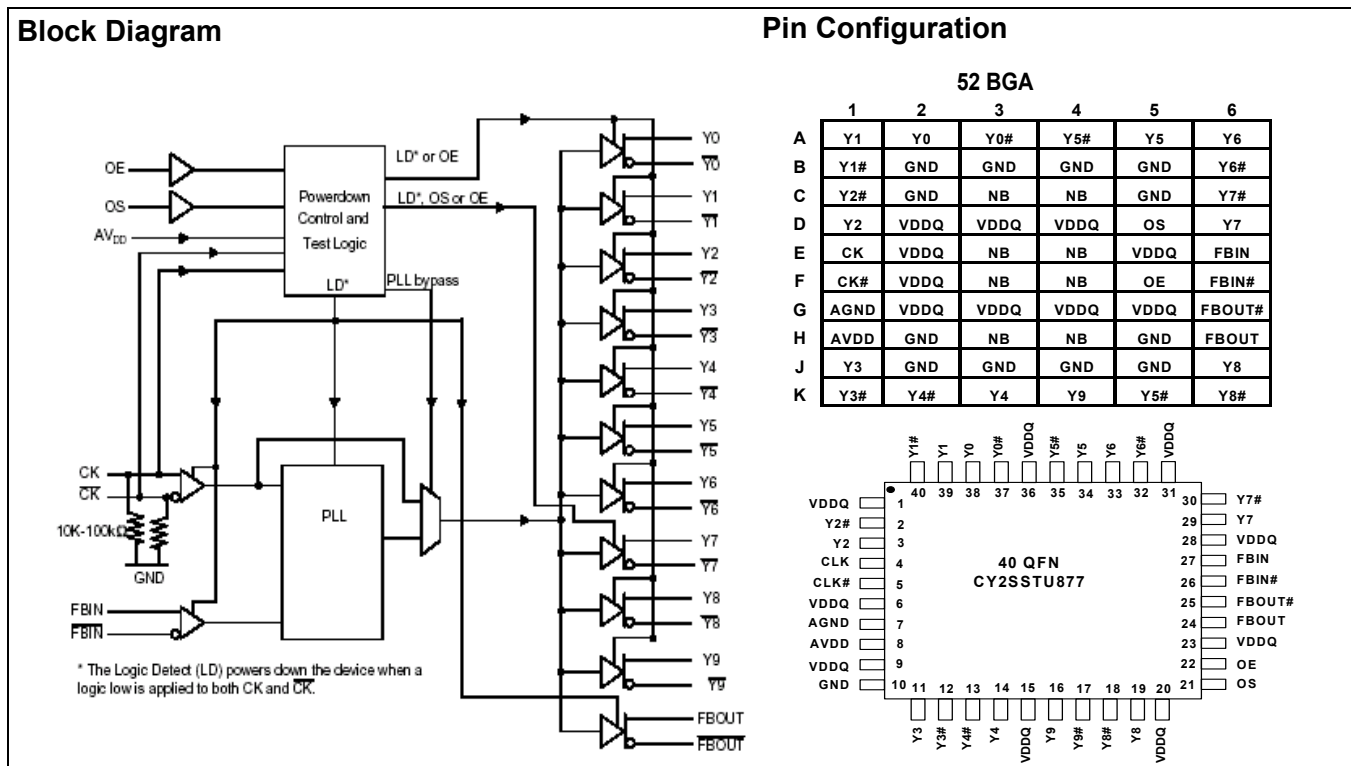
#### Functional Description

The CY2SSTU877 is a high-performance, low-skew, low-jitter zero delay buffer designed to distribute differential clocks in high-speed applications. The CY2SSTU877 generates ten differential pair clock outputs from one differential pair clock input. In addition, the CY2SSTU877 features differential feedback clock outputs and inputs. This allows the CY2SSTU877 to be used as a zero delay buffer. When used as a zero delay buffer in nested clock trees, the CY2SSTU877 locks onto the input reference and translates with near zero delay to low-skew outputs.

This phase-locked loop (PLL) clock buffer is designed for a VDD of 1.8V, an AVDD of 1.8V and differential data input and output levels. Package options include a plastic 52-ball VFBGA and a 40-pin MLF (QFN). The device is a zero delay buffer that distributes a differential clock input pair (CK, CK#) to ten differential pair of clock outputs (Y[0:9], Y#[0:9]) and one differential pair feedback clock outputs (FBOU, FBOU#). The input clocks (CK, CK#), the feedback clocks (FBIN, FBIN#), the LVCMOS (OE, OS), and the analog power input (AVDD) control the clock outputs.

The PLL in the CY2SSTU877 clock driver uses the input clocks (CK, CK#) and the feedback clocks (FBIN, FBIN#) to provide high-performance, low-skew, low-jitter output differential clocks (Y[0:9], Y#[0:9]). The CY2SSTU877 is also able to track Spread Spectrum Clocking (SSC) for reduced EMI.

When AVDD is grounded, the PLL is turned off and bypassed for test purposes. When both clock signals (CK, CK#) are logic low, the device will enter a low-power mode. An input logic detection circuit on the differential inputs, independent from the input buffers, will detect the logic low level and perform a low-power state where all outputs, the feedback, and the PLL are OFF. When the inputs transition from both being logic low to being differential signals, the PLL will be turned back on, the inputs and outputs will be enabled and the PLL will obtain phase lock between the feedback clock pair (FBIN, FBIN#) and the input clock pair (CK, CK#) within the specified stabilization time  $t_L$ .





## Pin Description

Pin No.		Name	Description
(BGA)	QFN		
G1	7	AGND	Ground for 1.8V analog supply
H1	8	AVDD	1.8V analog supply
E1, F1	4, 5	CLK, CLK#	Differential clock input with a (10K–100K $\Omega$ ) pull-down resistor
E6, F6	27, 26	FBIN, FBIN#	Feedback differential clock input
H6, G6	24, 25	FBOU, FBOU#	Feedback differential clock output
B2, B3, B4, B5, C2, C5, H2, H5, J2, J3, J4, J5	10	GND	Ground
F5	22	OE	Output enable (ASYNC) for Y[0:9] and Y# [0:9]
D5	21	OS	Output Select (Tied to GND or VCC)
D2, D3, D4, E2, E5, F2, G2, G3, G4, G5	1, 6, 9, 15, 20, 23, 28, 31, 36	VDDQ	1.8V supply
A2, A1, D1, J1, K3, A5, A6, D6, J6, K4,	38, 39, 3, 11, 14, 34, 33, 29, 19, 16	Y [0:9]	Buffered output of input clock, CLK
A3, B1, C1, K1, K2, A4, B6, C6, K6, K5	37, 40, 2, 12, 13, 35, 32, 30, 18, 17	Y# [0:9]	Buffered output of input clock, CLK

Table 1. Function Table

Inputs					Outputs				PLL
AVDD	OE	OS	CLK	CLK#	Y	Y#	FBOU	FBOU#	
GND	H	X	L	H	L	H	L	H	Bypassed/Off
GND	H	X	H	L	H	L	H	L	Bypassed/Off
GND	L	H	L	H	Lz	Lz	L	H	Bypassed/Off
GND	L	L	H	L	Lz, Y7 Active	Lz, Y7# Active	H	L	Bypassed/Off
VDD	L	H	L	H	Lz	Lz	L	H	On
VDD	L	L	H	L	Lz, Y7 Active	Lz, Y7# Active	H	L	On
VDD	H	X	L	H	L	H	L	H	On
VDD	H	X	H	L	H	L	H	L	On
VDD	X	X	L	L	Lz	Lz	Lz	Lz	Off
X	X	X	H	H	Reserved				

## Recommended Operating Conditions

Parameter	Description	Condition	Min.	Max.	Unit
T <sub>A</sub> (Ind.)	Ambient Operating Temp		-40	85	°C
T <sub>A</sub> (Com.)	Ambient Operating Temp		0	70	°C
V <sub>DD</sub>	Operating Voltage		1.7	1.9	V



### Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V <sub>IN</sub>	Input Voltage Range		-0.5	V <sub>DDQ</sub> + 0.5	V
V <sub>OUT</sub>	Output Voltage Range		-0.5	V <sub>DDQ</sub> + 0.5	V
T <sub>S</sub>	Storage Temperature		-65	150	°C
V <sub>CC</sub>	Supply Voltage Range		-0.5	2.5	V
I <sub>IK</sub>	Input Clamp Current		-50	50	mA
I <sub>OK</sub>	Output Clamp Current		-50	50	mA
I <sub>O</sub>	Continuous Output Current		-50	50	mA
	Continuous Current through V <sub>DD</sub> /GND		-100	100	mA

### DC Electrical Specifications

Parameter	Description	Conditions	Min.	Max.	Unit
V <sub>IX</sub>	Input Differential Crossing Voltage		(V <sub>DDQ</sub> /2) - 0.15	(V <sub>DDQ</sub> /2) + 0.15	V
V <sub>ID DC</sub>	Input Differential Voltage (DC Values)		0.3	V <sub>DDQ</sub> + 0.4	V
V <sub>ID AC</sub>	Input Differential Voltage (AC Values)		0.6	V <sub>DDQ</sub> + 0.4	V
V <sub>IL</sub>	Input Low Voltage	(OE, OS, CK, CK#)		0.35 * V <sub>DDQ</sub>	V
V <sub>IH</sub>	Input High Voltage	(OE, OS, CK, CK#)	0.65 * V <sub>DDQ</sub>		V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 100 μA		0.1	V
		I <sub>OL</sub> = 9 mA		0.6	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -100 μA	V <sub>DDQ</sub> - 0.2		V
		I <sub>OH</sub> = -9 mA	1.1		V
I <sub>OH</sub>	Output High Current			-9	mA
I <sub>OL</sub>	Output Low Current			9	mA
V <sub>IK</sub>	Input Clamping Voltage	I <sub>I</sub> = -18 mA		-1.2	V
V <sub>OD</sub>	Output Differential Voltage		0.5		V
V <sub>OX</sub>	Output Differential Crossing Voltage		V <sub>DDQ</sub> /2 - 0.08	V <sub>DDQ</sub> /2 + 0.08	V

### AC Electrical Specifications

Parameter	Description	Conditions	Min.	Max.	Unit
S <sub>LR(O)</sub>	Output Slew Rate	Y[0:9], Y#[0:9], FBOU, FBOU#	1.5	3	V/ns
S <sub>LR(I)</sub>	Input Slew Rate	CLK, CLK#, FBIN, FBIN#	1	4	V/ns
		OE	0.5		V/ns
C <sub>IN</sub>	Input Capacitance	(Input Capacitance of CK, CK#, FBIN, FBIN#) Vi = V <sub>DDQ</sub> or GND	2	3	pF
C <sub>OUT</sub>					pF
C <sub>IN(DELTA)</sub>		Ci(delta) (CK, CK#, FBIN, FBIN#) Vi = V <sub>DDQ</sub> or GND	-0.25	0.25	pF

### AC Timing Specifications

Parameter	Description	Conditions	Min.	Max.	Unit
F <sub>CLK</sub>	Clock Frequency		125	500	MHz
T <sub>DC</sub>	Duty Cycle		40	60	%
T <sub>LOCK</sub>	PLL Lock Time		-	10	μs
T <sub>jitt (cc)</sub>	Cycle-to-cycle jitter		-30	30	ps
T <sub>jitt (Period)</sub>	Period Cycle-to-cycle jitter		-40	20	ps

**AC Timing Specifications** (continued)

Parameter	Description	Conditions	Min.	Max.	Unit
T <sub>jit</sub> (H-Period)	Half Period Cycle-to-cycle jitter	Above 270 MHz	-45	45	ps
		Below 270 MHz	-70	70	ps
T <sub>d(0)</sub>	Static Phase Offset	Average 1000 cycles	-50	50	ps
T <sub>d(0)</sub>	Dynamic Phase Offset		-30	30	ps
T <sub>SKEW</sub>	Clock Skew		-	25	ps
T <sub>R</sub> /T <sub>F</sub>	Rise/Fall Time	(Y[0:9], Y#[0:9] @ 500 MHz)	-	300	ps
T <sub>ODC</sub>	Output Duty Cycle		49	51	%
T <sub>OENB</sub>	Output Enable Time	OE to any Y/Y#	-	8	ns
T <sub>ODIS</sub>	Output Disable Time	OE to any Y/Y#	-	8	ns
T <sub>PLH</sub>	Propagation Delay			8	ns

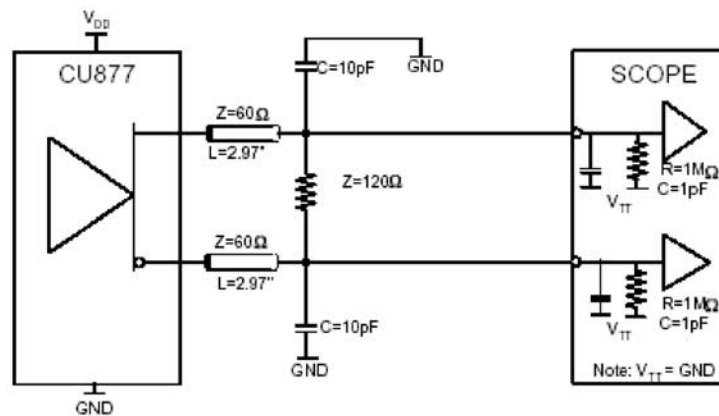


Figure 1. Test Loads for Timing Measurement #1

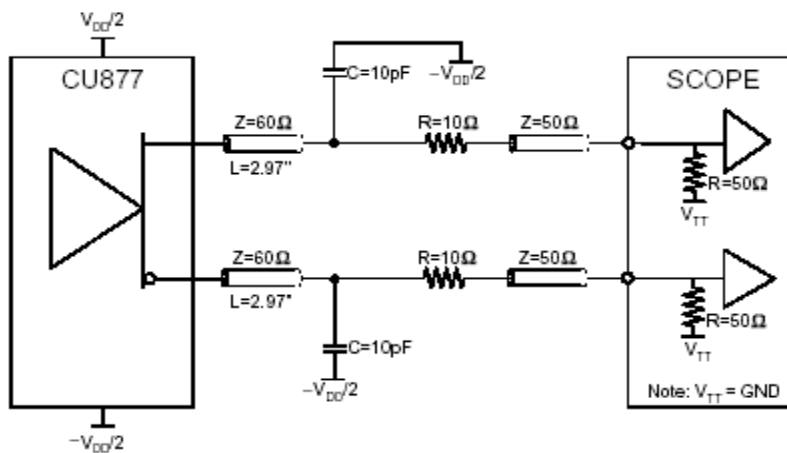
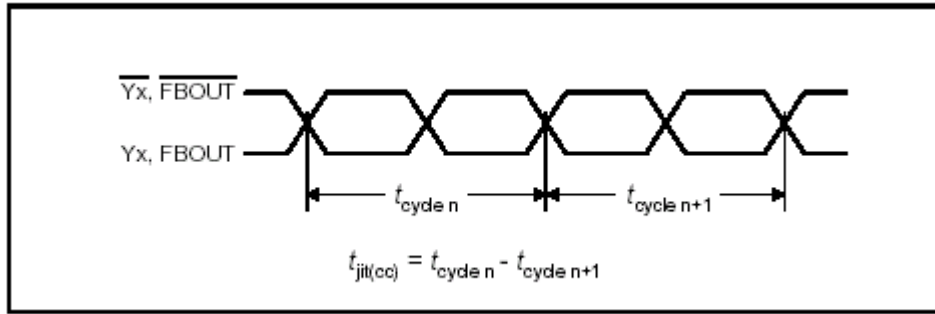
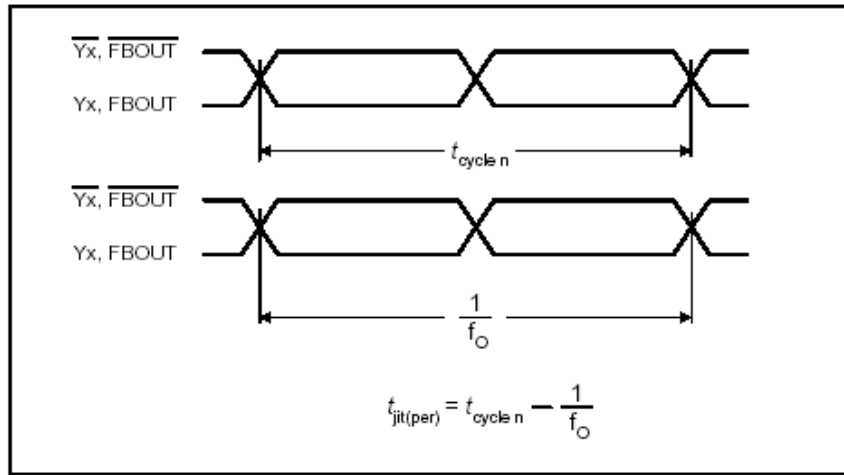


Figure 2. Test Loads for Timing Measurement #2

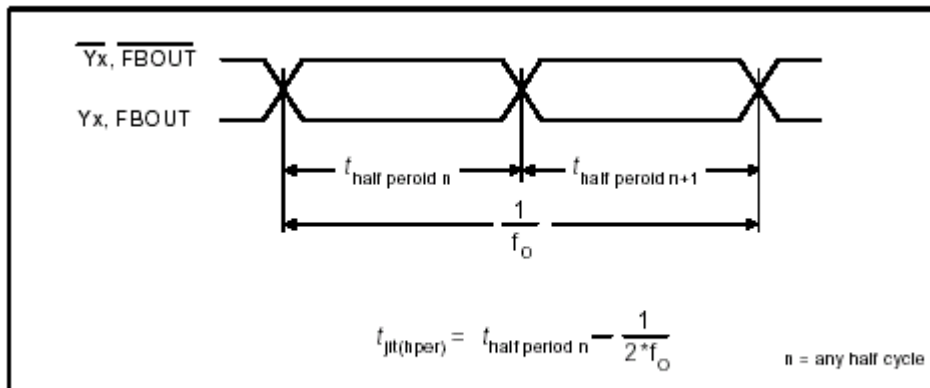


**Figure 3. Cycle to Cycle Jitter**



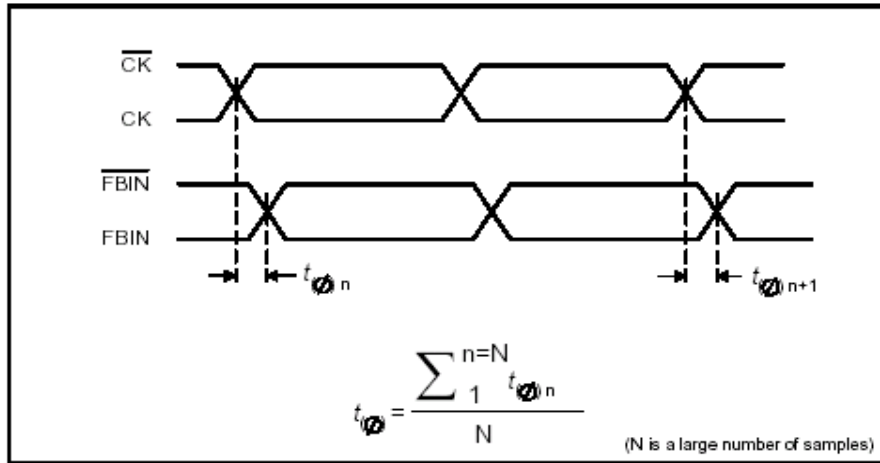
(f<sub>0</sub> = average input frequency measured at CK/CK)

**Figure 4. Period Jitter**



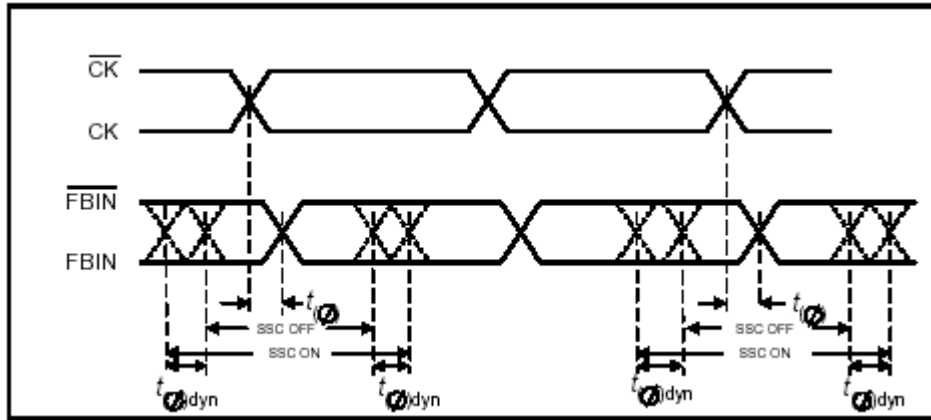
(f<sub>0</sub> = average input frequency measured at CK/CK)

**Figure 5. Half Period Jitter**

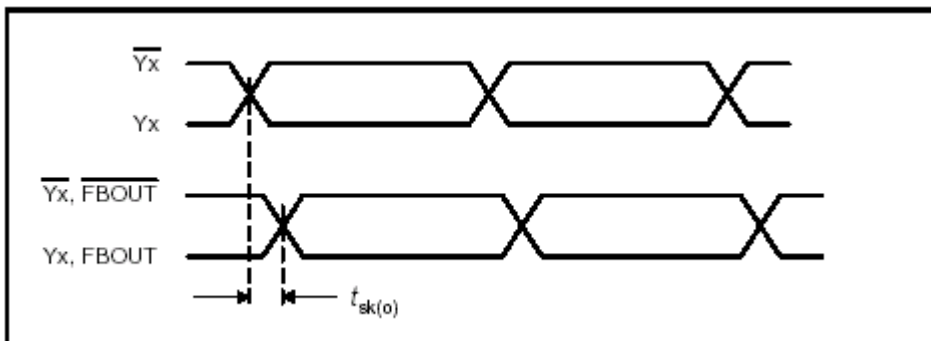


(N > 1000 samples)

**Figure 6. Static Phase Offset**



**Figure 7. Dynamic Phase Offset**



**Figure 8. Output Skew**

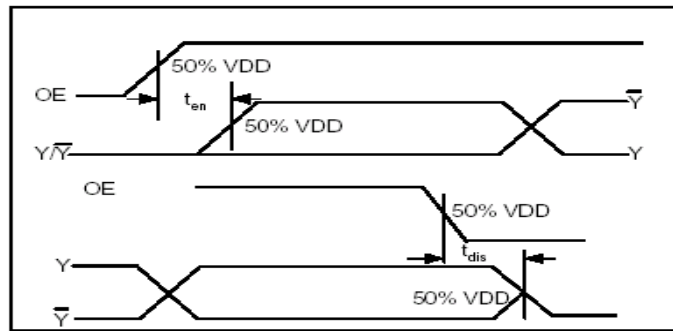


Figure 9. Time Delay Between OE and Clock Output (Y, Y)

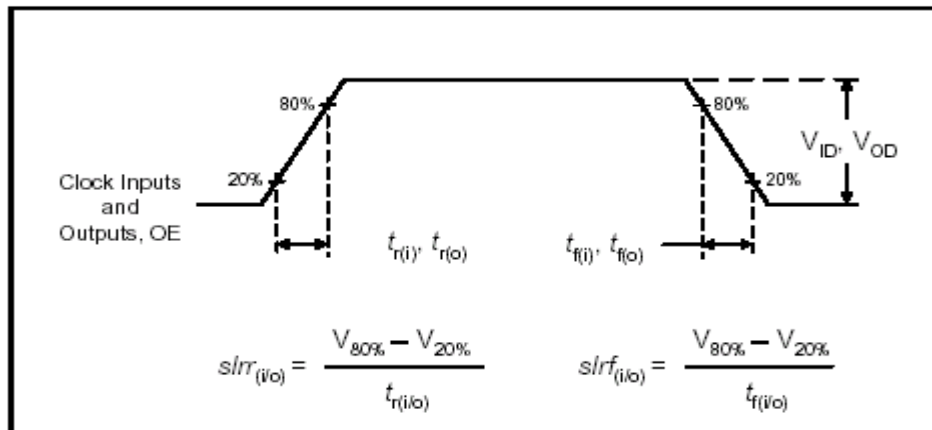


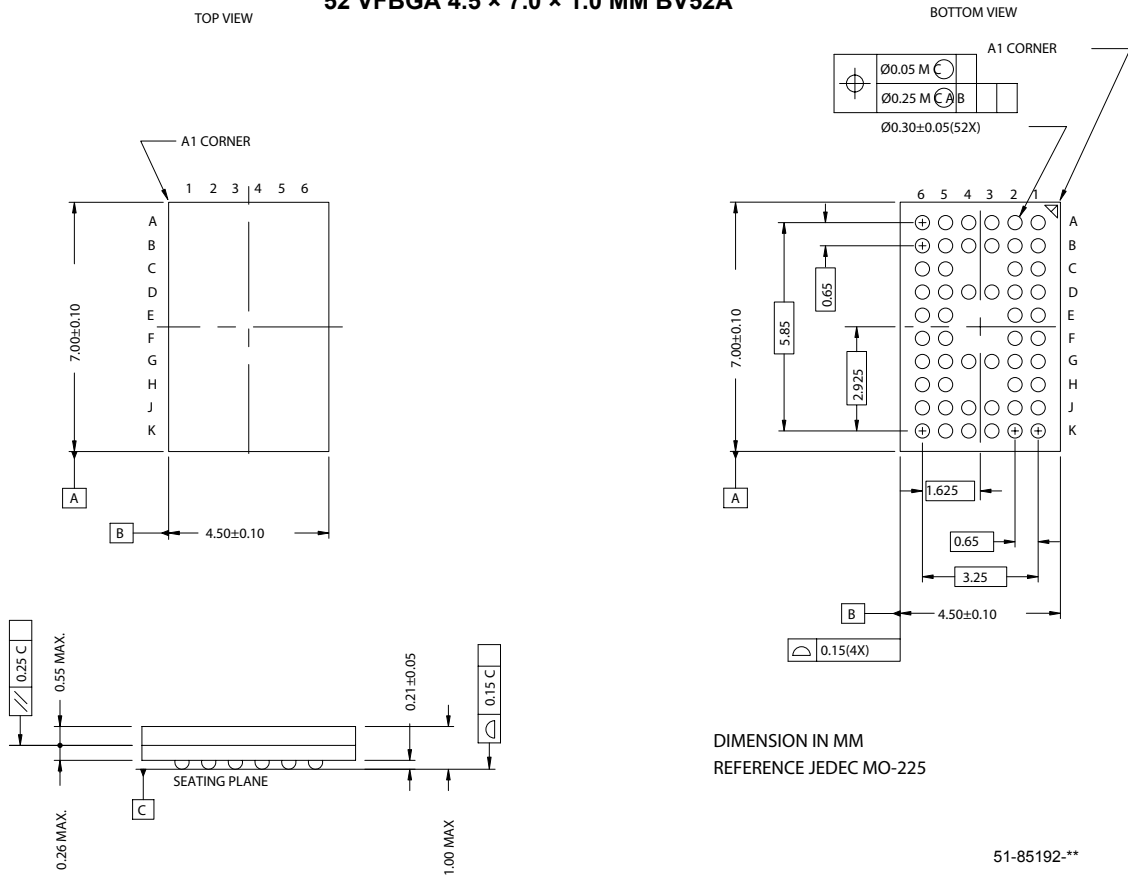
Figure 10. Input/Output Slew Rates

**Ordering Information**

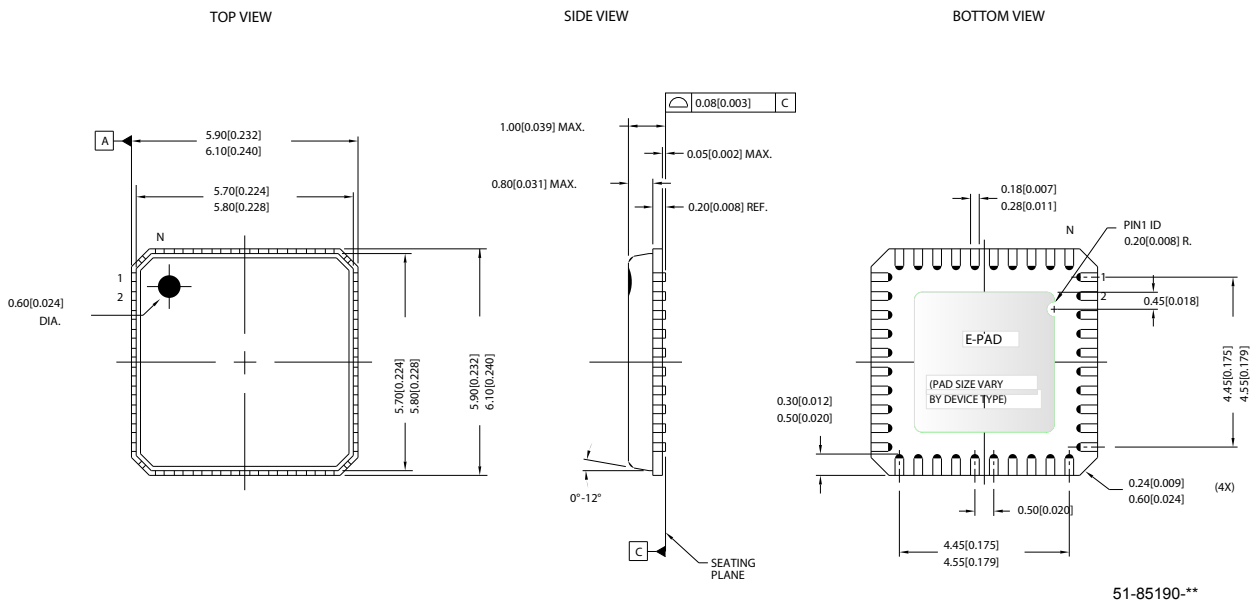
Part Number	Package Type	Product Flow
<b>Standard</b>		
CY2SSTU877LFC-XX	40-pin QFN	Commercial, 0° to 70°C
CY2SSTU877LFC-XXT	40-pin QFN – Tape and Reel	Commercial, 0° to 70°C
CY2SSTU877BVC-XX	52-pin VFBGA	Commercial, 0° to 70°C
CY2SSTU877BVC-XXT	52-pin VFBGA– Tape and Reel	Commercial, 0° to 70°C
CY2SSTU877LFI-XX	40-pin QFN	Industrial, –40° to 85°C
CY2SSTU877LFI-XXT	40-pin QFN – Tape and Reel	Industrial, –40° to 85°C
CY2SSTU877BVI-XX	52-pin VFBGA	Industrial, –40° to 85°C
CY2SSTU877BVI-XXT	52-pin VFBGA– Tape and Reel	Industrial, –40° to 85°C
<b>Lead-free</b>		
CY2SSTU877LFXC-XX	40-pin QFN	Commercial, 0° to 70°C
CY2SSTU877LFXC-XXT	40-pin QFN – Tape and Reel	Commercial, 0° to 70°C
CY2SSTU877BVXC-XX	52-pin VFBGA	Commercial, 0° to 70°C
CY2SSTU877BVXC-XXT	52-pin VFBGA– Tape and Reel	Commercial, 0° to 70°C
CY2SSTU877LFXI-XX	40-pin QFN	Industrial, –40° to 85°C
CY2SSTU877LFXI-XXT	40-pin QFN – Tape and Reel	Industrial, –40° to 85°C
CY2SSTU877BVXI-XX	52-pin VFBGA	Industrial, –40° to 85°C
CY2SSTU877BVXI-XXT	52-pin VFBGA– Tape and Reel	Industrial, –40° to 85°C

**Package Drawing**

**52 VFBGA 4.5 × 7.0 × 1.0 MM BV52A**



**40-lead QFN 6 x 6 MM LF40A**



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**Document History Page**

<b>Document Title: CY2SSTU877 1.8V, 500-MHz, 10-Output JEDEC-Compliant Zero Delay Buffer</b>				
<b>Document Number: 38-07575</b>				
<b>Rev.</b>	<b>ECN No.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	129198	08/22/03	RGL	New Data Sheet
*A	204389	See ECN	RGL	Added more Information. Deleted 4 rows from the bottom of the Pin description.
*B	310414	See ECN	RGL	Changed Advance Info. to Preliminary status Added Lead-free devices