Application Note

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PowerPC™ MPC7455 I/O Power Evaluation

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I/O power consumption for the PowerPC™ MPC7455 is not explicitly listed in the current MPC7455 *Hardware Specification*; however, it is suggested that a typical value is less than 20% of V_{DD} power. This value has been proven to be extremely conservative with typical measured values around 2% of V_{DD} power and max measured values less than 3%. The purpose of this document is to show the methodology used to reach these conclusions.

Part I Initial Theoretical Power

The initial theoretical power can be calculated using equation 1, shown below where P_{th} is theoretical power, n is active signals, C is load capacitance per pin, V is voltage swing, and f is average frequency per signal:

$$P_{th} = n * C * V^2 * f \qquad \text{(EQ1)}$$

In order to test this formula, a logic analyzer was used to collect signal transitions from the MPC7455 while running a bus-intensive Embedded Microprocessor Benchmark Consortium (EEMBC) benchmark. These transitions were then used to calculate f, average frequency of signals, for the above equation and theoretical power was calculated.

1.1 Sampling the JPEG Compression EEMBC Benchmark

The JPEG compression benchmark was chosen to evaluate theoretical power because it is a bus intensive benchmark. This benchmark retrieves bitmap data and converts it into JPEG format, simulating a common consumer digital camera application.

All active I/O signals were sampled using a logic analyzer including 32 address signals, 64 data signals and 12 control signals. In order to retrieve all signal states, the logic analyzer was set to sample at 1 / Bus Frequency. While collecting signal transitions using the logic analyzer, all caches were disabled in order to force all signals to be driven on the bus. Signals were then collected across three sampling periods, chosen to sample data from the beginning, middle, and end of the benchmark in an attempt to observe any variances.

1.2 Evaluating Signal Transitions

To evaluate signal transitions, a perl script was written to retrieve data line by line from the logic analyzer listings, count the number of transitions per signal, and write that number to a file. Also, using the number of transitions per signal, theoretical power was calculated using the power equation as shown in Figure 1-1.

$$P = n * C * V^2 * f$$

n - Active Signals
C - Load Capacitance per pin
V - Voltage Swing
f - Average Frequency Per Active Signal

$$f = \frac{\Sigma(\text{transitions}) * \text{Bus Frequency}}{2 * \text{Total Bus Clocks} * n}$$

$$n * f = \frac{\Sigma(\text{transitions}) * \text{Bus Frequency}}{2 * \text{Total Bus Clocks}}$$

$$P = \frac{C * V^2 * \Sigma(\text{transitions}) * \text{Bus Frequency}}{2 * \text{Total Bus Clocks}}$$

Figure 1-1. Power Formula Derivation

It is important to note that for the theoretical calculations, voltage swing (2.5 volts) and bus frequency can be measured and verified; however, for capacitance, a value of 10 pF per pin is used which is derived from the 8.0 pF maximum value in the hardware specification plus 2.0 pF for connections to the logic analyzer.

1.3 Initial Theoretical Results Summary

Data was collected over 394,710 clock cycles while running the JPEG decompression benchmark at a bus frequency of 100 MHz. Average frequency of the 106 active signals was 2.7 MHz, corresponding to an initial theoretical power value of 17.8 mW.

Taking a closer look at signals and associated average frequencies and power (see Table 1), it is evident that the low power value can partly be credited to a low frequency of signal transitions.

Table 1. Average Frequency and Power Associated with I/O Signals

Signal	Average Signal Transition Frequency (MHz)	Power (mW)
Address Signals	0.81	1.63
Data Signals	3.71	14.84
Control Signals	1.28	1.47

Part II Actual Power Measurement

Figure 2-2 shows the circuit used to measure actual power for this analysis. In order to measure I/O power the resistor R74 was removed from an MPC7455 development system and replaced with an ammeter as shown. Completely isolating OV_{DD} is difficult and as Figure 2-2 depicts, any current measurements include

some additional current from the Tundra Tsi107™ PowerPC host bridge and buffer. This additional current is very small and does not dramatically effect the measurements.

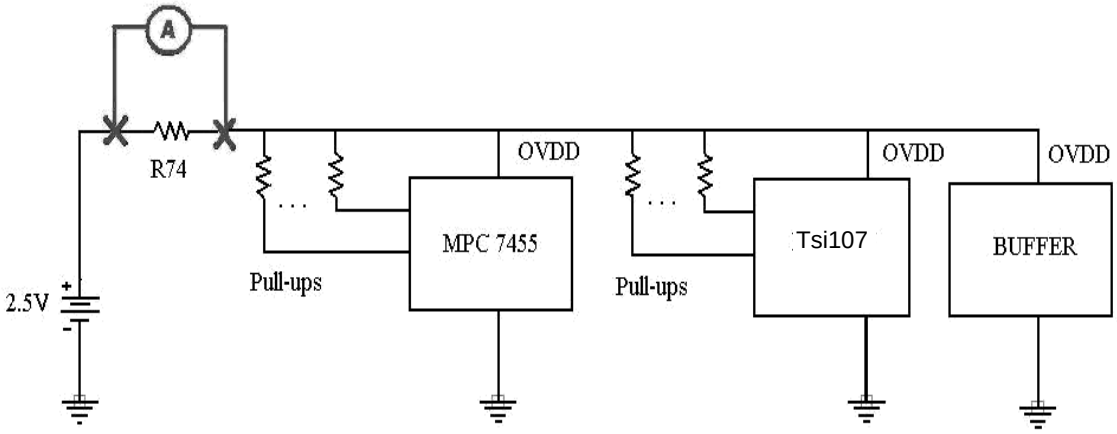

Figure 2-2. Actual Measurement Schematic

2.1 Actual Power Measurement Results

Using the technique pictured in Figure 2-2 while running the JPEG compression benchmark, the following measurement was attained:

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I = 81.6 mA -> P = V * I and at 2.5 V
P = 204 mW
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The measurement was taken with the caches disabled in order to force all signals to be driven on the bus; a lower power measurement could be attained with the caches were enabled. Although still very low, this result conflicts with the initial theoretical power calculation of 17.8 mW.

2.2 Actual vs. Initial Theoretical Power Discrepancies

Quiescent and leakage currents, pictured in Figures 2-3 account for some power losses and can help explain the discrepancy between measured and initial theoretical power values. Using the measurement schematic in Figure 2-2, these power losses can be measured.

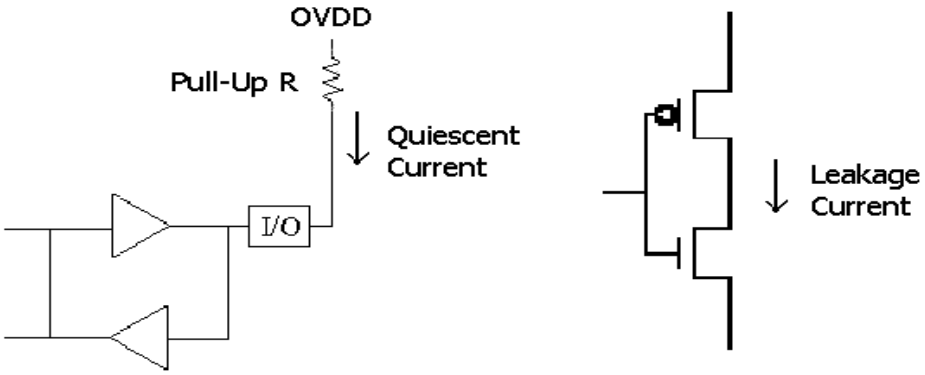

Figure 2-3. Quiescent and Leakage Current Diagrams

For this measurement, a routine was written to continuously branch to itself. With the caches enabled, it is assumed that the bus will be idle, meaning any current measured can be attributed to power losses. Once

again as Figure 2-2 depicts, the Tsi107 host bridge and buffer have an effect on the current measurement but their effect is small. This theory was tested by tracking memory signals with the logic analyzer and in fact, less than a handful of signals were driven during the routine and they transitioned at a very low frequency. While running this routine on the MPC7455 the following measurement was taken:

$$I_{LOSSES} = 65\ mA \rightarrow P_{LOSSES} = 162.5\ mW$$

After adding this result with the initial theoretical power from Part I, a final theoretical power value of 180.3 mW is attained which is very close to the measured value of 204 mW. The close relationship of the two values proves the validity of the measured value.

2.3 Measured Power for all EEMBC Benchmarks

The same procedure, including having the caches off, for measuring actual I/O power for the JPEG compression benchmark was used for the 46 other EEMBC benchmarks and the results are summarized in Figure 2-4.

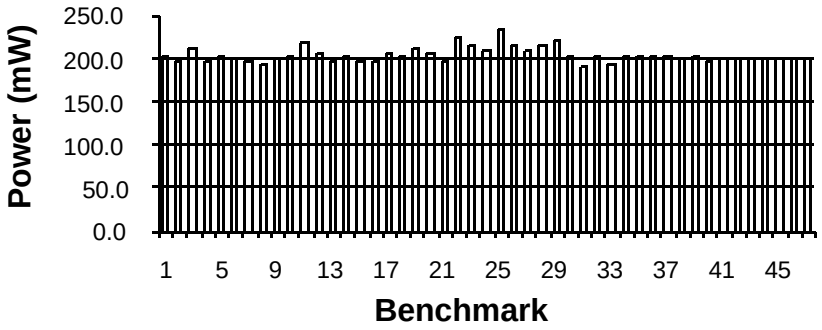

Figure 2-4. Power for all EEMBC Benchmarks

The average current measured for all 47 benchmarks was 81.2 mA corresponding to an average power of 203.1 mW. These benchmarks were created to simulate a variety of real world applications so these results can represent typical I/O power values for the MPC7455. From Figure 2-4, one can see that typical I/O power is not only low at around 200 mW, but also does not vary much at all.

Part III Varying Bus Frequency and Power

The equation shown in Figure 1-1 implies that power is linearly related to bus frequency. This section investigates that assumption.

3.1 Varying Bus Frequency Measurements

Using the same setup pictured in Figure 2-2, current measurements were taken at bus frequencies of 66, 100, and 133 MHz for the JPEG compression benchmark. Power losses and initial theoretical power were also re-evaluated for the same varying frequencies. The results are summarized in Table 2 below.

Table 2. Power Values at Varying Frequencies (in mW)

Value	66 MHz	100 MHz	133 MHz
Initial Theoretical Power	12	18	24
Power Losses	148	163	177
Total Theoretical Power	160	181	201
Measured Power	163	204	247

Figure 3-5 shows a graphical depiction of the data, and it shows that measured power and power losses both appear to vary linearly.

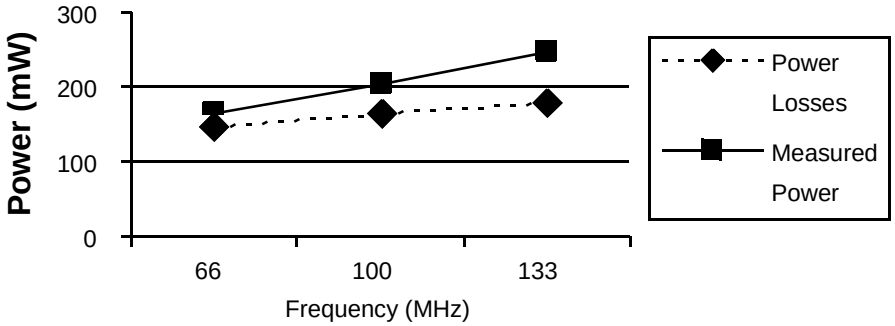

Figure 3-5. Power vs. Frequency Relationship

The linear relationship for measured power is expected; however, power losses associated with quiescent and leakage currents should be constant. The variance can be explained by considering the Tsi107 host bridge and buffer loads pictured in Figure 2-2.

Part IV Determining Maximum I/O Power

Sometimes it is necessary to determine maximum I/O power in order to appropriately provide enough power supply current. For that reason, this section investigates the derivation of a value for maximum I/O power on the MPC7455.

4.1 Measuring Maximum I/O Power

In order to simulate an application that affects the maximum number of I/O signals as frequently as possible, the routine depicted in Figure 4-6 was used.

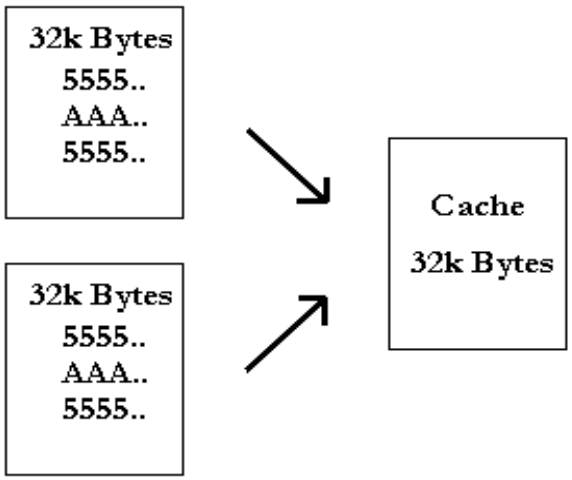

Figure 4-6. Max Power Simulation

The routine loads two 32k blocks of memory with alternating lines of 5s and As. Then, in the main loop, it continuously bursts data into the cache, alternating between memory blocks. The size of the memory block was chosen to be exactly twice the size of the cache to prevent any data from being pulled from cache rather than memory, and the location of the memory blocks was chosen such that as much variance in address signals could be achieved.

While running this routine on the MPC7455 the measured I/O power was 458.75 mW. This was run with a 100 MHz bus and the data signals were found to switch at an average frequency of 24 MHz.

4.2 Estimating Max I/O Power

It is possible that with a different system configuration, the frequency of data, address and control signal switching could increase slightly. Assuming a 100 MHz bus frequency it is possible to estimate a maximum (although not attainable) value for I/O power.

Assuming power can be calculated according to the equation below:

$$P = n * C * V^2 * f + P_o \qquad \text{(EQ 2)}$$

where P_o is constant for a given bus frequency and both P_o and C are unknowns. By using the process described in Part I, n and f are calculated while running varying routines, P is measured using the process shown in Part II and, of course, voltage swing (V) is constant. With this in mind, by running two routines, values for P_o and C can be attained (two equations, two unknowns) and by running a third routine these values can be checked.

This procedure was used with the JPEG compression benchmark, the maximum I/O power routine from section 4.1 and a third routine written to generate a power dissipation value in between these two values. The following results for P_o and C were attained and checked:

$$P_o = 0.147 \text{ W}$$
$$C = 29.7 \text{ pF}$$

These values can now be used to calculate a theoretical (but not attainable) maximum I/O power. When running a 100 MHz bus frequency where signals are triggered on the rising or trailing edge of the bus clock, the fastest frequency a signal could possibly transition is 50 MHz. Assuming all 108 I/O signals are active and transitioned at 50 MHz (which is not attainable), using EQ 2 above, theoretical maximum I/O power is only 1.15 W.

Conclusion

Although I/O power is not defined in the hardware specification for the MPC7455, it is defined typically to be less than 20% of V_{DD} power. V_{DD} power is listed in the hardware specification at 17.0 W with a processor frequency of 800 MHz (which is the processor frequency used for all examples at 100 MHz bus frequency). This corresponds to a typical I/O power value of 3.4 W. The EEMBC benchmarks were used to simulate typical applications and the I/O power measured while running these benchmarks was in the range of 200 mW, which is less than 2% of V_{DD} power. The maximum value for power measured on the MPC7455 was less than 3% of V_{DD} and maximum theoretical value is less than 7%. These results are summarized in Table 3 below. According to these results, I/O power as defined in the hardware specification is extremely conservative and could more accurately be described by a smaller value.

Table 3. Summary of Results

Result	Power	Relation to V_{DD} Power
Typical Power	204 mW	< 2%
Measured Maximum Power	458.75 mW	< 3%
Theoretical Maximum Power (Not Attainable)	1.15 W	< 7%

Revision History

Table 4 lists this document's significant changes and revisions.

Table 4. Document History

Rev. No.	Substantial Changes
0	Initial release
0.1	Nontechnical reformatting
0.2	Nontechnical reformatting

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