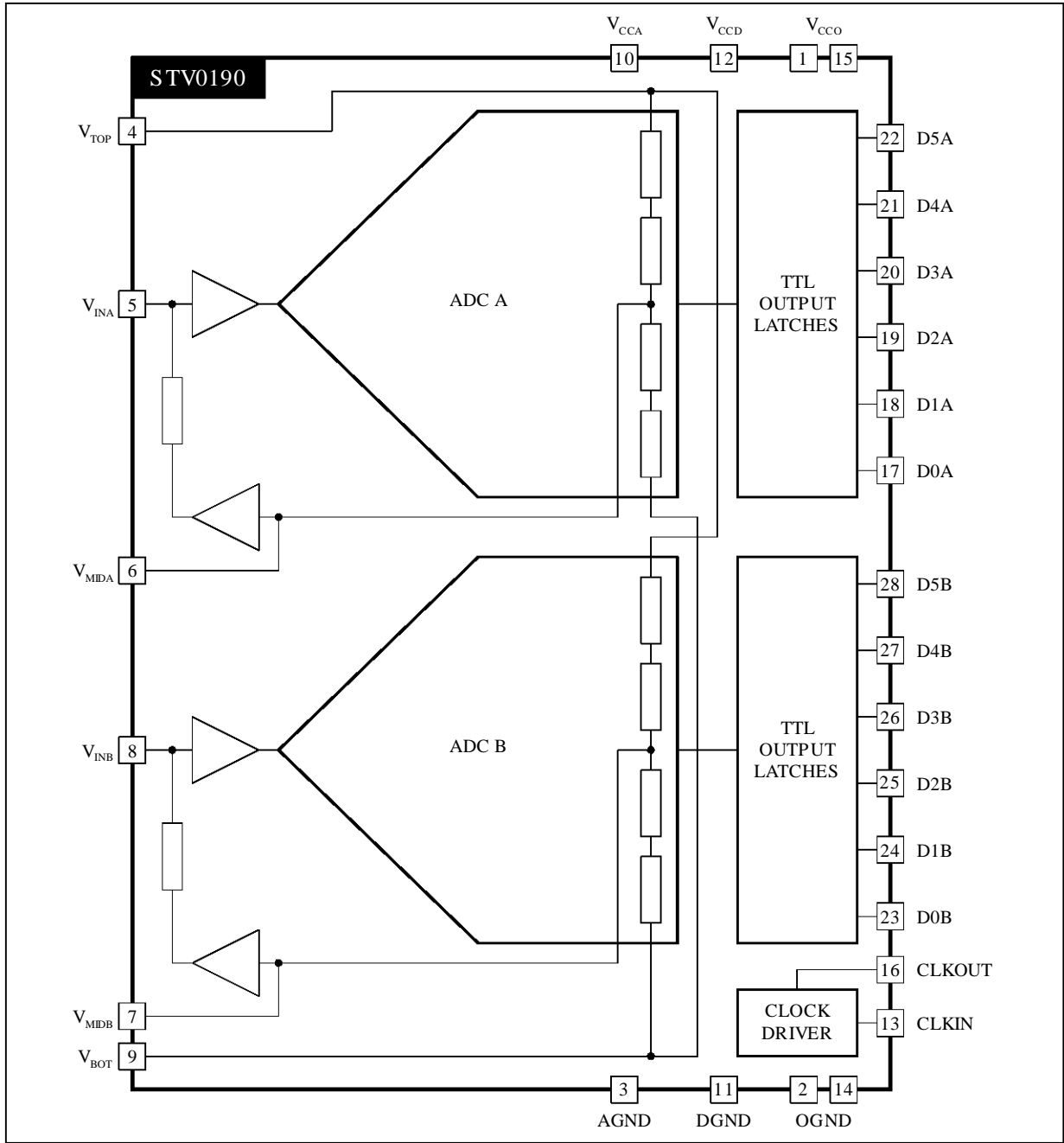


PIN CONFIGURATION

Pin N°	Symbol	Function
1	V _{CCO}	Output Buffer Supply Voltage Channel A + B
2	OGND	Output Buffer Ground Channel A + B
3	AGND	Analog Ground
4	V _{TOP}	Top Reference Voltage
5	V _{INA}	Analog Input Channel A
6	V _{MIDA}	Reference Voltage DC Coupling Channel A
7	V _{MIDB}	Reference Voltage DC Coupling Channel B
8	V _{INB}	Analog Input Channel B
9	V _{BOT}	Bottom Reference Voltage
10	V _{CCA}	Analog Supply Voltage
11	DGND	Digital Ground
12	V _{CCD}	Digital Supply Voltage
13	CLKIN	Clock Input
14	OGND	Output Buffer Ground Channel A + B
15	V _{CCO}	Output Buffer Supply Voltage Channel A + B
16	CLKOUT	Clock Output
17 to 22	D0A to D5A	D0 (LSB) to D5 (MSB) Outputs Channel A
23 to 28	D0B to D5B	D0 (LSB) to D5 (MSB) Outputs Channel B

0190-01.TBL

BLOCK DIAGRAM



0190-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
	Analog Supply Voltage	3.1, 3.45	V
	Digital Supply Voltage	3.1, 3.45	V
T _{oper}	Operating Temperature	0, +70	°C

0190-02.TBL

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.3V, T_{amb} = 0 to 70°C, Full scale 10MHz, 1.5V_{PP} input, 40MSPS, C_L = 20pF, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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ANALOG INPUT

	Differential Reference Voltage	V _{TOP} - V _{BOT}	1	1.5		V _{PP}
	Variation of Channel A to Channel B (FS)	0.5 LSB			8	mV
R _{IN}	Input Resistance		20			kΩ
	Input Bandwidth 3dB		20			MHz

DIGITAL OUTPUTS

	High Logic Voltage		2.4		V _{CC}	V																																												
	Low Logic Voltage		0		0.4	V																																												
	High Logic Current		-4			mA																																												
	Low Logic Current				4	mA																																												
	Logic Format		<table border="1"> <thead> <tr> <th colspan="2">Analog Input</th> <th colspan="2">Digital Output</th> </tr> </thead> <tbody> <tr> <td>most positive input</td> <td>63</td> <td>111111</td> <td></td> </tr> <tr> <td></td> <td>62</td> <td>111110</td> <td></td> </tr> <tr> <td></td> <td>....</td> <td>.....</td> <td></td> </tr> <tr> <td></td> <td>33</td> <td>100001</td> <td></td> </tr> <tr> <td></td> <td>32</td> <td>100000</td> <td></td> </tr> <tr> <td></td> <td>31</td> <td>011111</td> <td></td> </tr> <tr> <td></td> <td>30</td> <td>011110</td> <td></td> </tr> <tr> <td></td> <td>....</td> <td>.....</td> <td></td> </tr> <tr> <td></td> <td>1</td> <td>000001</td> <td></td> </tr> <tr> <td>least positive input</td> <td>0</td> <td>000000</td> <td></td> </tr> </tbody> </table>				Analog Input		Digital Output		most positive input	63	111111			62	111110					33	100001			32	100000			31	011111			30	011110					1	000001		least positive input	0	000000	
Analog Input		Digital Output																																																
most positive input	63	111111																																																
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	32	100000																																																
	31	011111																																																
	30	011110																																																
																																																
	1	000001																																																
least positive input	0	000000																																																
t _{PD}	Output Timing	See Figure 1			9	ns																																												
t _v	Output Timing	See Figure 1	5			ns																																												
t _{SKEW}	Data Output Skew TSK (all outputs, settled within 20%)	See Figure 1			1	ns																																												
t _{APER}	Aperture Delay relative to Data Clock	See Figure 1			1	ns																																												
t _R , t _F	Data Output Rise and Fall Time				4	ns																																												

CLOCK INPUT

V _{IH}	High Input Voltage		2.0		V _{CC}	V
V _{IL}	Low Input Voltage		0		0.8	V
I _{IH}	High Input Current				TBD	μA
I _{IL}	Low Input Current		TBD			μA
	Clock Duty Cycle		40		60	%
t _{CL}	Clock Period	See Figure 1	24			ns

0190-03.TBL

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CLOCK OUTPUT						
V_{OH}	High Output Voltage		2.4		V_{CC}	V
V_{OL}	Low Output Voltage		0		0.4	V
I_{OH}	High Output Current		-4			mA
I_{OL}	Low Output Current				4	mA
	Clock Duty Cycle		40		60	%
t_{CL}	Clock Period		24			ns

REFERENCE LADDER

	Top Voltage				$V_{CC} - 0.5$	V
	Bottom Voltage		$V_{CC} + 0.5$			V
	DC Bias Restoration Error	Open input digital output should be	32/64 011111		33/64 100000	
ZV_{TOP}/V_{BOT}	Input Impedance		90			Ω

CROSSTALK

	Isolation A/B		37			dB
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DC ACCURACY

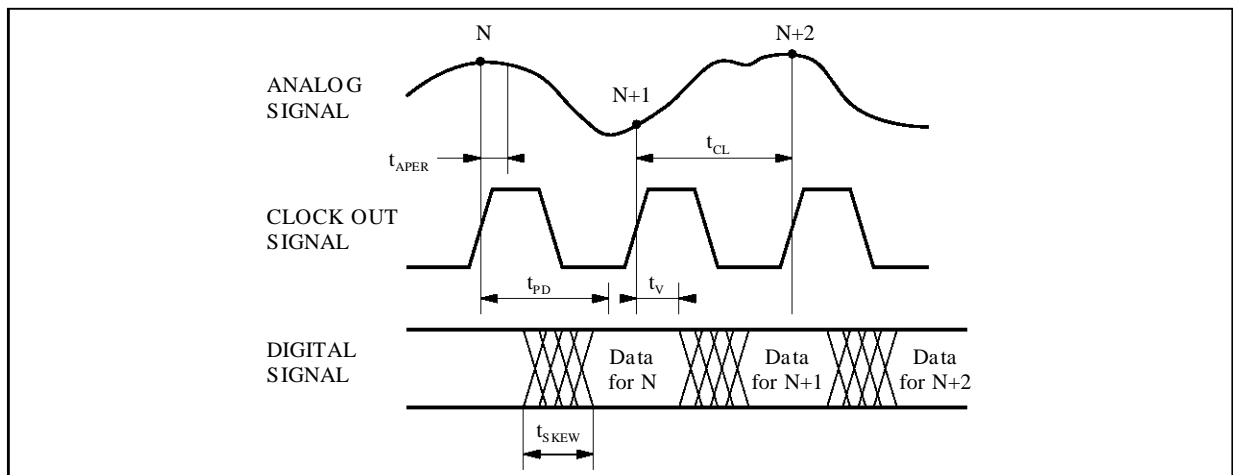
	Integral non Lin.		-0.5		+0.5	LSB
	Diff. Non Lin.		-0.5		+0.5	LSB

AC ACCURACY ($f_{IN} = 10\text{MHz}$, $FS = 40\text{MSPS}$, $V_{IN} = 95\% \text{FSCALE}$)

	Effective Number of Bit		5			bits
SNR			33			dB
THD	THD First 5 Harmony		33			dB
	Integral non Lin.		-1		+1	LSB
	A/D Amplifier Response Mismatching				0.2	dB

0190-04.TBL

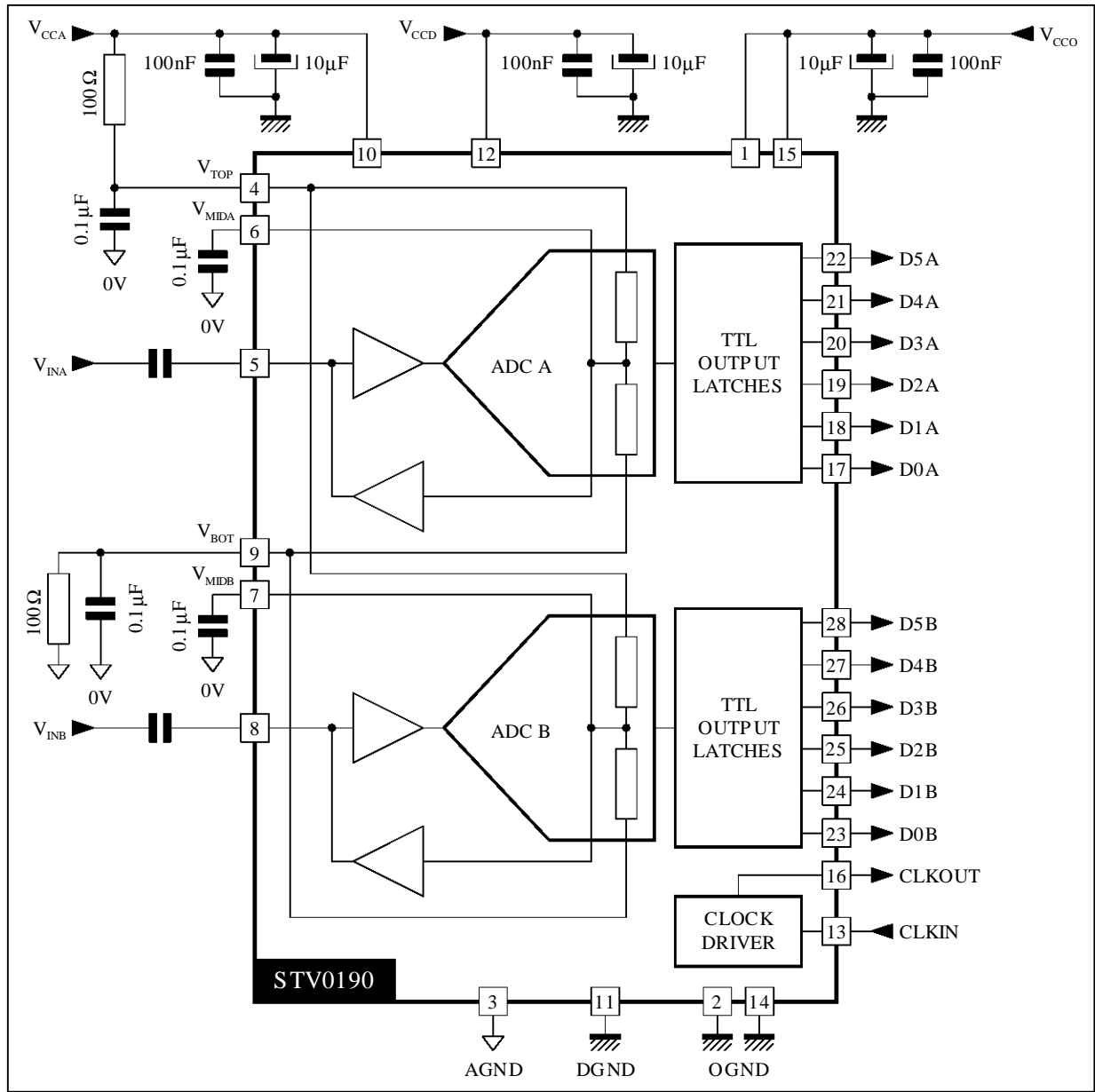
Figure 1 : Timing Diagram



0190-03.EPS

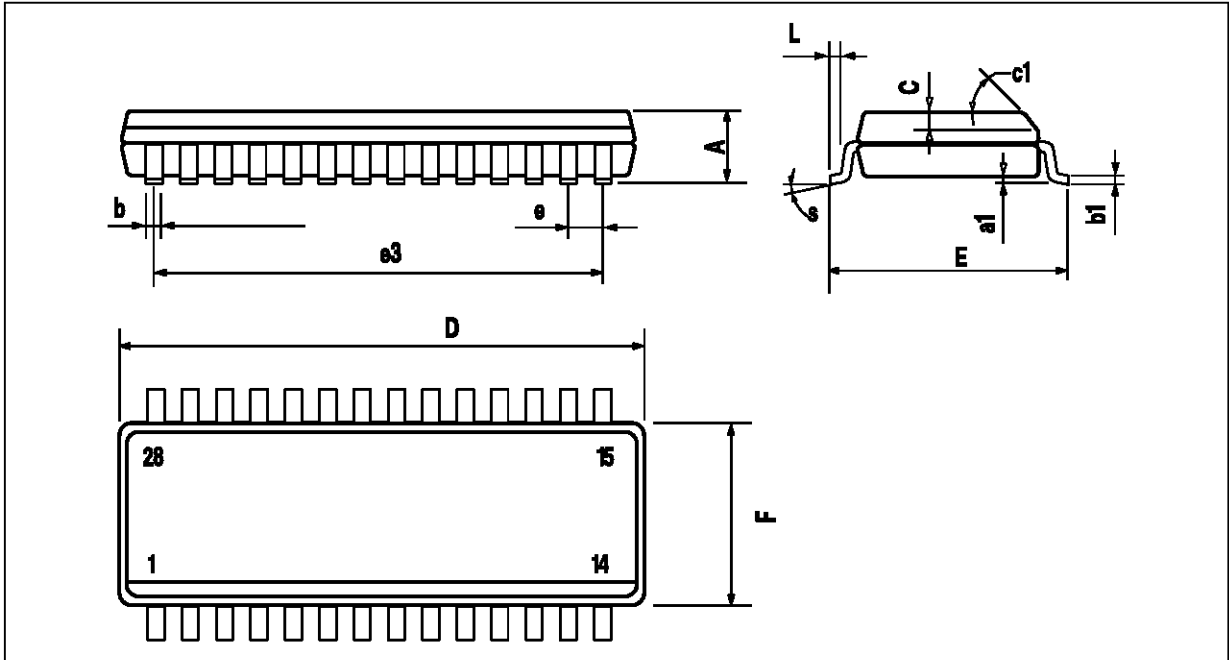
Note : This diagram shows a delay of one clock cycle. Additional integer multiple delay periods are acceptable. Output data must be valid on the rising edge of the clock out signal.

TYPICAL APPLICATION



0190-04-EFS

PACKAGE MECHANICAL DATA
 28 PINS - PLASTIC MICROPACKAGE (SO)



PM-SO28LEFS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (Typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8° (Max.)					

SO28TBL

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