CY2PD817

320-MHz 1:7 PECL to PECL/CMOS Buffer

Features

- **DC to 320-MHz operation**
- **50-ps output-output skew**
- **30-ps cycle-cycle jitter**
- **2.5V power supply**
- **LVPECL input @ 320-MHz Operation**
- **One LVPECL output @ 320-MHz Operation**
- **Four LVCMOS/LVTTL outputs @ 250 MHz/160 MHz**
- **Two LVCMOS/LVTTL outputs @ 250 MHz/80 MHz**
- **45% to 55% output duty cycle**
- **Output divider control**
- **Output enable/disable control**
- **Operating temperature range: 0°C to +85°C**
- **24-pin TSSOP**

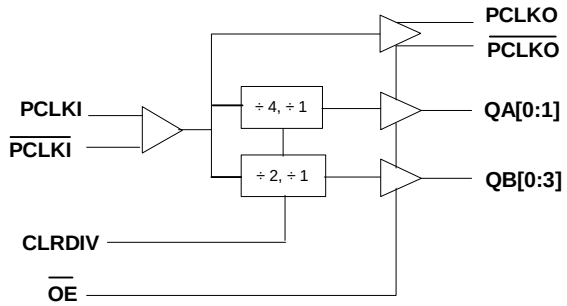
Description

The CY2PD817 is a low-voltage LVPECL-to-LVPECL and LVCMOS fanout buffer designed for servers, data communications, and clock management.

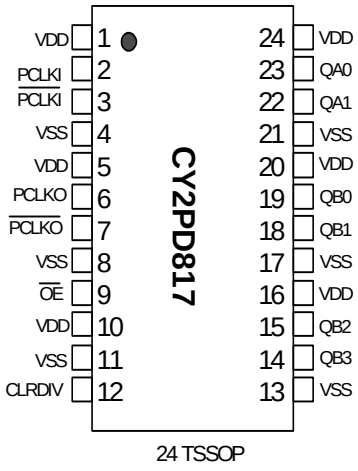
The CY2PD817 is ideal for applications requiring mixed differential and single-ended clock distribution. This device accepts an LVPECL input reference clock and provides one LVPECL and six LVCMOS/LVTTL output clocks. The outputs are partitioned into three banks of one, two, and four outputs. The LVPECL output is a buffered copy of the input clock while the LVCMOS outputs are divided by 1, 2, and 4. When CLRDIV is set HIGH, the output dividers are set to 1. In this mode, the maximum input frequency is limited to 250 MHz.

When $\overline{OE}$ is set HIGH, the outputs are disabled in a High-Z state.

Block Diagram



Pin Configuration



24 TSSOP

Pin Description[1]

Pin	Name	I/O	Type	Description
2	PCLKI	I, PD	LVPECL	LVPECL reference clock input
3	PCLKI	I, PU/PD	LVPECL	LVPECL reference clock input
6	PCLKO	O	LVPECL	LVPECL clock output
7	PCLKO	O	LVPECL	LVPECL clock output
23, 22	QA[1,0]	O	LVCMOS	Bank A, LVCMOS clock outputs
14, 15, 18, 19	QB[3:0]	O	LVCMOS	Bank B, LVCMOS clock outputs
12	CLRDIV	I, PD	LVCMOS	Clear divider input. See functional *Table 1*
9	OE	I, PD	LVCMOS	Output enable/disable input. See functional *Table 1*
1, 5, 10, 16, 20, 24	VDD	Supply	VDD	2.5V power supply[2]
4, 8, 11, 13, 17, 21	VSS	Supply	Ground	Common ground

Table 1. Functional Table

Control	Default	0	1
CLRDIV	0	Bank A = ÷4, Bank B = ÷2	Bank A = ÷1, Bank B = ÷1
$\overline{OE}$	0	All outputs are enabled	All outputs are three-stated

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}	DC Supply Voltage		–0.5	3.3	V
V_{DD}	DC Operating Voltage	Functional	2.375	2.625	V
V_{IN}	DC Input Voltage	Relative to V_{SS}, with or V_{DD} applied	–0.5	V_{DD} + 0.5	V
V_{OUT}	DC Output Voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	V
V_{TT}	Output termination Voltage	LVCMOS outputs	V_{DD} / 2		V
		LVPECL output	V_{DD} – 2		
LU	Latch Up Immunity	Functional	200	–	mA
R_{PS}	Power Supply Ripple	Ripple Frequency < 100 kHz	–	150	mVp-p
T_S	Temperature, Storage	Non-functional	–65	+150	°C
T_A	Temperature, Operating Ambient	Functional	0	+85	°C
T_J	Temperature, Junction	Functional	–	+150	°C
$Ø_{JC}$	Dissipation, Junction to Case	Functional	–	42	°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	Functional	–	105	°C/W
ESD_H	ESD Protection (Human Body Model)		2000	–	V
FIT	Failure in Time	Manufacturing test	10		ppm

Notes:

1. PU = Internal pull up, PD = Internal pull down.
2. A 0.1-uF bypass capacitor should be placed as close as possible to each positive power pin (< 0.2”). If these bypass capacitors are not close to the pins their high frequency filtering characteristics will be cancelled by the lead inductance of the trace.

DC Electrical Specifications (V_{DD} = 2.5V ± 5%, T_A = 0°C to +85°C)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V_{PP}	Input Peak-Peak Voltage	PCLKI, $\overline{PCLKI}$	250	–	V_{DD} – 1.3	mV
V_{CMR}	Input Common Mode Range	PCLKI, $\overline{PCLKI}$	1.0	–	V_{DD} – 0.6	V
V_{IL}	Input Voltage, Low	OE, CLRDIV	–0.30	–	0.7	V
V_{IH}	Input Voltage, High		1.7	–	V_{DD} + 0.3	V
V_{OL}	Output Voltage, Low	PCLKO, $\overline{PCLKO}$, 50Ω to V_{TT}	0.2	–	0.8	V
V_{OH}	Output Voltage, High	PCLKO, $\overline{PCLKO}$, 50Ω to V_{TT}	V_{DD} – 1.2	–	V_{DD} – 0.4	V
V_{OL}	Output Voltage, Low [3]	I_{OL} = 16 mA, QA, QB	–0.3	–	0.6	V
V_{OH}	Output Voltage, High[3]	I_{OH} = –16 mA, QA, QB	1.8	–	V_{DD} + 0.3	V
I_{IL}	Input Current, Low[4]	V_{IL} = V_{SS}	–	–	–20	µA
I_{IH}	Input Current, High[4]	V_{IH} = V_{DD}	–	–	100	µA
I_{DDQ}	Quiescent Supply Current	V_{IN} = 0V, outputs disabled	–	2.5	3.5	mA
I_{DD}	Dynamic Supply Current	Outputs loaded @ 250 MHz	–	250	–	mA
C_{IN}	Input Pin Capacitance		–	4	–	pF
C_{OUT}	Output Pin Capacitance		–	4	–	pF
Z_{OUT}	Output Impedance	QA, QB	–	25	–	Ω

AC Electrical Specifications (V_{DD} = 2.5V ± 5%, T_A = 0°C to +85°C) [5, 6]

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
f_{in}	Input Frequency	CLRDIV = 0	0	–	320	MHz
		CLRDIV = 1	–	–	250	
V_{PP}(AC)	Input Peak-Peak Voltage	PCLKI, $\overline{PCLKI}$	500	–	1000	mV
V_{CMR}(AC)	Input Common Mode Range	PCLKI, $\overline{PCLKI}$	1.2	–	V_{DD} – 0.6	V
f_{refDC}	Reference Input Duty Cycle		40	–	60	%
f_{max}	Output Frequency	PCLKO, $\overline{PCLKO}$	0	–	320	MHz
		Bank B, CLRDIV = 0	0	–	160	
		Bank A, CLRDIV = 0	–	–	80	
		Bank A, Bank B, CLRDIV = 1	–	–	250	
t_r, t_f	Output Rise/Fall Time	20% to 80%, PCLKO, $\overline{PCLKO}$	200	–	700	ps
		0.6V to 1.8V, QA, QB	0.1	–	1.2	ns
DC	Output Duty Cycle, DC_{REF} = 50%	Bank A/Bank B	45	–	55	%
		LVPECL Output, fmax < 300 MHz	45	–	55	
		LVPECL Output, fmax > 300 MHz	40	–	60	
$t_{sk(O)}$	Output-to-Output Skew	Skew within Bank	–	50	75	ps
		BankA to BankB Skew	–	150	200	
		PECL Output to all Banks Skew	–	200	250	
T_{PLH}	Propagation Delay	PCLKI to PCLKO	–	–	7	ns
		PCLKI to QA/QB	–	–	7	
T_{PHL}	Propagation Delay	PCLKI to PCLKO	–	–	7	ns
		PCLKI to QA/QB	–	–	7	
t_{Qoff}	Output Disable Time	$\overline{OE}$ to any output	–	3	6	ns
t_{Qon}	Output Enable Time	$\overline{OE}$ to any output	–	3	6	ns
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	LVPECL output	–	|30|	|75|	ps
		LVTTL output	–	–	|50|	

Notes:

3. Driving 50Ω parallel terminated transmission line to a termination voltage of V_{TT}.
4. Inputs have pull-down resistors that affect the input current.
5. AC characteristics apply for parallel output termination to V_{TT}. Parameters are guaranteed by characterization and are not 100% tested.
6. AC test are measured with f_{in} = 250 MHz at VDD/2 unless otherwise specified.

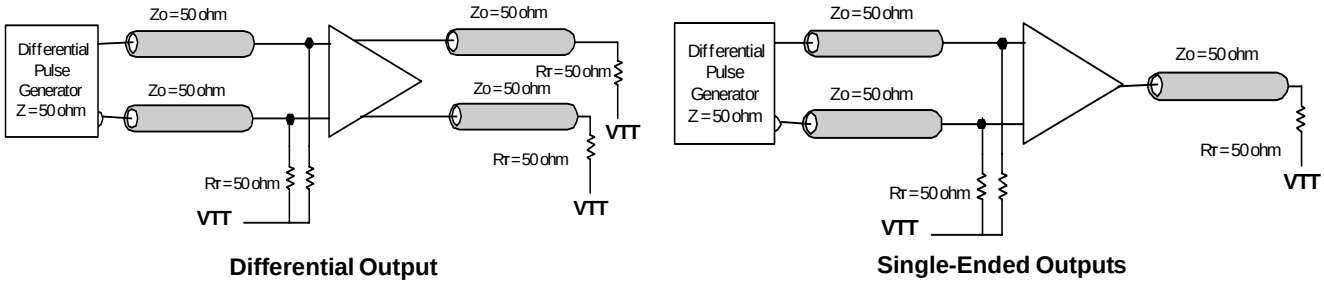


Figure 1. CY2PD817 Test Reference

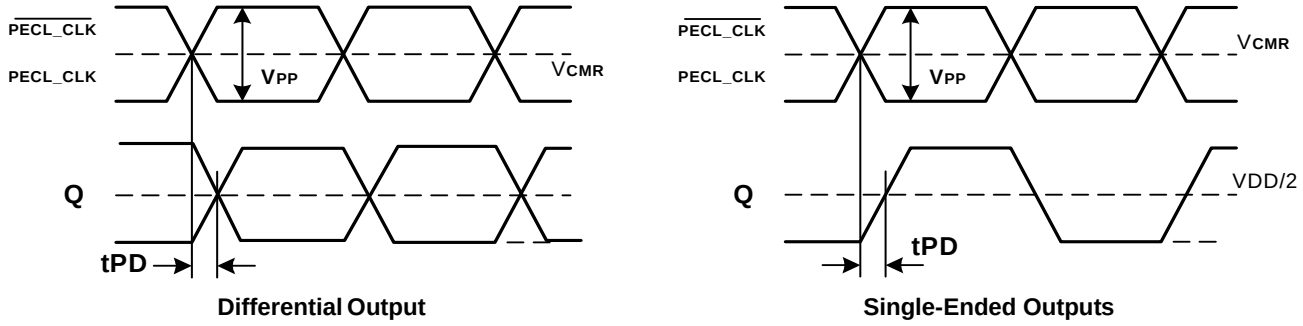


Figure 2. Propagation Delay (TPD) Test Reference

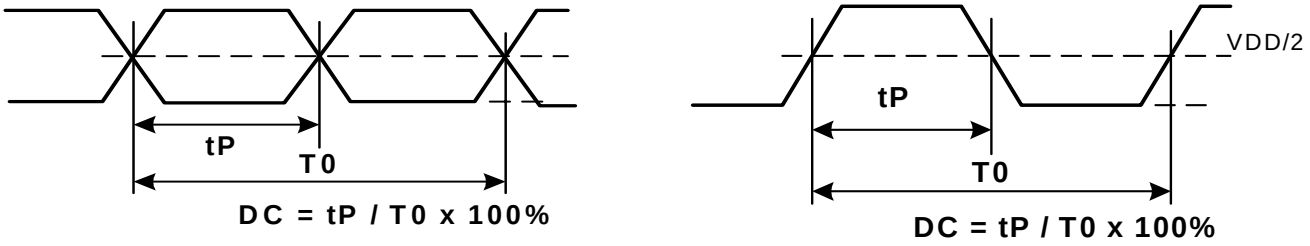


Figure 3. Output Duty Cycle

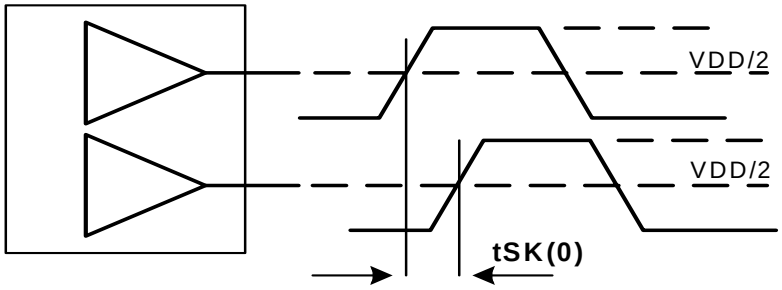


Figure 4. Output-Output Skew

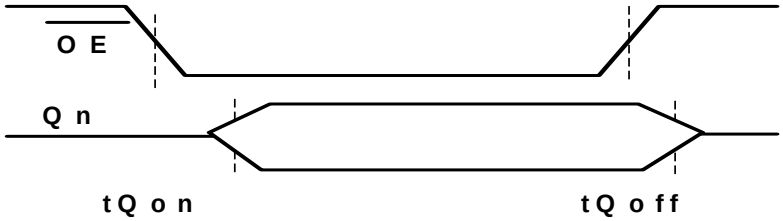


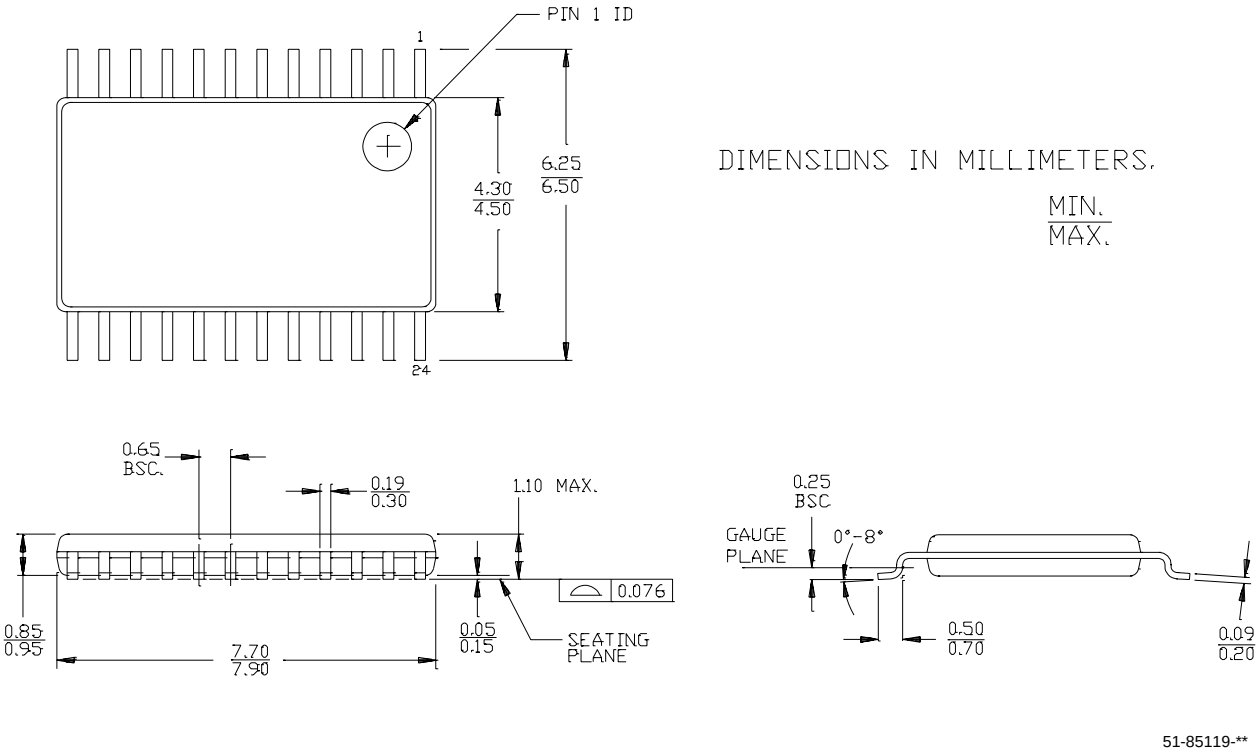
Figure 5. Output Enable/Disable Time

Ordering Information

Part Number	Package Type	Product Flow
CY2PD817ZC	24-pin TSSOP	Commercial, 0°C to +85°C
CY2PD817ZCT	24-pin TSSOP – Tape and Reel	

Package Drawing and Dimensions

24-lead Thin Shrunk Small Outline Package (4.40-mm Body) Z24



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Document History Page

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REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	129024	08/29/03	RGL	New Data Sheet