Application Note

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Connecting an MSC8102 TDM to a Time-Slot Interchange Switching Device

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CONTENTS

The MSC8102 time-division multiplex (TDM) interface enables many devices to communicate over a single bus. Traffic is managed according to a TDM method in which only one device drives the bus (transmit) for each channel. Each active device drives its active transmit channels and samples its active receive channels. It is the system designer's responsibility to guarantee that there is no conflict in transmit channel allocation. The TDM interface consists of four identical and independent TDM modules, each supporting 256 channels running at up to 50 Mbps with 2,4, 8, and 16-bit word size. The TDM bus connects gluelessly to most T1/E1 frames as well as to common buses such as the H.110, SCAS, and MVIP.

This document presents a test set-up example in which one MSC8102 TDM is connected to a time-slot interchange device (TSI), in this case, the Infineon PEF24471. There are two data links per channel, each with its own transmit and receive lines, thus doubling the amount of data that can be driven through the system. This application note first describes the physical interface between the MSC8102 and the Infineon PEF24471 (TSI) switching device and then it explains how to configure one MSC8102 TDM module and the TSI.

1 MSC8102 TDM to TSI Interface

An E1 interface is implemented using 32 × 64 Kbps slots, yielding a 2.048 Mbps bandwidth. **Figure 1** shows MSC8102 TDM0 connected to ports 0 and 1 on the PEF24471 switching device. The TDM interface is simple, consisting of a common clock for receive and transmit, a synchronization signal, and data signals. The MSC8102 device receives clock (TDM0TCLK) and synchronization signals (TDM0TSYN) from the PEF24471 device. The MSC8102 transmits data to the PEF24471 device through ports TDM0TDAT and TDM0RCLK, and it receives data through ports TDM0RDAT and TDM0RSYN. An internal loopback is achieved by setting CDR2 in the PEF24471 device to as value of 0x15 so that port IN0 connects to port OUT0 and port IN1 connects to port OUT1, as shown in **Figure 1**.

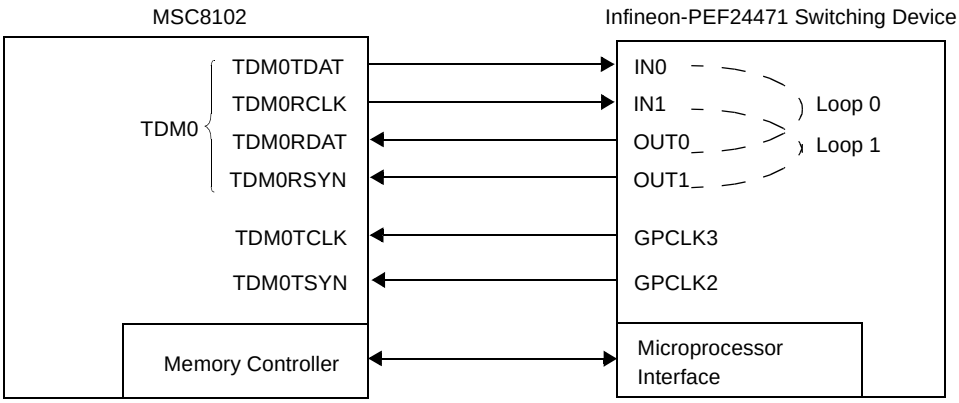
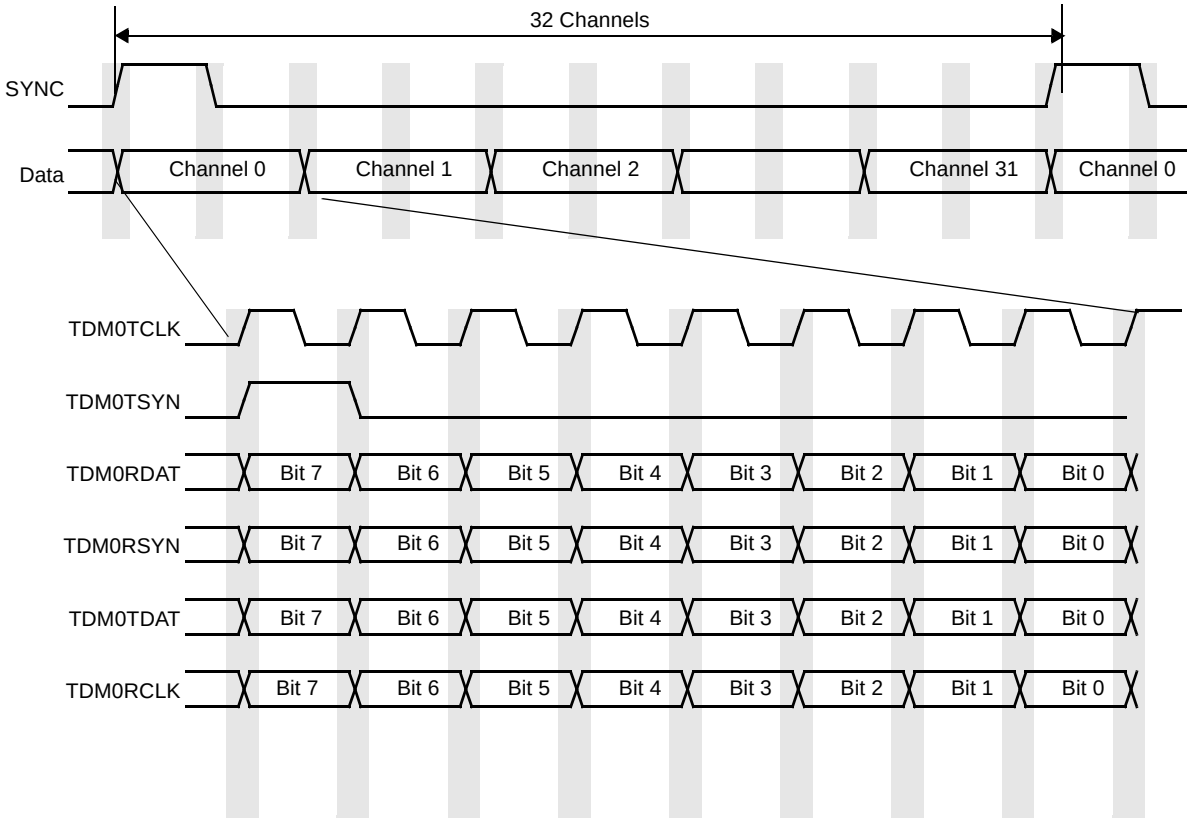


Figure 1. MSC8102 to PEF24471(TSI) Interface

The E1 frame is delimited by the switching (TSI) synchronization signal (GPCLK2) that marks the start of the first time slot in the frame and by a clock (GPCLK3) that controls the data bit rate.The E1 frame is split into multiple time slots, each designated for a different logical channel. **Figure 2** illustrates an E1 frame, consisting of thirty-two 8-bit logical channels.



Note: TDM0RCLK,TDM0RSYN,TDM0TDATA, and TDM0RDAT ports function as data links.

Figure 2. E1 Data Frame

1.1 Configuring the MSC8102 TDM

The overall steps in initializing an MSC8102 TDM are as follows:

1. Initialize the configuration registers to define the basic interface between the external device and the MSC8102 TDM.
2. Initialize the channel parameter registers to determine the channel type (A-law, μ–law, or transparent) and the buffer location of each channel.

   The channel parameter register values can change during TDM operation.
3. Initialize the control registers.
4. Clear the event registers (TDMxRER, TDMxTER).
5. Configure the external interface:

   a. Set up the parallel I/O pins.

   b. Enable the TDM.

This section presents the register settings to complete these steps. For the example presented here,

1.2 Configuration Registers

Table 1 describes the TDM configuration registers that define the interface between the MSC8102 device and the TSI. The configuration register settings determine the signal polarity, timings, and device functionality. The TDM clocks are always driven from an external source. In our example, the clock is driven from the TDM0TCLK port (the receive and transmit shared clock and sync signals). The reference clock is input to these pins from the TSI. The synchronization signals can be supplied from external source, or they can be generated internally in the TDM module. The TDMxTIR[18]:TSO field determines the transmit sync direction. Here, the TSI provides the sync, and it connects to the TDM0TSYN port because the receiver and transmitter share sync and clock signals (TDMxGIR[28–31]:RTSAL = 01).

Table 1. Receive/Transmit Interface Registers

Bit Setting	Description
TDM0GIR[28–31]:RTSAL = 0x5	The receive and transmit have a common clock and sync. The TDM receives two data links (TDM0RDAT and TDM0RSYN) and transmits two data links (TDM0TDAT and TDM0RCLK).
TDM0GIR[27]:CTS = 0x0	TDM0 does not share signals with the other TDM modules
TDM0RIR[26–27]:RFSD = 0x0	There is no clock delay between the first bit of the receive frame and the synchronization signal.
TDM0RIR[28]:RSL = 0x0	TDM0TSYN is an active high signal and is common for receive and transmit.
TDM0RIR[29]:RDE = 0x0	The receive data signals (TDM0RDAT and TDM0RSYN) are sampled at the rising edge of TDM0TCLK.
TDM0RIR[30]:RFSE = 0x1	The TDM0TSYN signal is sampled at the falling edge of TDM0TCLK.
TDM0RIR[31]:RRDO = 0x0	The MSB bit is received first.
TDM0TIR[26–27]:TFSD = 0x1	There is no clock delay between the first bit of the transmit frame and the synchronization signal.
TDM0TIR[28]:TSL = 0x0	TDM0TSYN is an active high signal and is common for receive and transmit.
TDM0TIR[29]:TDE = 0x1	The transmit data signals (TDM0TDAT and TDM0RCLK) are driven out at the falling edge of TDM0TCLK.
TDM0TIR[30]:TFSE = 0x1	The TDM0TSYN signal is sampled at the falling edge of TDM0TCLK.
TDM0TIR[31]:TRDO = 0x0	The MSB bit is transmitted first.
TDM0TIR[18]:TSO = 0x0	TDM0TSYN is an input
TDM0TIR[19]:TAO = 0x1	The TDM transmitter drives the TDMxDAT, regardless of whether the channel is active. That is, the TDM outputs are always active (never tri-stated).
Register Setting Summary:	TDM0GIR = 0x00000005, TDM0RIR = 0x00010002, TDM0tIR = 0x00011016

The E1 frame contains thirty-two 8-bit channels. The TDM has two data links for receive operations and two links for transmit operations. Each link transfers 32 channels, so the RNCF/TNCF field is set to 64 channels. **Table 2** shows the settings for the Receive Frame Paramter Register (TDM0RFP). The Transmit Frame Parameter Register (TDM0TFP) is identical to TDM0RFP because the receiver and transmitter operate in sharing mode.

Table 2. Receive Frame Parameter Register (TDM0RFP) Settings

Bits fields Setting	Description
TDM0RFP[8–15]:RNCF = 0X3F	64 receive channels (32 channels per data link).
TDM0RFP[21–23]:RCDBL = 0x1	Receive data buffer latency is 128 bits.

Table 2. Receive Frame Parameter Register (TDM0RFP) Settings (Continued)

Bits fields Setting	Description
TDM0RFP[26–29]:RCS = 0X7	Receive channel size is 8 bits.
TDM0RFP[30]:RT1 = 0X0	The receive frame is not T1 frame (E1 frame).
TDM0RFP[31]:RUBM = 0X0	The receiver functions in regular mode.
Register Setting Summary:	TDM0RFP = 0x003F011C,TDM0TFP = 0x003F011C

Memory resource can become scarce as the number of TDM channels increases. The size of the data buffers should suit the protocol and the number of active channels. The data buffers of a TDM channel can be located in the M1 memory of the SC140 cores and in M2 memory. The location of each data buffer is independent and is indicated in the Receive/Transmit Channel Parameter Registers (RCPRn). The data buffer size is identical for all receive channels belonging to a TDM module and is indicated by the TDMx[8–31]:RDBS field. The transmit buffer size is also identical for all the transmit channels belonging to a TDM module and is indicated by the TDMxTDBS[8–31]:TDBS field. field. In this example, the data buffers are located in M2 memory, and the size of each buffer is 64 bytes.

The receive data buffer base address is a function of the following:

- Receive Global Base Address. TDMxRGBA[16–31]:RGBA field.
- Receive Channel Data Base Address. TDMxRCPRn[8–31]:RCDBA field.

  Receive data buffer n =RGBA >> 16 + RCDBA

The transmit data buffer base address is a function of the following:

- Transmit Global Base Address. TDMxTGBA[16–31]:TGBA field.
- Transmit Channel Data Base Address. TDMxTCPRn[8–31]:TCDBA field.

  Transmit data buffer n =TGBA >> 16 + TCDBA

Note: The data buffer base address is in the local bus address space.

For example, if the transmit data buffer of channel *n* is located at the first byte of M2 (address at the local bus space = 0x2000000), then the following is true:

- Transmit Global Base Address. TDMxTGBA[16–31]:TGBA = 0x200.
- Transmit Channel Data Base Address. TDMxTCPRn[8–31] = 0x0.

Table 3. Receive/Transmit Data Buffer Registers

Bit Setting	Description
TDM0RDBS[8–31]:RDBS = 0x00003F	The receive data buffer size is 64 bytes.
TDM0TDBS[8–31]:TDBS = 0x00003F	The transmit data buffer size is 64 bytes.
TDM0RGBA[16–31]:RGBA = 0x00000200	The receive global base address points to the start of the local bus memory map (M2).
TDM0TGBA[16–31]:TGBA = 0x00000200	The transmit global base address points to the start of the local bus memory map (M2).
Register Setting Summary:	TDM0RDBS = 0x0000003F, TDM0TDBS = 0x0000003F, TDM0RGBA = 0x00000200, TDM0TGBA = 0x00000200

1.3 Channel Parameter Registers

The channel parameter registers determine the parameters of each channel, such as the buffer location, channel type, and channel activation. Channels that are not used should be clear. In this example the receive and transmit TDM buffers reside in M2 memory in consecutive order and all the channels are active and transparent. **Table 4** describe the receive and transmit channel parameter registers.

Table 4. Receive/transmit Channel Parameter Registers

Register Setting	Description
TDM0RCPR0 = 0x80000000	The receive data buffer of channel 0 is located at an offset of 0 (refer to the TDMx Receive Global Base Address Register, TDMxRGBA[16–31]:RGBA field). The data buffer address is 0x200000 (local memory address space).
TDM0RCPR1 = 0x80000040	The receive data buffer of channel 1 is located at an offset of 64 bytes (refer to the TDMxRGBA[16–31]:RGBA field). The data buffer address is 0x200040 (local memory address space).
TDM0RCPR2 = 0x80000080	The receive data buffer of channel 2 is located at an offset of 128 bytes (refer to the TDMxRGBA[16–31]:RGBA field). The data buffer address is 0x200080 (local memory address space).
:	
TDM0RCPR63 = 0x80000FC0	The receive data buffer of channel 63 is located at address 0x200FC0 (local memory address space).
TDM0TCPR0 = 0x80001000	The transmit data buffer of channel 0 is located at an offset of 4096 bytes (refer to the TDMx Transmit Global Base Address Register, TDMxTGBA[16–31]:TGBA field). The address of transmit channel 0 is 0x201000 (local memory address space).
TDM0TCPR1 = 0x80001040	The transmit data buffer of channel 1 is located at an offset of 4160 bytes (refer to the TDMxTGBA[16–31]:TGBA field). The address of transmit channel 1 is 0x201040 (local memory address space).
TDM0TCPR2 = 0x80001080	The transmit data buffer of channel 3 is located at address 0x201080 (local memory address space).
TDM0TCPR31 = 0x80001FC0	The transmit data buffer of channel 63 is located at address 0x201FC0 (local memory address space).
Note: All the receive and transmit channels are active and transparent.	

1.4 Control Registers

The control registers set the threshold pointers and enable TDM events. The threshold registers determine the offset in the data buffers that cause interrupts to be generated. Here, the receive first threshold interrupt is generated when the first half of the buffer is filled with new data, and the second receive threshold interrupt is generated when the second half of the buffer is full. The transmit first threshold interrupt is generated when the TDM reads the first half of the buffer, and the second threshold interrupt is generated when the TDM reads the second half of the buffer. The TDM0RIER and TDM0TIER registers enable interrupt generation, and a value of zero written into the appropriate field disables interrupt generation.

Table 5. Receive and Transmit Threshold Registers

Bits fields Setting	Description
TDM0TDBFT[8–31]:TDBFT = 0x000018	The transmit first threshold interrupt is generated when the first half of the data buffer is empty.

Table 5. Receive and Transmit Threshold Registers (Continued)

Bits fields Setting	Description
TDM0TDBST[TDBST] = 0x000038	The transmit second threshold interrupt is generated when the second half of the data buffer is empty.
TDM0RDBFT[RDBFT] = 0x000018	The receive first threshold interrupt is generated when the first half of the data buffer is full.
TDM0RDBST[RDBST] = 0x000038	The receive second threshold interrupt is generated when the second half of the data buffer is full
Register Setting Summary:	TDM0RDBFT = 0x00000018, TDM0RDBST = 0x00000038, TDM0TDBFT = 0x00000018, TDM0TDBST = 0x00000038

1.5 External Interface

The TDM interface is essentially a set of I/O pins that can configured for either a peripheral or a general-purpose function. The multiplexed peripheral pins for the TDM configured through the parallel I/O registers (PSOR, PDIR, and PAR).

Table 6. Parallel I/O Registers

Register Setting	Description
PSOR = 0x07B00000	TDM0TSYN,TDM0TDAT,TDM0TDAT,TDM0RDAT, and TDM0RSYN ports are dedicated peripheral functions.
PODR = 0x00000000	All the I/O ports are actively driven as outputs.
PDIR = 0x00000000	All the I/O ports counteract as inputs (the TDM determines the direction of the port).
PAR = 0x07F00000	TDM0TSYN,TDM0TDAT,TDM0TDAT,TDM0RDAT,TDM0RSYN, and TDM0TCLK ports are dedicated peripheral ports.

1.6 TDM Activation

TDM0 is enabled as follows:

- Reset the event registers (TDM0RER and TDM0TER) by writing a value of 0x32xF to these registers
- Activate the receiver and transmitter by setting the TDM0RCR and TDM0TCR register to 32x1.

2 Configuring the PEF24471 (TSI)

An E1 interface is implemented between the MSC8102 TDM and the Infineon-PEF24471 TSI modules. The TSI is configured to supply a clock frequency of 2.048 MHz and a frame sync frequency of 8 KHz. The IN0 port is connected internally to OUT and port IN1 is connected internally to OUT1.The write and read to/from the TSI occurs via the memory controller port. The read and the write access is a standard 8-bit microprocessor interface. **Table 7** shows the steps in configuring the TSI.

Table 7. TSI Configuration

Description	Register Setting
Set the external frequency to 16 MHz.	Write a value of 0x51 to CMDR2.
Wait 800 ns.	Read ISTA1, which should contain a value of 0x81.

Table 7. TSI Configuration

Description	Register Setting
Set PDC and PFC as outputs. The PDC frequency is 2.048 MHz	Write a value of 0x96 to CMDR2.
Define GPCLK2 as a frame sync.	Write a value of 0x0 to GI1. Write a value of 0xE0 to GI2. Write a value of 0x26 to CMD2.
Define a s clock of frequency of 2.048 MHz for GPCLK3.	Write a value of 0x01 to GI1. Write a value of 0x37 to CMD2.
Configure all the GPIO signals as outputs	Write a value of 0x00 to GPPO. Write a value of 0xFF to GPD.
Select PCM master mode.	Write a value of 0x14 to CMD2.
Enable loopbacks in the PCM lines. Loopbacks are used for testing. In real applications, a different connection is defined.	Write a value of 0x15 to CMD2.

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