

## 1:4 LVPECL Fanout Buffer with Selectable Clock Input

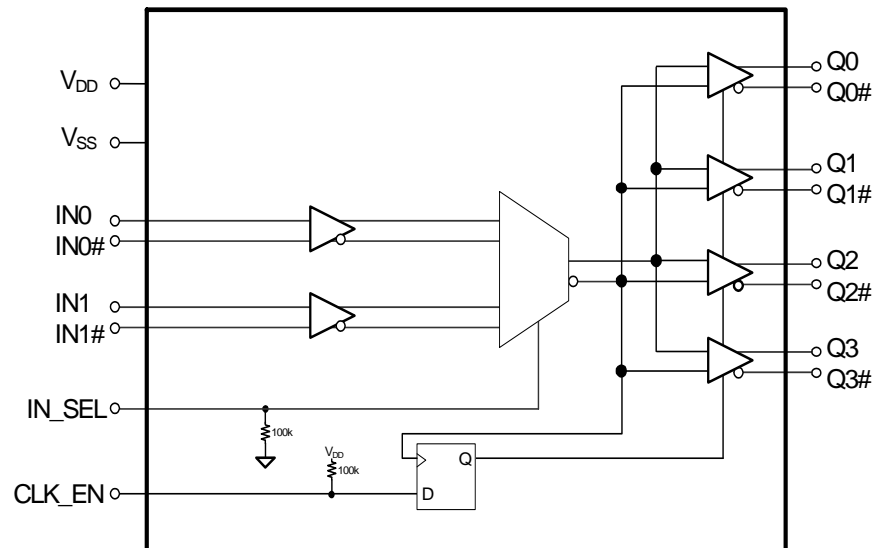
### Features

- Select one of two low-voltage positive emitter-coupled logic (LVPECL) input pairs to distribute to four LVPECL output pairs
- 30 ps maximum output-to-output skew
- 480-ps maximum propagation delay
- 0.15-ps maximum additive RMS phase jitter at 156.25 MHz (12-kHz to 20-MHz offset)
- Up to 1.5-GHz operation
- Synchronous clock enable function
- 20-pin thin shrunk small outline package (TSSOP)
- 2.5-V or 3.3-V operating voltage<sup>[1]</sup>
- Commercial and industrial operating temperature range

### Functional Description

The CY2DP1504 is an ultra-low noise, low-skew, low-propagation delay 1:4 LVPECL fanout buffer targeted to meet the requirements of high-speed clock distribution applications. The CY2DP1504 can select between two separate LVPECL input clock pairs using the IN\_SEL pin. The synchronous clock enable function ensures glitch-free output transitions during enable and disable periods. The device has a fully differential internal architecture that is optimized to achieve low additive jitter and low skew at operating frequencies of up to 1.5 GHz.

### Logic Block Diagram



#### Note

1. Input AC-coupling capacitors are required for voltage-translation applications.

## Contents

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Pinouts

Figure 1. Pin Diagram – 20-Pin TSSOP Package

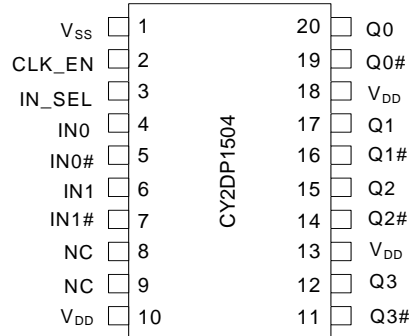


Table 1. Pin Definitions

| Pin No.     | Pin Name        | Pin Type | Description   |
|-------------|-----------------|----------|---|
| 1           | V <sub>SS</sub> | Power    | Ground  |
| 2           | CLK_EN          | Input    | Synchronous clock enable. Low-voltage complementary metal oxide semiconductor (LVCMOS)/low-voltage transistor-transistor-logic (LVTTTL). When CLK_EN = Low, Q(0:3) outputs are held Low and Q(0:3)# outputs are held High |
| 3           | IN_SEL          | Input    | Input clock select pin. LVCMOS/LVTTTL;<br>When IN_SEL = Low, the IN0/IN0# differential input pair is active<br>When IN_SEL = High, the IN1/IN1# differential input pair is active   |
| 4           | IN0             | Input    | LVPECL input clock. Active when IN_SEL = Low  |
| 5           | IN0#            | Input    | LVPECL complementary input clock. Active when IN_SEL = Low  |
| 6           | IN1             | Input    | LVPECL input clock. Active when IN_SEL = High   |
| 7           | IN1#            | Input    | LVPECL complementary input clock. Active when IN_SEL = High   |
| 8,9         | NC              |          | No connection   |
| 10,13,18    | V <sub>DD</sub> | Power    | Power supply  |
| 11,14,16,19 | Q(0:3)#         | Output   | LVPECL complementary output clocks  |
| 12,15,17,20 | Q(0:3)          | Output   | LVPECL output clocks  |

## Absolute Maximum Ratings

| Parameter       | Description   | Condition           | Min   | Max                             | Unit |
|-----------------|---|---------------------|---|---------------------------------|------|
| $V_{DD}$        | Supply voltage  | Nonfunctional       | -0.5  | 4.6                             | V    |
| $V_{IN}^{[2]}$  | Input voltage, relative to $V_{SS}$                         | Nonfunctional       | -0.5  | lesser of 4.0 or $V_{DD} + 0.4$ | V    |
| $V_{OUT}^{[2]}$ | DC output or I/O voltage, relative to $V_{SS}$              | Nonfunctional       | -0.5  | lesser of 4.0 or $V_{DD} + 0.4$ | V    |
| $T_S$           | Storage temperature   | Non functional      | -55   | 150                             | °C   |
| $ESD_{HBM}$     | Electrostatic discharge (ESD) protection (Human body model) | JEDEC STD 22-A114-B | 2000  | -                               | V    |
| $L_U$           | Latch up  |                     | Meets or exceeds JEDEC Spec JESD78B IC Latchup Test |                                 |      |
| UL-94           | Flammability rating   | At 1/8 in           | V-0   |                                 |      |
| MSL             | Moisture sensitivity level                                  |                     | 3   |                                 |      |

## Operating Conditions

| Parameter | Description                   | Condition   | Min   | Max   | Unit |
|-----------|-------------------------------|---|-------|-------|------|
| $V_{DD}$  | Supply voltage                | 2.5-V supply  | 2.375 | 2.625 | V    |
|           |                               | 3.3-V supply  | 3.135 | 3.465 | V    |
| $T_A$     | Ambient operating temperature | Commercial  | 0     | 70    | °C   |
|           |                               | Industrial  | -40   | 85    | °C   |
| $t_{PU}$  | Power ramp time               | Power-up time for $V_{DD}$ to reach minimum specified voltage (power ramp must be monotonic). | 0.05  | 500   | ms   |

**Note**

2. The voltage on any I/O pin cannot exceed the power pin during power up. Power supply sequencing is not required.

## DC Electrical Specifications

( $V_{DD} = 3.3\text{ V} \pm 5\%$  or  $2.5\text{ V} \pm 5\%$ ;  $T_A = 0\text{ }^\circ\text{C}$  to  $70\text{ }^\circ\text{C}$  (Commercial) or  $-40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$  (Industrial))

| Parameter      | Description   | Condition  | Min             | Max             | Unit          |
|----------------|---|--|-----------------|-----------------|---------------|
| $I_{DD}$       | Operating supply current  | All LVPECL outputs floating (internal $I_{DD}$ )     | –               | 61              | mA            |
| $V_{IH1}$      | Input high voltage, LVPECL input clocks<br>IN0 and IN0#, IN1 and IN1# |  | –               | $V_{DD} + 0.3$  | V             |
| $V_{IL1}$      | Input low voltage, LVPECL input clocks<br>IN0 and IN0#, IN1 and IN1#  |  | –0.3            | –               | V             |
| $V_{IH2}$      | Input high voltage, CLK_EN, IN_SEL                                    | $V_{DD} = 3.3\text{ V}$                              | 2.0             | $V_{DD} + 0.3$  | V             |
| $V_{IL2}$      | Input low voltage, CLK_EN, IN_SEL                                     | $V_{DD} = 3.3\text{ V}$                              | –0.3            | 0.8             | V             |
| $V_{IH3}$      | Input high voltage, CLK_EN, IN_SEL                                    | $V_{DD} = 2.5\text{ V}$                              | 1.7             | $V_{DD} + 0.3$  | V             |
| $V_{IL3}$      | Input low voltage, CLK_EN, IN_SEL                                     | $V_{DD} = 2.5\text{ V}$                              | –0.3            | 0.7             | V             |
| $V_{ID}^{[3]}$ | Input differential amplitude  | See <a href="#">Figure 2</a> on page 7               | 0.4             | 1.0             | V             |
| $V_{ICM}$      | Input common mode voltage   | See <a href="#">Figure 2</a> on page 7               | 0.5             | $V_{DD} - 0.2$  | V             |
| $I_{IH}$       | Input high current, all inputs  | Input = $V_{DD}^{[4]}$                               | –               | 150             | $\mu\text{A}$ |
| $I_{IL}$       | Input low current, all inputs   | Input = $V_{SS}^{[4]}$                               | –150            | –               | $\mu\text{A}$ |
| $V_{OH}$       | LVPECL output high voltage  | Terminated with $50\ \Omega$ to $V_{DD} - 2.0^{[5]}$ | $V_{DD} - 1.20$ | $V_{DD} - 0.70$ | V             |
| $V_{OL}$       | LVPECL output low voltage   | Terminated with $50\ \Omega$ to $V_{DD} - 2.0^{[5]}$ | $V_{DD} - 2.0$  | $V_{DD} - 1.63$ | V             |
| $R_P$          | Internal pull-up/pull-down resistance,<br>LVCMOS logic inputs         | CLK_EN has pull-up only<br>IN_SEL has pull-down only | 60              | 140             | k $\Omega$    |
| $C_{IN}$       | Input capacitance   | Measured at 10 MHz; per pin                          | –               | 3               | pF            |

### Notes

- $V_{ID}$  minimum of 400 mV is required to meet all output AC Electrical Specifications. The device is functional with  $V_{ID}$  minimum of greater than 200 mV.
- Positive current flows into the input pin, negative current flows out of the input pin.
- Refer to [Figure 3](#) on page 7.

## AC Electrical Specifications

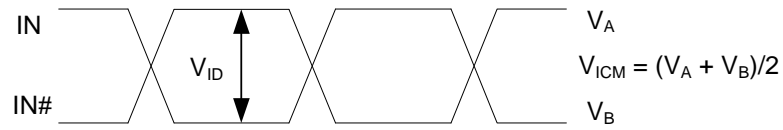
( $V_{DD} = 3.3\text{ V} \pm 5\%$  or  $2.5\text{ V} \pm 5\%$ ;  $T_A = 0\text{ }^\circ\text{C}$  to  $70\text{ }^\circ\text{C}$  (Commercial) or  $-40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$  (Industrial))

| Parameter                  | Description  | Condition   | Min | Typ | Max  | Unit   |
|----------------------------|--|---|-----|-----|------|--------|
| $F_{IN}$                   | Input frequency  |   | DC  | –   | 1.5  | GHz    |
| $F_{OUT}$                  | Output frequency   | $F_{OUT} = F_{IN}$  | DC  | –   | 1.5  | GHz    |
| $V_{PP}$                   | LVPECL differential output voltage peak to peak, single-ended. Terminated with $50\ \Omega$ to $V_{DD} - 2.0$ <sup>[6]</sup> | $F_{out} = \text{DC to } 150\text{ MHz}$  | 600 | –   | –    | mV     |
|                            |  | $F_{out} = >150\text{ MHz to } 1.5\text{ GHz}$  | 400 | –   | –    | mV     |
| $t_{PD}$ <sup>[7]</sup>    | Propagation delay input pair to output pair  | Input rise/fall time $< 1.5\text{ ns}$ (20% to 80%)   | –   | –   | 480  | ps     |
| $t_{ODC}$ <sup>[8]</sup>   | Output duty cycle  | 50% duty cycle at input<br>Frequency range up to 1 GHz  | 48  | –   | 52   | %      |
| $t_{SK1}$ <sup>[9]</sup>   | Output-to-output skew  | Any output to any output, with same load conditions at DUT  | –   | –   | 30   | ps     |
| $t_{SK1 D}$ <sup>[9]</sup> | Device-to-device output skew   | Any output to any output between two or more devices. Devices must have the same input and have the same output load.             | –   | –   | 150  | ps     |
| $PN_{ADD}$                 | Additive RMS phase noise<br>156.25 MHz Input<br>Rise/fall time $< 150\text{ ps}$ (20% to 80%)<br>$V_{ID} > 400\text{ mV}$    | Offset = 1 kHz  | –   | –   | –120 | dBc/Hz |
|                            |  | Offset = 10 kHz   | –   | –   | –130 | dBc/Hz |
|                            |  | Offset = 100 kHz  | –   | –   | –135 | dBc/Hz |
|                            |  | Offset = 1 MHz  | –   | –   | –145 | dBc/Hz |
|                            |  | Offset = 10 MHz   | –   | –   | –153 | dBc/Hz |
|                            |  | Offset = 20 MHz   | –   | –   | –155 | dBc/Hz |
| $t_{JIT}$ <sup>[10]</sup>  | Additive RMS phase jitter (Random)   | 156.25 MHz, 12 kHz to 20 MHz offset; input rise/fall time $< 150\text{ ps}$ (20% to 80%), $V_{ID} > 400\text{ mV}$                | –   | –   | 0.15 | ps     |
| $t_R, t_F$ <sup>[11]</sup> | Output rise/fall time  | 50% duty cycle at input, 20% to 80% of full swing ( $V_{OL}$ to $V_{OH}$ )<br>Input rise/fall time $< 1.5\text{ ns}$ (20% to 80%) | –   | –   | 300  | ps     |
| $t_{SOD}$                  | Time from clock edge to outputs disabled   | Synchronous clock enable (CLK_EN) switched Low  | –   | –   | 700  | ps     |
| $t_{SOE}$                  | Time from clock edge to outputs enabled  | Synchronous clock enable (CLK_EN) switched High   | –   | –   | 700  | ps     |

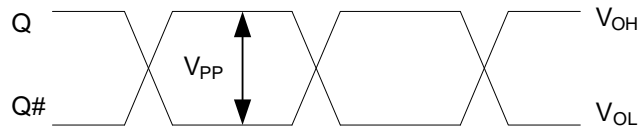
### Notes

6. Refer to Figure 3 on page 7.
7. Refer to Figure 4 on page 7.
8. Refer to Figure 5 on page 7.
9. Refer to Figure 6 on page 8.
10. Refer to Figure 7 on page 8.
11. Refer to Figure 8 on page 8.

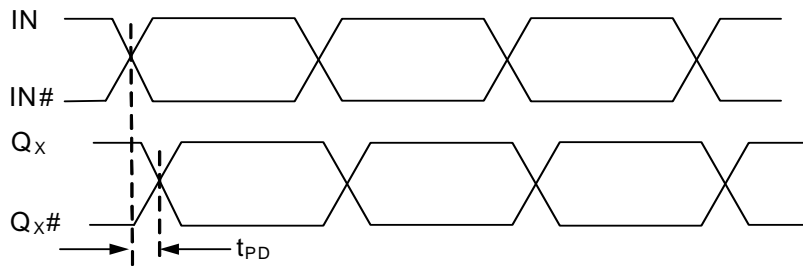
**Figure 2. Input Differential and Common Mode Voltages**



**Figure 3. Output Differential Voltage**



**Figure 4. Input to Any Output Pair Propagation Delay**



**Figure 5. Output Duty Cycle**

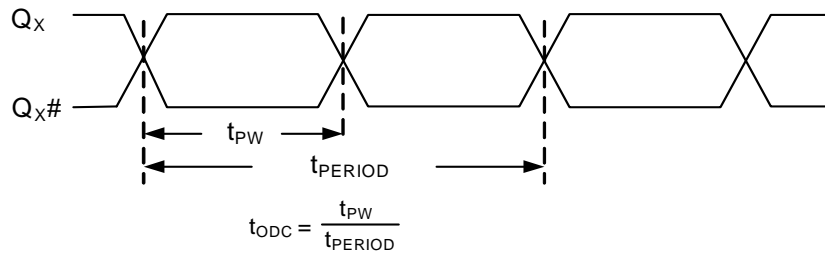


Figure 6. Output-to-Output and Device-to-Device Skew

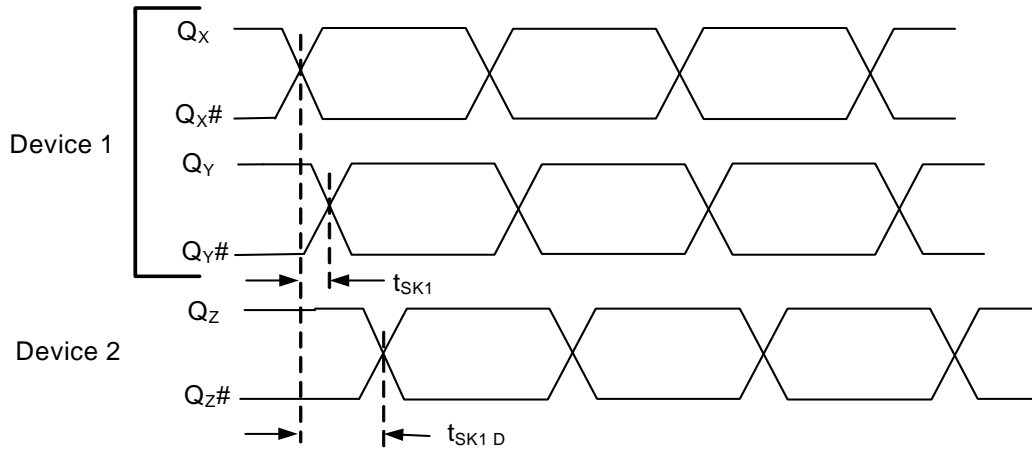


Figure 7. RMS Phase Jitter

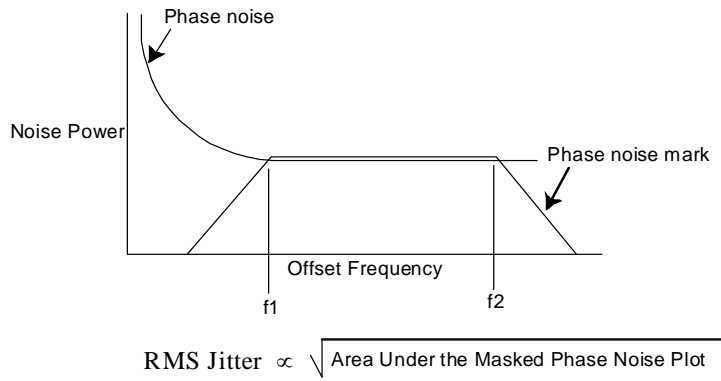


Figure 8. Output Rise/Fall Time

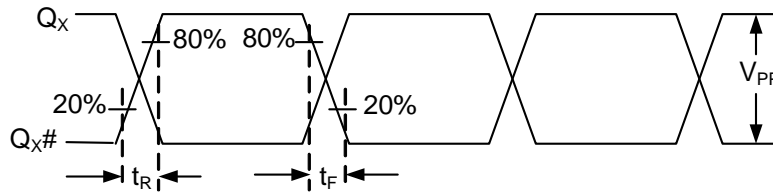
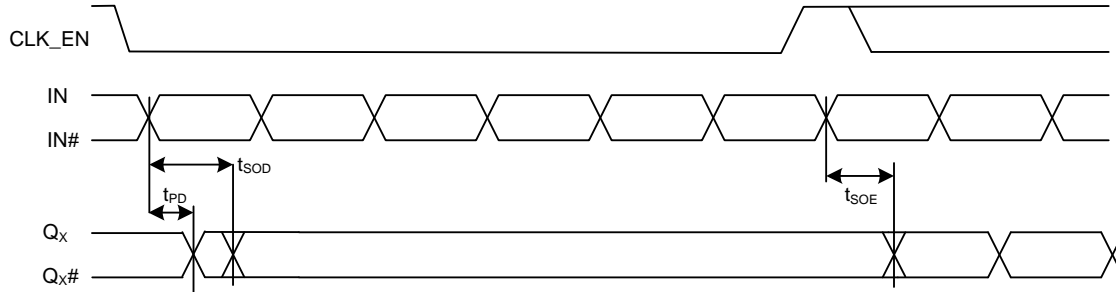




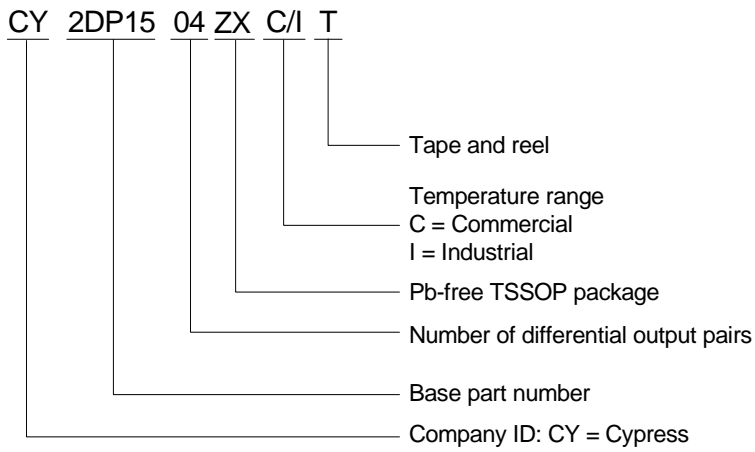
Figure 9. Synchronous Clock Enable Timing



### Ordering Information

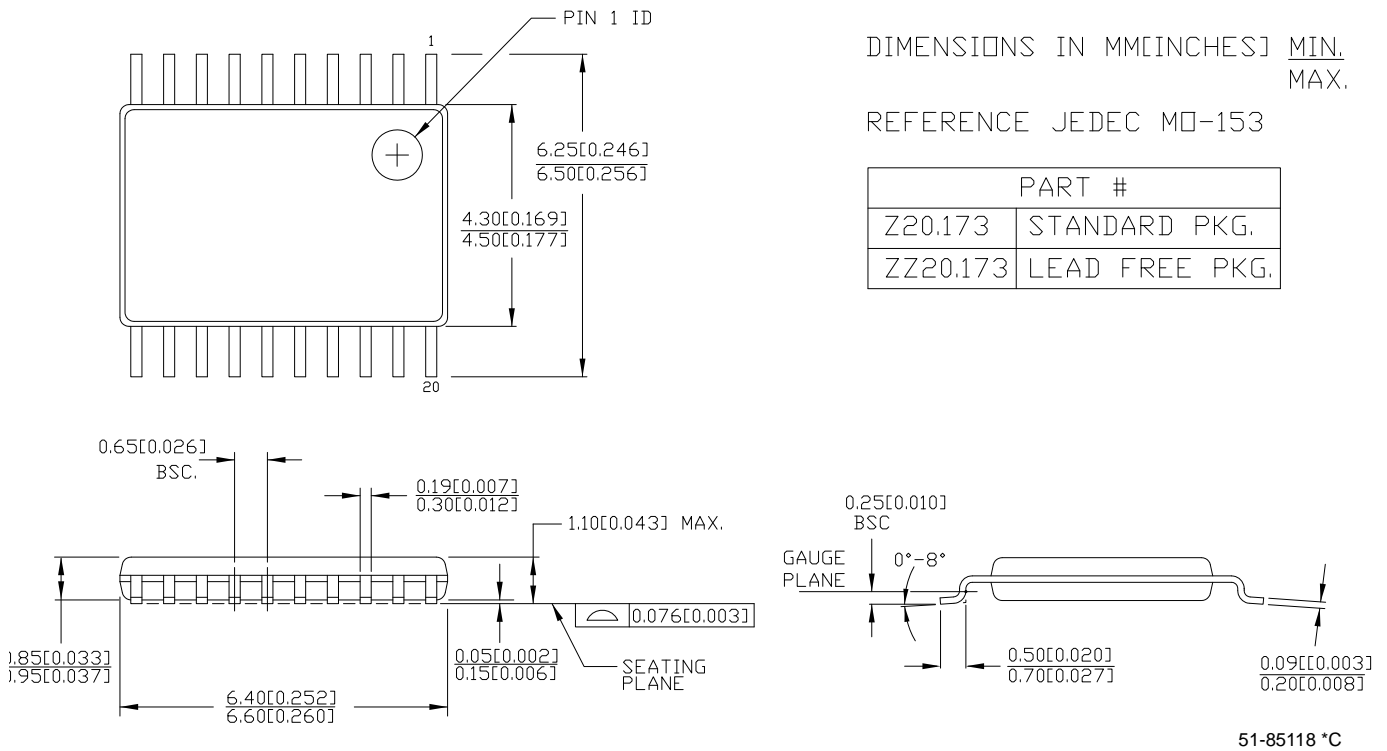
| Part Number    | Type                       | Production Flow             |
|----------------|----------------------------|-----------------------------|
| <b>Pb-free</b> |                            |                             |
| CY2DP1504ZXC   | 20-Pin TSSOP               | Commercial, 0 °C to 70 °C   |
| CY2DP1504ZXCT  | 20-Pin TSSOP tape and reel | Commercial, 0 °C to 70 °C   |
| CY2DP1504ZXI   | 20-Pin TSSOP               | Industrial, -40 °C to 85 °C |
| CY2DP1504ZXIT  | 20-Pin TSSOP tape and reel | Industrial, -40 °C to 85 °C |

### Ordering Code Definition



Package Dimension

Figure 10. 20-Pin Thin Shrink Small Outline Package (4.40 mm Body) ZZ20



## Acronyms

**Table 2. Acronyms Used in this Document**

| Acronym | Description   |
|---------|---|
| ESD     | electrostatic discharge                             |
| HBM     | human body model                                    |
| JEDEC   | Joint electron devices engineering council          |
| LVC MOS | low-voltage complementary metal oxide semiconductor |
| LVPECL  | low-voltage positive emitter-coupled logic          |
| LVTTTL  | low-voltage transistor-transistor logic             |
| OE      | Output enable                                       |
| RMS     | root mean square                                    |
| TSSOP   | thin shrunk small outline package                   |

## Document Conventions

**Table 3. Units of Measure**

| Symbol | Unit of Measure                  |
|--------|----------------------------------|
| °C     | degree Celsius                   |
| dBc    | decibels relative to the carrier |
| GHz    | giga hertz                       |
| Hz     | hertz                            |
| kΩ     | kilo ohm                         |
| μA     | microamperes                     |
| μF     | micro Farad                      |
| μs     | microsecond                      |
| mA     | milliamperes                     |
| ms     | millisecond                      |
| mV     | millivolt                        |
| MHz    | megahertz                        |
| ns     | nanosecond                       |
| Ω      | ohm                              |
| pF     | pico Farad                       |
| ps     | pico second                      |
| V      | volts                            |
| W      | watts                            |

Document History Page

| Document Title: CY2DP1504 1:4 LVPECL Fanout Buffer with Selectable Clock Input |         |                 |                 |  |
|--|---------|-----------------|-----------------|--|
| Document Number: 001-56215   |         |                 |                 |  |
| Revision   | ECN     | Orig. of Change | Submission Date | Description of Change  |
| **   | 2782891 | CXQ             | 10/09/09        | New Datasheet.   |
| *A   | 2838916 | CXQ             | 01/05/2010      | <p>Changed status from "ADVANCE" to "PRELIMINARY".</p> <p>Changed from 0.34 ps to 0.25 ps maximum additive jitter in "Features" on page 1 and in <math>t_{JIT}</math> in the AC Electrical Specs table on page 5.</p> <p>Added <math>t_{PU}</math> spec to the Operating Conditions table on page 3.</p> <p>Changed max <math>I_{DD}</math> spec in the DC Electrical Specs table on page 4 from 60 mA to 61 mA.</p> <p>Change <math>V_{OH}</math> in the DC Electrical Specs table on page 4: minimum from <math>V_{DD} - 1.15V</math> to <math>V_{DD} - 1.20V</math>; maximum from <math>V_{DD} - 0.75V</math> to <math>V_{DD} - 0.70V</math>.</p> <p>Removed <math>V_{OD}</math> spec from the DC Electrical Specs table on page 4.</p> <p>Added <math>R_P</math> spec in the DC Electrical Specs table on page 4. Min = 60 k<math>\Omega</math>, Max = 140 k<math>\Omega</math>.</p> <p>Added a measurement definition for <math>C_{IN}</math> in the DC Electrical Specs table on page 4.</p> <p>Added <math>V_{PP}</math> spec to the AC Electrical Specs table on page 5. <math>V_{PP}</math> min = 600 mV for DC - 150 MHz and min = 400 mV for 150 MHz to 1.5 GHz.</p> <p>Changed letter case and some names of all the timing parameters in the AC Electrical Specs table on page 5 to be consistent with EROS.</p> <p>Lowered all additive phase noise mask specs by 3 dB in the AC Electrical Specs table on page 5.</p> <p>Added condition to <math>t_R</math> and <math>t_F</math> specs in the AC Electrical specs table on page 5 that input rise/fall time must be less than 1.5 ns (20% to 80%).</p> <p>Changed letter case and some names of all the timing parameters in Figures 3, 4, 5, 6 and 8, to be consistent with EROS.</p> |
| *B   | 3011766 | CXQ             | 08/20/2010      | <p>Changed maximum additive jitter from 0.25 ps to 0.11 ps in "Features" on page 1 and in <math>t_{JIT}</math> in the AC Electrical Specs table.</p> <p>Added note 3 to describe <math>I_{IH}</math> and <math>I_{IL}</math> specs.</p> <p>Removed reference to data distribution from "Functional Description".</p> <p>Changed <math>R_P</math> for differential inputs from 100 k<math>\Omega</math> to 150 k<math>\Omega</math> in the Logic Block Diagram and from 60 k<math>\Omega</math> min / 140 k<math>\Omega</math> max to 90 k<math>\Omega</math> min / 210 k<math>\Omega</math> max in the DC Electrical Specs table.</p> <p>Added max <math>V_{ID}</math> of 1.0V in DC Electrical Specs table.</p> <p>Updated phase noise specs for 1 k/10 k/100 k/1 M/10 M/20 MHz offset to -120/-130/-135/-150/-150/-150dBc/Hz, respectively, in the AC Electrical Specs table.</p> <p>Added "Frequency range up to 1 GHz" condition to <math>t_{ODC}</math> spec.</p> <p>Updated package diagram.</p> <p>Added Acronyms and Ordering Code Definition.</p>   |
| *C   | 3017258 | CXQ             | 08/27/2010      | Corrected Output Rise/Fall time diagram.   |
| *D   | 3100234 | CXQ             | 11/18/2010      | <p>Updated Phase jitter to 0.15ps max from 0.11ps max.</p> <p>Changed <math>V_{IN}</math> and <math>V_{OUT}</math> specs from 4.0V to "lesser of 4.0 or <math>V_{DD} + 0.4</math>"</p> <p>Removed 200mA min LU spec, replaced with "Meets or exceeds JEDEC Spec JESD78B IC Latchup Test"</p> <p>Removed <math>R_P</math> spec for differential input clock pins <math>IN_X</math> and <math>IN_X\#</math>.</p> <p>Changed <math>C_{IN}</math> condition to "Measured at 10 MHz".</p> <p>Changed <math>PN_{ADD}</math> specs for 1MHz, 10MHz, and 20MHz offsets.</p> <p>Removed <math>t_S</math> and <math>t_H</math> specs from AC specs table.</p>  |
| *E   | 3135201 | CXQ             | 01/12/2011      | <p>Removed "Preliminary" status heading.</p> <p>Removed resistors from <math>IN_X/IN_X\#</math> in <a href="#">Logic Block Diagram</a>.</p> <p>Added <a href="#">Figure 9</a> to describe <math>T_{SOE}</math> and <math>T_{SOD}</math>.</p>   |
| *F   | 3090938 | CXQ             | 02/25/2011      | Post to external web.  |

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