

1:10 Clock Fanout Buffer

Features

- Low voltage operation
- Full range support:
 - 3.3V
 - 2.5V
 - 1.8V
- Over voltage tolerant input hot swappable
- 1:10 Fanout
- Drives either a 50-Ohm or 75-Ohm load
- Low input capacitance
- Low output skew
- Low propagation delay
- Typical (t_{pd} less than 4 ns)
- High speed operation:
 - 200 MHz at 1.8V
 - 650 MHz at 2.5V and 3.3V
- Industrial versions available
- Available packages include: SOIC, SSOP

Description

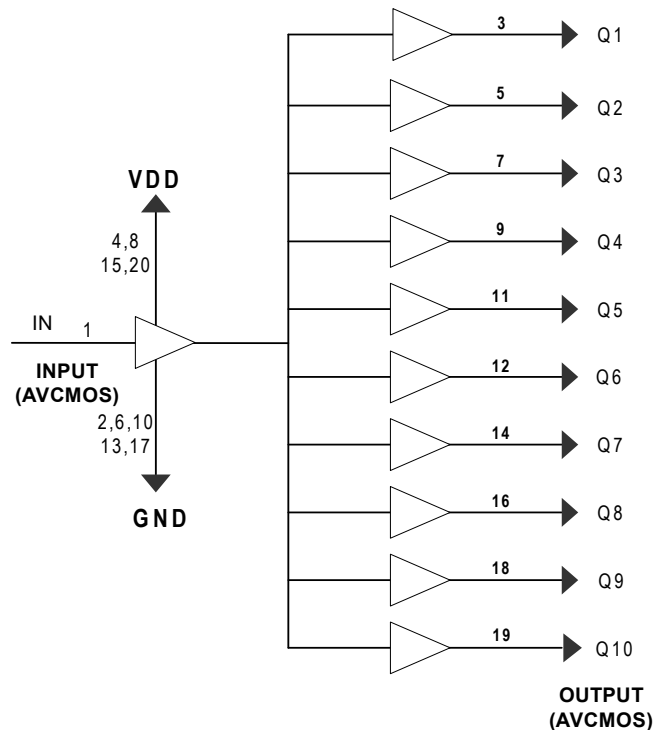
The Cypress series of network circuits are produced using advanced 0.35 micron CMOS technology, achieving the industry's fastest logic and buffers.

The Cypress CY2CC910 fanout buffer features one input and 10 outputs. It is ideal for conversion from and to 3.3V, 2.5V, and 1.8V

Designed for Data Communications clock management applications, the large fanout from a single input reduces loading on the input clock.

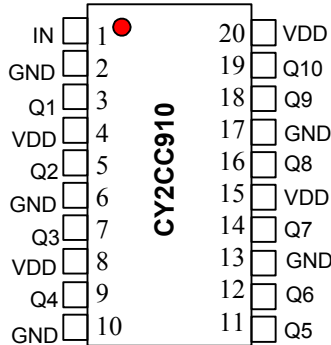
Cypress employs the unique AVCMOS type outputs VOI (Variable Output Impedance) that dynamically adjust for variable impedance matching, eliminate the need for series damping resistors, and reduce overall noise.

Logic Block Diagram



Pin Configuration

Figure 1. 20-Pin SOIP-SSOP



20 pin SOIC/SSOP

Pin Description

| Pin Number | Pin Name | Description |
|---------------------------|--------------------------------|--------------|
| 1 | IN | Input |
| 2,6,10,13,17 | GND | Ground |
| 4,8,15,20 | V _{DD} | Power Supply |
| 3,5,7,9,11,12,14,16,18,19 | Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8,Q9,Q10 | Output |

Maximum Ratings^[1]

Storage Temperature: -65°C to +150°C
 Ambient Temperature: -40°C to +85°C
 Supply Voltage to Ground Potential
 V_{CC} -0.5V to 4.6V
 Input -0.5V to 5.8V

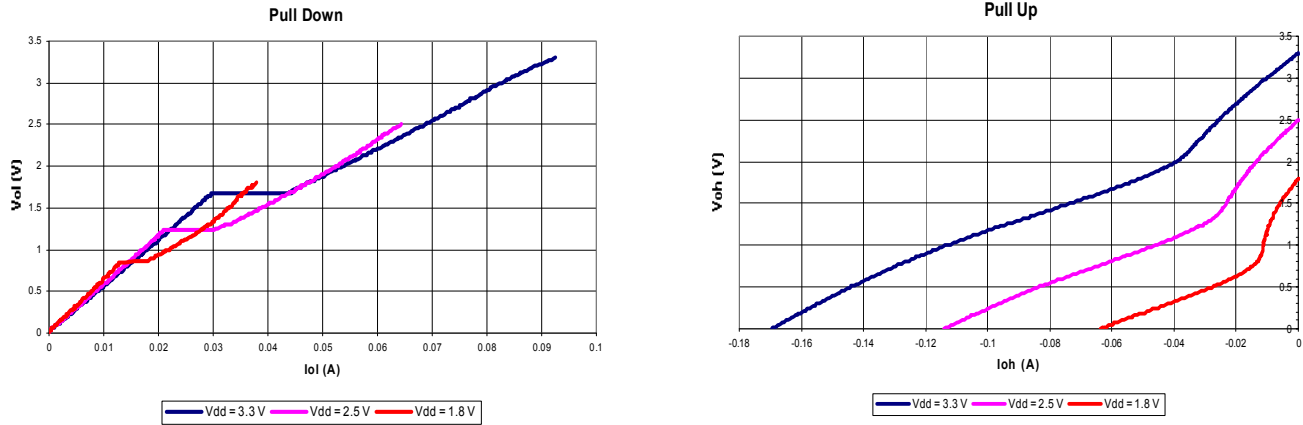
Supply Voltage to Ground Potential
 (Outputs only) -0.5V to V_{DD} + 1V
 DC Output Voltage -0.5V to V_{DD} + 1V
 Power Dissipation 0.75W

Note

1. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Variable Output Impedance Control (VOI)

Figure 2. Output Voltage versus Output Current ($T_A = 25^\circ\text{C}$)



DC Electrical Characteristics

At 3.3V (See Figure 3)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|------------------|--------------------------|---|-----|------|------|------|
| V _{OH} | Output High Voltage | V _{DD} = Min., V _{IN} = V _{IH} or V _{IL} I _{OH} = -12 mA | 2.3 | 3.3 | | V |
| V _{OL} | Output Low Voltage | V _{DD} = Min., V _{IN} = V _{IH} or V _{IL} I _{OL} = 12 mA | | 0.2 | 0.5 | V |
| V _{IH} | Input High Voltage | Guaranteed Logic High Level | 2 | | 5.8 | V |
| V _{IL} | Input Low Voltage | Guaranteed Logic Low Level | | | 0.8 | V |
| I _{IH} | Input High Current | V _{DD} = Max. V _{IN} = 2.7V | | | 1 | μA |
| I _{IL} | Input Low Current | V _{DD} = Max. V _{IN} = 0.5V | | | -1 | μA |
| I _I | Input High Current | V _{DD} = Max., V _{IN} = V _{DD} (Max.) | | | 20 | μA |
| V _{IK} | Clamp Diode Voltage | V _{DD} = Min., I _{IN} = -18 mA | | -0.7 | -1.2 | V |
| I _{OK} | Continuous Clamp Current | V _{DD} = Max., V _{OUT} = GND | | | -50 | mA |
| O _{OFF} | Power-down Disable | V _{DD} = GND, V _{OUT} = < 4.5V | | | 100 | μA |
| V _H | Input Hysteresis | | | 80 | | mV |

At 2.5V (See [Figure 3](#))

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|------------------|--------------------------|--|-------------------------|------|------|------|
| V _{OH} | Output High Voltage | V _{DD} = Min., V _{IN} = V _{IH} or V _{IL} | I _{OH} = -7 mA | 1.8 | | V |
| | | | I _{OH} = 12 mA | 1.6 | | V |
| V _{OL} | Output Low Voltage | V _{DD} = Min., V _{IN} = V _{IH} or V _{IL} | | | 0.65 | V |
| V _{IH} | Input High Voltage | Guaranteed Logic High Level | 1.6 | | 5.0 | V |
| V _{IL} | Input Low Voltage | Guaranteed Logic Low Level | | | 0.8 | V |
| I _{IH} | Input High Current | V _{DD} = Max. | | | 1 | μA |
| I _{IL} | Input Low Current | V _{DD} = Max. | | | -1 | μA |
| I _I | Input High Current | V _{DD} = Max., V _{IN} = V _{DD} (Max.) | | | 20 | μA |
| V _{IK} | Clamp Diode Voltage | V _{DD} = Min., I _{IN} = -18 mA | | -0.7 | -1.2 | V |
| I _{OK} | Continuous Clamp Current | V _{DD} = Max., V _{OUT} = GND | | | -50 | mA |
| O _{OFF} | Power Down Disable | V _{DD} = GND, V _{OUT} = < 4.5V | | | 100 | μA |
| V _H | Input Hysteresis | | | 80 | | mV |

At 1.8V (See [Figure 7](#))

| Parameter | Description | Test Condition ^[2] | Min | Max | Unit |
|-----------------|---------------------|-------------------------------|-----------------------------|----------------------------|------|
| V _{DD} | Supply Voltage | | 1.71 | 1.89 | V |
| V _{IH} | Input High Voltage | | 0.65V _{DD} [1.1] | 4.3 | V |
| V _{IL} | Input Low Voltage | | -0.3 | 0.35 V _{DD} [0.6] | V |
| V _{OH} | Output High Voltage | I _{OH} = -2 mA | V _{DD} - 0.45[1.2] | | V |
| V _{OL} | Output Low Voltage | I _{OH} = 2 mA | | 0.45 | V |

Capacitance

| Parameter | Description | Test Conditions | Typ | Max | Unit |
|------------------|--------------------|-----------------------|-----|-----|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 2.5 | | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 6.5 | | pF |

Power Supply Characteristics (See [Figure 3](#))

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|------------------|--|---|-----|-----|------|------------|
| ΔI _{CC} | Delta I _{CC} Quiescent Power Supply Current | (I _{DD} @ V _{DD} = Max and V _{IN} = V _{DD}) - (I _{DD} @ V _{DD} = Max and V _{IN} = V _{DD} - 0.6V) | | | 50 | μA |
| I _{CCD} | Dynamic Power Supply Current | V _{DD} = Max Input toggling 50% Duty Cycle, Outputs Open | | | 0.63 | mA/ MHZ |
| I _C | Total Power Supply Current | V _{DD} = Max Input toggling 50% Duty Cycle, Outputs Open fL = 40 MHZ | | | 25 | mA |

Note

2. Test load conditions: 500-Ohm to ground with approximately 6-pF total loading and 200-MHz maximum frequency.

High Frequency Parametrics

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|-------------------|--------------------------------------|--|-----|-----|-----|------|
| D_J | Jitter, Deterministic | 50% duty cycle $t_W(50-50)$ The "point to point load circuit" Output Jitter – Input Jitter | | | 20 | ps |
| F_{max} 3.3V | Maximum frequency $V_{DD} = 3.3V$ | 50% duty cycle $t_W(50-50)$ Standard Load Circuit. | | | 160 | MHz |
| | | 50% duty cycle $t_W(50-50)$ The "point to point load circuit" | | | 650 | |
| F_{max} 2.5V | Maximum frequency $V_{DD} = 2.5V$ | The "point-to-point load circuit" $V_{IN} = 2.4V/0.0V$ $V_{OUT} = 1.7V/0.7V$ | | | 200 | MHz |
| F_{max} 1.8V | Maximum frequency $V_{DD} = 1.8V$ | The "6-pF load circuit" $V_{IN} = 1.7/0.0V$ $V_{OUT} = 1.2V/0.4V$ | | | 200 | MHz |
| $F_{max(20)}$ | Maximum frequency $V_{DD} = 3.3V$ | 20% duty cycle $t_W(20-80)$ The "point to point load circuit" $V_{IN} = 3.0V/0.0V$ $V_{OUT} = 2.3V/0.4V$ | | | 250 | MHz |
| t_W 3.3V | Minimum pulse $V_{DD} = 3.3V$ | The "point-to-point load circuit" $V_{IN} = 3.0V/0.0V$ $F = 100$ MHz $V_{OUT} = 2.0V/0.8V$ | 1 | | | ns |
| t_W 2.5V | Minimum pulse $V_{DD} = 2.5V$ | The "point-to-point load circuit" $V_{IN} = 2.4V/0.0V$ $F = 100$ MHz $V_{OUT} = 1.7V/0.7V$ | 1 | | | ns |
| t_W 1.8V | Minimum pulse $V_{DD} = 1.8V$ | The "6-pF load circuit" $V_{IN} = 1.7V/0.0V$ $V_{OUT} = 1.2V/0.4V$ | 1 | | | ns |

AC Switching Characteristics

At 3.3V ($V_{DD} = 3.3V \pm 5\%$, Temperature = $-40^\circ C$ to $+85^\circ C$)

| Parameter | Description | Min | Typ | Max | Unit |
|-------------|--|-----|-----|-----|------|
| t_{PLH} | Propagation Delay – Low to High | 1.5 | 2.7 | 3.5 | ns |
| t_{PHL} | Propagation Delay – High to Low | 1.5 | 2.7 | 3.5 | ns |
| t_R | Output Rise Time | | 0.8 | | V/ns |
| t_F | Output Fall Time | | 0.8 | | V/ns |
| $t_{SK(0)}$ | Output Skew: Skew between outputs of the same package (in phase). | | | 0.2 | ns |
| $t_{SK(p)}$ | Pulse Skew: Skew between opposite transitions of the same output ($t_{PHL} - t_{PLH}$). | | | 0.2 | ns |
| $t_{SK(t)}$ | Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type. | | | 0.4 | ns |

At 2.5V ($V_{DD} = 2.5V \pm 5\%$, Temperature = $-40^\circ C$ to $+85^\circ C$)

| Parameter | Description | Min | Typ | Max | Unit |
|-------------|--|-----|-----|-----|------|
| t_{PLH} | Propagation Delay – Low to High | 1.5 | 2.7 | 3.5 | ns |
| t_{PHL} | Propagation Delay – High to Low | 1.5 | 2.7 | 3.5 | ns |
| t_R | Output Rise Time | | 0.8 | | V/ns |
| t_F | Output Fall Time | | 0.8 | | V/ns |
| $t_{SK(0)}$ | Output Skew: Skew between outputs of the same package (in phase). | | | 0.2 | ns |
| $t_{SK(p)}$ | Pulse Skew: Skew between opposite transitions of the same output ($t_{PHL} - t_{PLH}$). | | | 0.2 | ns |
| $t_{SK(t)}$ | Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type. | | | 0.4 | ns |

AC Switching Characteristics

At 1.8V ($V_{DD} = 1.8V \pm 5\%$, Temperature = $-40^{\circ}C$ to $+85^{\circ}C$)

| Parameter | Description | Min | Typ | Max | Unit |
|-------------|--|-----|-----|-----|------|
| t_{PLH} | Propagation Delay – Low to High | 1.5 | 2.7 | 3.5 | ns |
| t_{PHL} | Propagation Delay – High to Low | 1.5 | 2.7 | 3.5 | ns |
| t_R | Output Rise Time 20 – 80% | 0.2 | | 1.5 | ns |
| t_F | Output Fall Time 20 – 80% | 0.2 | | 1.5 | ns |
| $t_{SK(0)}$ | Output Skew: Skew between outputs of the same package (in phase). | | | 0.2 | ns |
| $t_{SK(p)}$ | Pulse Skew: Skew between opposite transitions of the same output ($t_{PHL} - t_{PLH}$). | | | 0.2 | ns |
| $t_{SK(t)}$ | Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type. | | | 0.4 | ns |

Parameter Measurement Information: V_{DD} at 3.3V to 2.5V

Figure 3. Load Circuit [3,4,5]

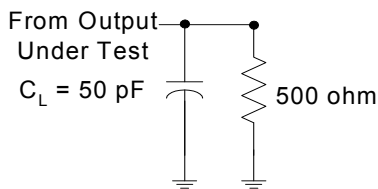


Figure 5. Point to Point Load Circuit [3,4,5]

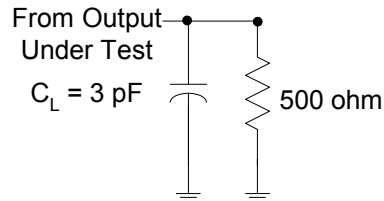


Figure 4. Voltage Waveforms Propagation Delay Times [6]

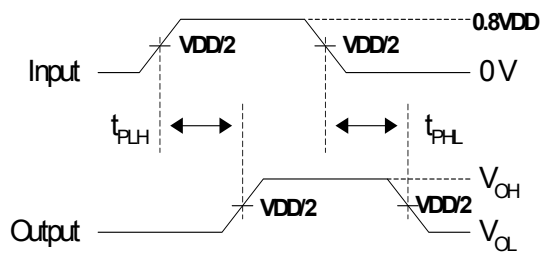
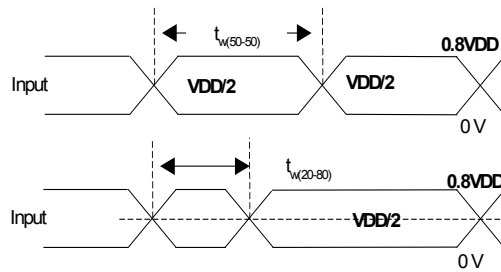


Figure 6. Voltage Waveforms – Pulse Duration [4]



Parameter Measurement Information: V_{DD} at 8V

Figure 7. Load Circuit [3,4,5]

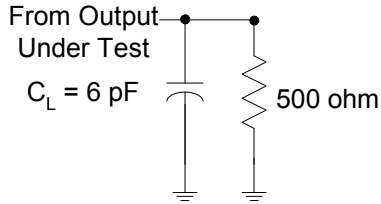


Figure 9. Voltage Waveforms – Pulse Duration^[4]

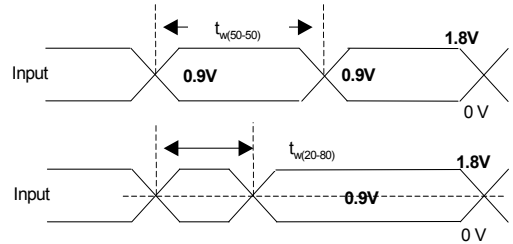


Figure 8. Voltage Waveforms Propagation

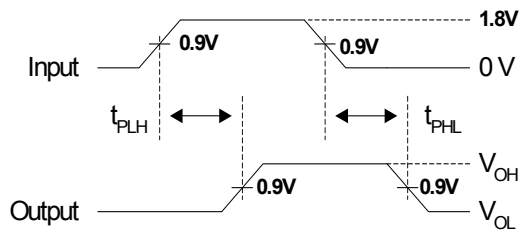


Figure 10. Pulse Skew - $tsk_{(p)}$

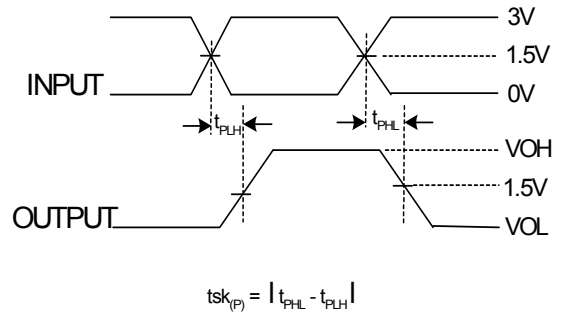
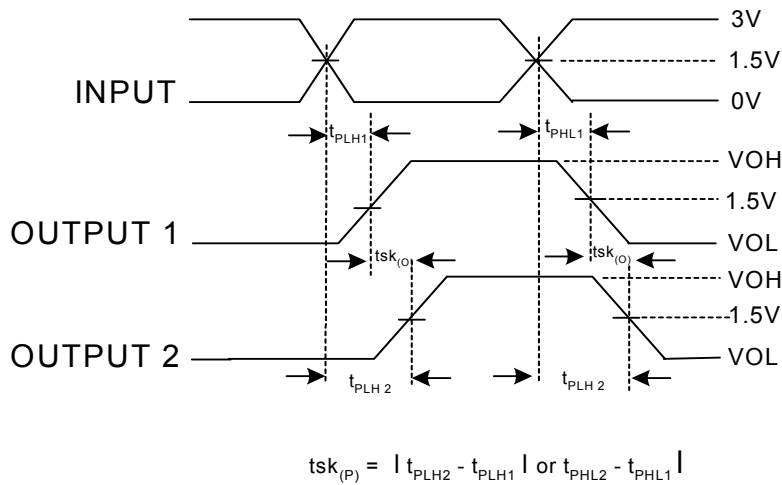


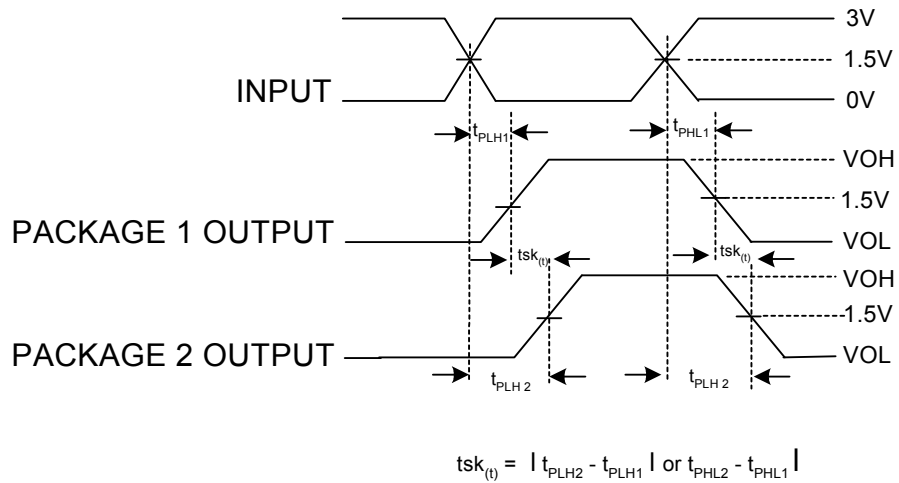
Figure 11. Output Skew - $tsk_{(0)}$



Notes

3. C_L includes probe and jig capacitance.
4. All input pulses are supplied by generators having the following characteristics: PRR < 100 MHz, $Z_0 = 50\Omega$, $t_R < 2.5$ ns, $t_F < 2.5$ ns.
5. The outputs are measured one at a time with one transition per measurement.
6. T_{PLH} and T_{PHL} are the same as t_{pd} .

Figure 12. Package Skew - $tsk_{(t)}$

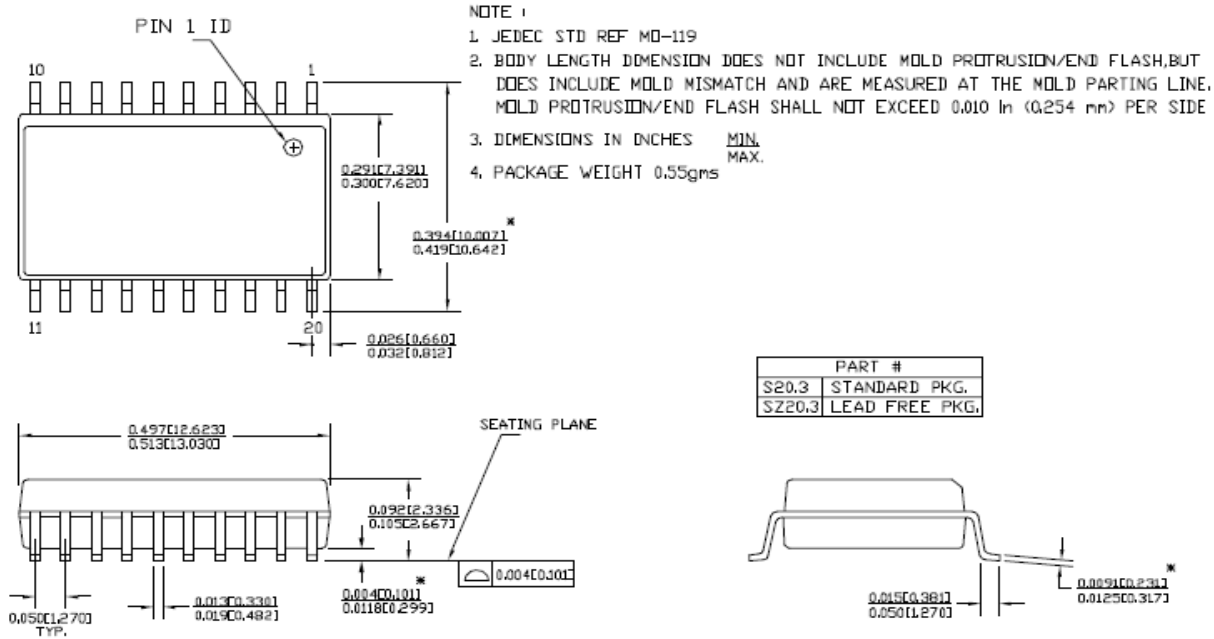


Ordering Information

| Part Number | Package Type | Product Flow | Status |
|----------------|---------------------------|--------------------------|----------|
| CY2CC910SI | 20-pin SOIC | Industrial, -40° to 85°C | Obsolete |
| CY2CC910SIT | 20-pin SOIC-Tape and Reel | Industrial, -40° to 85°C | Obsolete |
| CY2CC910SC | 20-pin SOIC | Commercial, 0°C to 70°C | Obsolete |
| CY2CC910SCT | 20-pin SOIC-Tape and Reel | Commercial, 0°C to 70°C | Obsolete |
| CY2CC910OI | 20-pin SSOP | Industrial, -40° to 85°C | Obsolete |
| CY2CC910OIT | 20-pin SSOP-Tape and Reel | Industrial, -40° to 85°C | Obsolete |
| CY2CC910OC | 20-pin SSOP | Commercial, 0°C to 70°C | Obsolete |
| CY2CC910OCT | 20-pin SSOP-Tape and Reel | Commercial, 0°C to 70°C | Obsolete |
| Pb-free | | | |
| CY2CC910OXI | 20-pin SSOP | Industrial, -40° to 85°C | Active |
| CY2CC910OXIT | 20-pin SSOP-Tape and Reel | Industrial, -40° to 85°C | Active |
| CY2CC910OXC | 20-pin SSOP | Commercial, 0°C to 70°C | Active |
| CY2CC910OXCT | 20-pin SSOP-Tape and Reel | Commercial, 0°C to 70°C | Active |

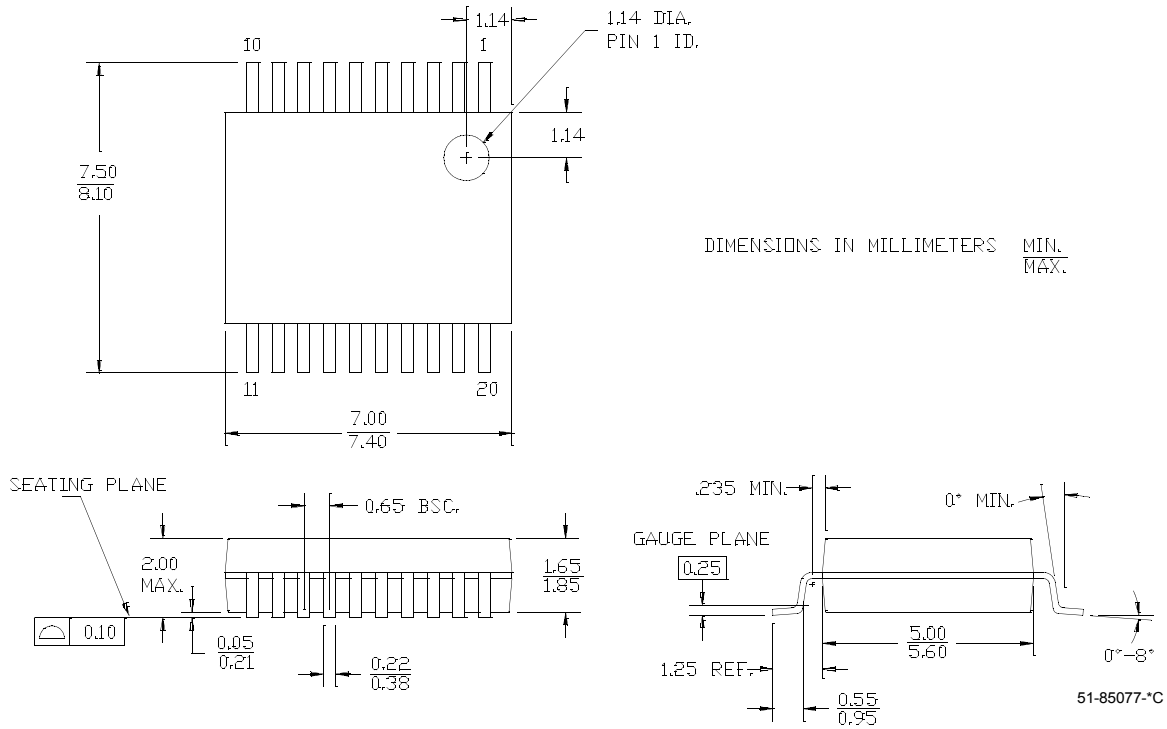
Package Drawing and Dimensions

Figure 13. 20-Pin (300-Mil) SOIC S5 (51-85024)



51-85024 *C

Figure 14. 20-Pin Shrunk Small Outline Package O20



Document History Page

| Document Title: CY2CC910 1:10 Clock Fanout Buffer Document No: 38-07348 | | | | |
|--|---------|-----------------|-----------------|---|
| Rev. | ECN NO. | Orig. of Change | Submission Date | Description of Change |
| ** | 114318 | TSM | 05/10/02 | New Data Sheet |
| *A | 119148 | RGL | 10/07/02 | Added 5.8 as the Max. value for V_{IH} in the DC Electrical Characteristics @3.3V table. Changed the Max. value of V_{IH} from 5.8 to 5.0 in the DC Electrical Characteristics @2.5V table. Changed the value of V_{IH} from $V_{DD}+0.3$ [2.25] to 4.3 in the DC Electrical Characteristics @1.8V table. |
| *B | 404287 | RGL | See ECN | Added Lead-free devices for SSOP |
| *C | 2595534 | CXQ/PYRS | 10/23/08 | Added "Status" column to Ordering Information table Updated Package Diagram 51-85024 Updated template |

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