FAIRCHILD SEMICONDUCTOR®

October 2008

FAN6300
Highly Integrated Quasi-Resonant Current Mode PWM Controller

Features

- High-Voltage Startup
- Quasi-Resonant Operation
- Cycle-by-Cycle Current Limiting
- Peak-Current-Mode Control
- Leading-Edge Blanking
- Internal Minimum t_{OFF}
- Internal 2ms Soft-Start
- Over-Power Compensation
- GATE Output Maximum Voltage
- Auto-Recovery Short-Circuit Protection (FB Pin)
- Auto-Recovery Open-Loop Protection (FB Pin)
- VDD Pin & Output Voltage (DET Pin) OVP Latched

Applications

- AC/DC NB Adapters
- Open-Frame SMPS

Description

The highly integrated FAN6300 PWM controller provides several features to enhance the performance of flyback converters. A built-in HV startup circuit can provide more startup current to reduce the startup time of the controller. Once the V_{DD} voltage exceeds the turn-on threshold voltage, the HV startup function is disabled immediately to improve power consumption. An internal valley voltage detector ensures the power system operates at Quasi-Resonant operation in wide-range line voltage and any load conditions and reduces switching loss to minimize switching voltage on drain of power MOSFET.

To minimize standby power consumption and light-load efficiency, a proprietary green-mode function provides off-time modulation to decrease switching frequency and perform extended valley voltage switching to keep to a minimum switching voltage.

FAN6300 controller also provides many protection functions. Pulse-by-pulse current limiting ensures the fixed peak current limit level, even when a short circuit occurs. Once an open-circuit failure occurs in the feedback loop, the internal protection circuit disables PWM output immediately. As long as V_{DD} drops below the turn-off threshold voltage, controller also disables PWM output. The gate output is clamped at 18V to protect the power MOS from high gate-source voltage conditions. The minimum t_{OFF} time limit prevents the system frequency from being too high. If the DET pin reaches OVP, internal OTP is triggered, and the power system enters latch-mode until AC power is removed.

FAN6300 controller is available in 8-pin SOP and DIP packages.

Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	Packing Method
FAN6300SY	-40 to +105°C	Green	8-Lead, Small Out-line Package (SOP)	Tape & Reel
FAN6300DY	-40 to +105°C	Green	8-Lead, Dual In-line Package (DIP)	Tube

For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Application Diagram

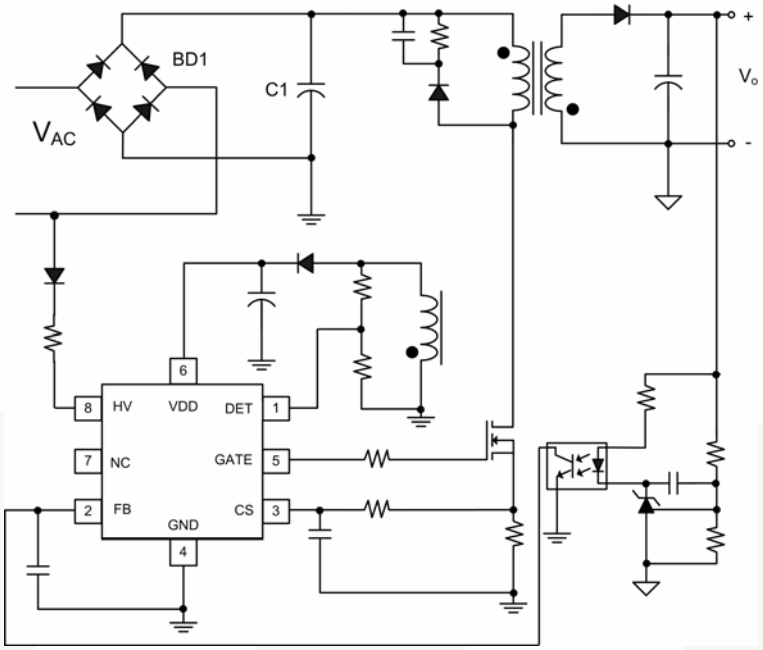


Figure 1. Typical Application

Internal Block Diagram

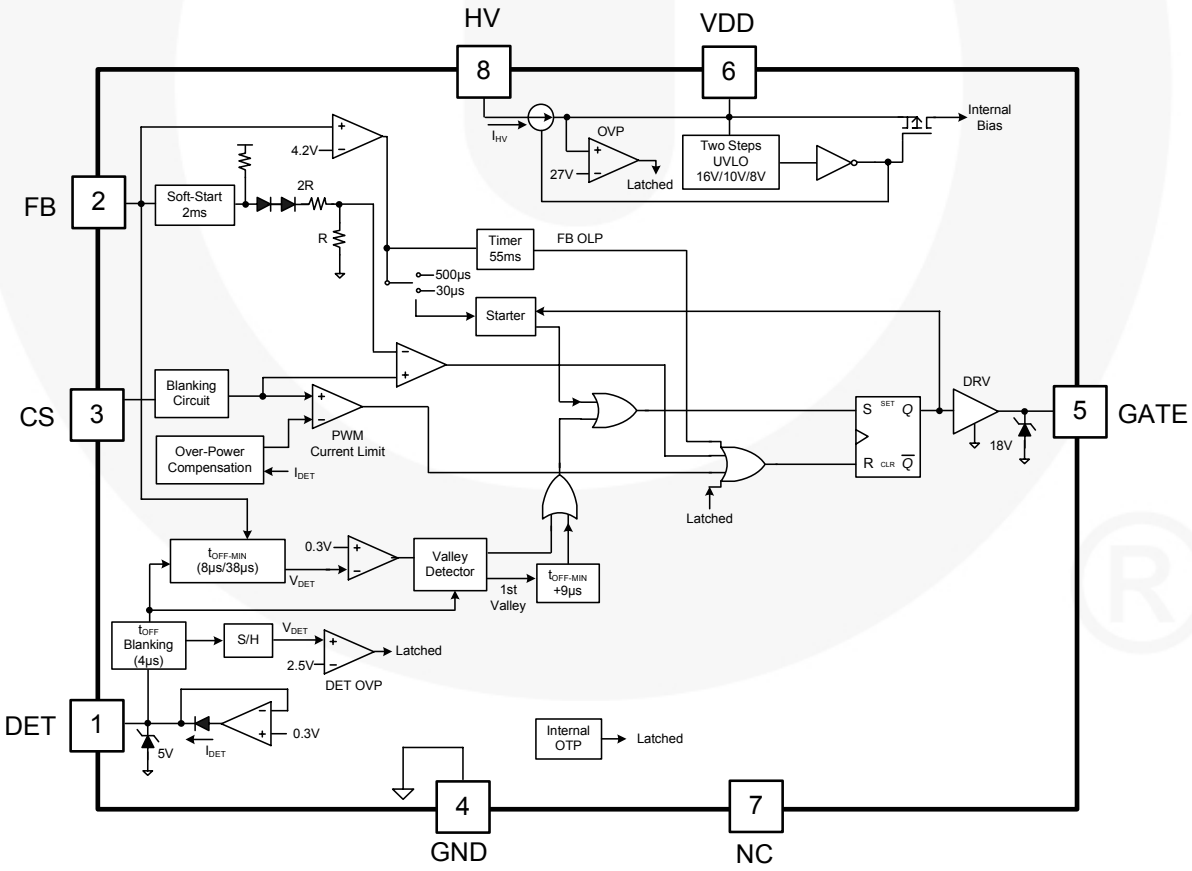
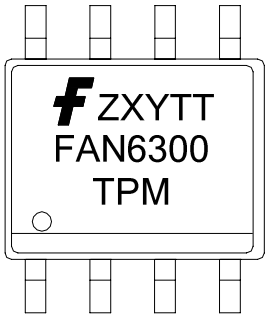


Figure 2. Functional Block Diagram

Marking Information



F: Fairchild logo
Z: Plant Code
X: Year Code
Y: Week Code
TT: Die Run Code
T: Package type (D =DIP, S = SOP)
P: Y = Green Package
M: Manufacturing flow code

Figure 3. Marking Diagram

Pin Configuration

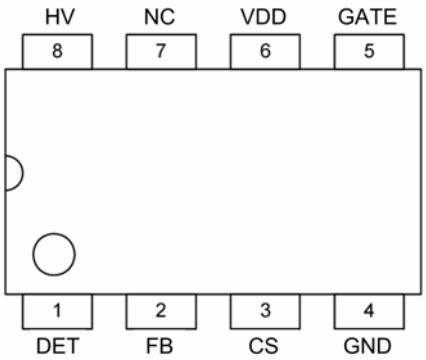


Figure 4. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	DET	This pin is connected to an auxiliary winding of the transformer via resistors of the divider for the following purposes: - Generates a ZCD signal once the secondary-side switching current falls to zero. - Produces an offset voltage to compensate the threshold voltage of the peak current limit to provide a constant power limit. The offset is generated in accordance with the input voltage when PWM signal is enabled. - Detects the valley voltage of the switching waveform to achieve the valley voltage switching and minimize the switching losses. A voltage comparator and a 2.5V reference voltage develop an output OVP protection. The ratio of the divider decides what output voltage to stop gate, as an optical coupler and secondary shunt regulator are used.
2	FB	The Feedback pin is supposed to be connected to the output of the error amplifier for achieving the voltage control loop. The FB should be connected to the output of the optical coupler if the error-amplifier is equipped at the secondary-side of the power converter. For the primary-side control application, this pin is applied to connect a RC network to the ground for feedback-loop compensation. The input impedance of this pin is a 5kΩ equivalent resistance. A 1/3 attenuator connected between the FB and the PWM circuit is used for the loop gain attenuation. FAN6300 performs an open-loop protection once the FB voltage is higher than a threshold voltage (around 4.2V) more than 55ms.

Pin #	Name	Description
3	CS	Input to the comparator of the over-current protection. A resistor senses the switching current and the resulting voltage is applied to this pin for the cycle-by-cycle current limit. The threshold voltage for peak current limit is 0.8V.
4	GND	The power ground and signal ground. A 0.1μF decoupling capacitor placed between V_{DD} and GND is recommended.
5	GATE	Totem-pole output generates the PWM signal to drive the external power MOSFET. The clamped gate output voltage is 18V.
6	VDD	Power supply. The threshold voltages for startup and turn-off are 16V and 10V. The startup current is less than 20μA and the operating current is lower than 4.5mA.
7	NC	No connect.
8	HV	High-voltage startup.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	DC Supply Voltage		30	V
V_{HV}	HV Pin		500	V
V_H	GATE Pin	-0.3	25.0	V
V_L	V_{FB}, V_{CS}, V_{DET}	-0.3	7.0	V
P_D	Power Dissipation		400	mW
T_J	Operating Junction Temperature		+150	°C
T_{STG}	Storage Temperature Range	-55	+150	°C
T_L	Lead Temperature, Soldering 10 Seconds		+270	°C
ESD	Human Body Model, JEDEC:JESD22-A114		2.5	KV
	Charged Device Model, JEDEC:JESD22-C101		1.5	

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltage values, except differential voltages, are given with respect to GND pin.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating Ambient Temperature	-40	+105	°C

Electrical Characteristics

V_{DD}=15V, T_A=25℃, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD SECTION						
V_{OP}	Continuously Operating Voltage				25	V
V_{DD-ON}	Turn-on Threshold Voltage		15	16	17	V
$V_{DD-PWM-OFF}$	PWM Off Threshold Voltage		9	10	11	V
V_{DD-OFF}	Turn-Off Threshold Voltage		7	8	9	V
I_{DD-ST}	Startup Current	0V< V_{DD} < V_{DD-ON} GATE Open		10	30	µA
I_{DD-OP}	Operating Current	V_{DD}=15V, f_s=60KHz, C_L=2nF		4.5	5.5	mA
$I_{DD-PWM-OFF}$	Operating Current at PWM-Off Phase	V_{DD}=$V_{DD-PWM-OFF}$-0.5V	70	80	90	µA
V_{DD-OVP}	V_{DD} Over-Voltage Protection (Latch-Off)		26	27	28	V
$t_{VDD-OVP}$	V_{DD} OVP Debounce Time		100	150	200	µs
HV STARTUP CURRENT SOURCE SECTION						
I_{HV}	Supply Current Drawn From HV Pin	V_{AC}=90V (V_{DC}=120V), V_{DD}=0V		1.2		mA
I_{HV-LC}	Leakage Current After Startup	HV=500V, V_{DD}=V_{DD-OFF} +1V		1	20	µA
FEEDBACK INPUT SECTION						
A_V	Input-voltage to Current Sense Attenuation	A_V=$\Delta V_{CS}/\Delta V_{FB}$ 0<V_{CS}<0.9	1/2.75	1/3.00	1/3.25	V/V
Z_{FB}	Input Impedance		3	5	7	KΩ
I_{OZ}	Bias Current	FB=V_{OZ}		1.2	2.0	mA
V_{OZ}	Zero Duty Cycle Input Voltage			1		V
V_{FB-OLP}	Open-Loop Protection Threshold Voltage		3.9	4.2	4.5	V
t_{D-OLP}	Debounce Time for Open-Loop / Overload Protection			55		ms
t_{SS}	Internal Soft-Start Time		1.6	2.0	2.4	ms
DET PIN OVP AND VALLEY DETECTION SECTION						
$V_{DET-OVP}$	Comparator Reference Voltage		2.45	2.50	2.55	V
V_{V-HIGH}	Output High Voltage		4.5			V
V_{V-LOW}	Output Low Voltage				0.5	V
$t_{DET-OVP}$	Output OVP (Latched) Debounce Time		100	150	200	µs
$I_{DET-SOURCE}$	Maximum Source Current				1	mA
$V_{DET-HIGH}$	Upper Clamp Voltage				5	V
$V_{DET-LOW}$	Lower Clamp Voltage		0.1	0.3		V
$t_{OFF-BNK}$	Leading-Edge Blanking Time for DET-OVP, PWM MOS Turns Off[3]			4		µs

Note:

3. Guaranteed by design.

Electrical Characteristics (Continued)

V_{DD}=15V, T_A=25℃, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
OSCILLATOR SECTION						
t_{ON-MAX}	Maximum On Time		38	45	52	μs
$t_{OFF-MIN}$	Minimum Off Time (Maximum Frequency)	$V_{FB} \geqq V_N$	7	8	9	μs
		$V_{FB}=V_G$		38		μs
V_N	Beginning of Green-On Mode at FB Voltage Level		1.95	2.10	2.25	V
V_G	Beginning of Green-Off Mode at FB Voltage Level		1.05	1.20	1.35	V
ΔV_{FBG}	Green-Off Mode V_{FB} Hysteresis Voltage			0.1		V
$t_{STARTER}$	Start Timer (Time-out Timer)	$V_{FB}<V_G$	450	550	650	μs
		$V_{FB}>V_{FB-OLP}$	25	30	35	μs
$t_{TIME-OUT}$	Timeout After $t_{OFF-MIN}$ (If No Valley Signal)			9		μs
OUTPUT SECTION						
V_{OL}	Output Voltage Low	V_{DD}=15V, I_O=150mA			1.5	V
V_{OH}	Output Voltage High	V_{DD}=12V, I_O=150mA	7.5			V
t_R	Rising Time			120		ns
t_F	Falling Time			60		ns
V_{CLAMP}	GATE Output Clamping Voltage		17	18	19	V
CURRENT SENSE SECTION						
t_{PD}	Delay to Output			150	250	ns
V_{LIMIT}	Cycle-by-Cycle Current Limit Threshold Voltage	I_{DET} = 60μA	0.74	0.78	0.82	V
		I_{DET} = 175μA	0.545	0.585	0.625	V
		I_{DET} = 220μA	0.42	0.46	0.50	V
V_{SLOPE}	Slope Compensation	t_{ON}=45μs		0.3		V
		t_{ON}=0μs		0.1		V
t_{BNK}	Leading Edge Blanking Time (MOS Turns On)		225	300	375	ns
V_{CS-H}	V_{CS} Camped High Voltage	CS Pin Floating	4.5		5.0	V
t_{CS-H}	Delay Time	CS Pin Floating	100	150	200	μs

Typical Performance Characteristics

These characteristic graphs are normalized at T_A = 25°C.

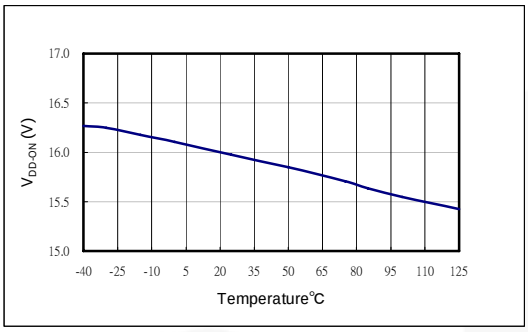


Figure 5. Turn-on Threshold Voltage

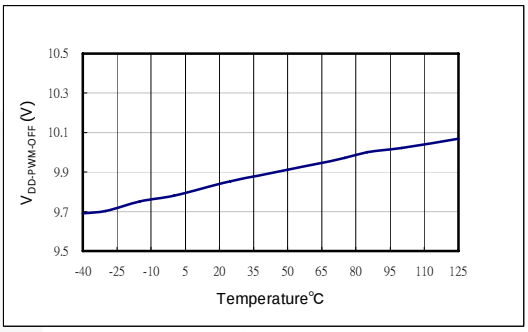


Figure 6. PWM Off Threshold Voltage

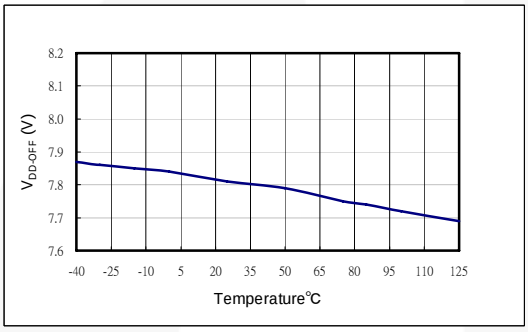


Figure 7. Turn-off Threshold Voltage

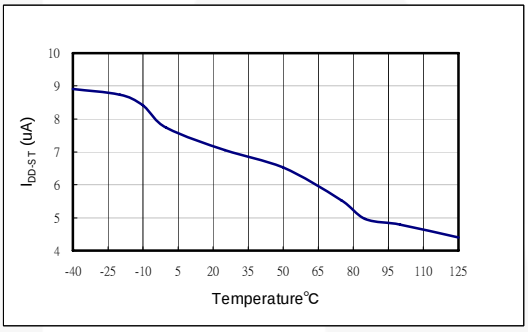


Figure 8. Startup Current

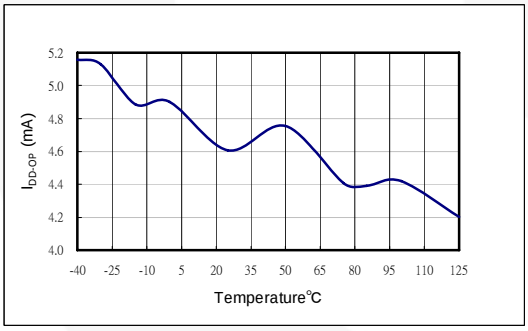


Figure 9. Operating Current

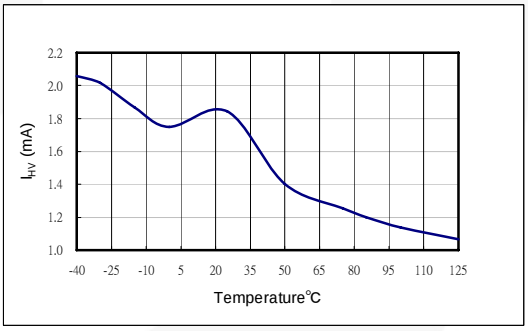


Figure 10. Supply Current Drawn From HV Pin

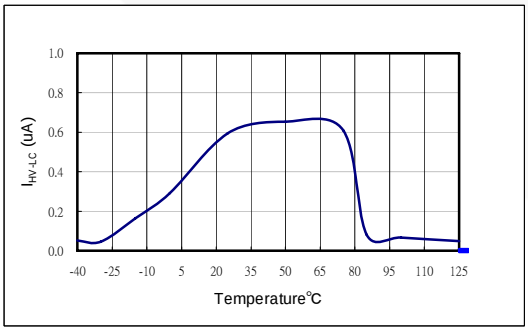


Figure 11. Leakage Current After Startup

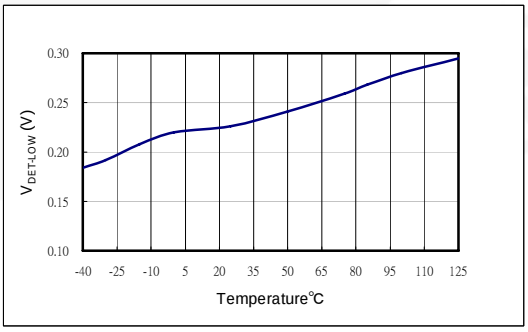


Figure 12. Lower Clamp Voltage

Typical Performance Characteristics

These characteristic graphs are normalized at T_A = 25°C.

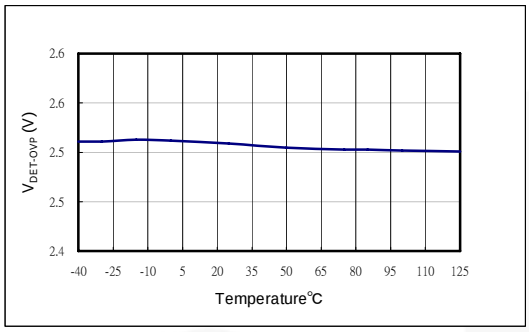


Figure 13. Comparator Reference Voltage

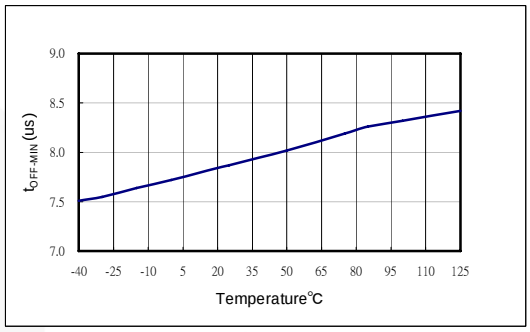


Figure 14. Minimum Off Time (V_{FB}>V_N)

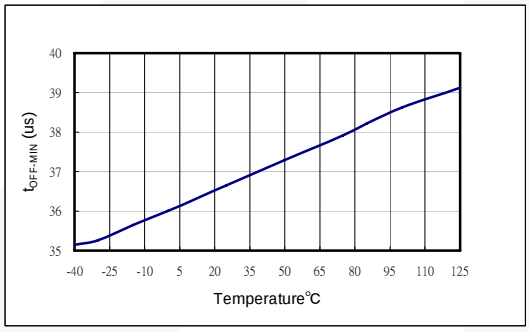


Figure 15. Minimum Off Time (V_{FB}=V_G)

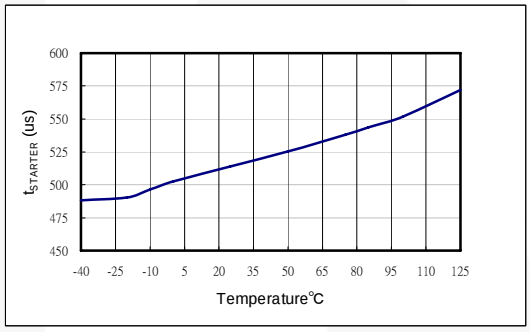


Figure 16. Start Timer (V_{FB}<V_G)

Operation Description

The FAN6300 of PWM controller integrates designs to enhance the performance of flyback converters. An internal valley voltage detector ensures power system operates at Quasi-Resonant (QR) operation in a wide range of line voltage. The following descriptions highlight some of the features of the FAN6300 series.

Startup Current

For startup, the HV pin is connected to the line input or bulk capacitor through an external diode and resistor, R_{HV}, which are recommended as 1N4007 and 100kΩ. Typical startup current drawn from pin HV is 1.2mA and it charges the hold-up capacitor through the diode and resistor. When the V_{DD} voltage level reaches V_{DD-ON}, the startup current switches off. At this moment, the V_{DD} capacitor only supplies the FAN6300 to maintain V_{DD} until the auxiliary winding of the main transformer provides the operating current.

Valley Detection

The DET pin is connected to an auxiliary winding of the transformer via resistors of the divider to generate a valley signal once the secondary-side switching current discharges to zero. It detects the valley voltage of the switching waveform to achieve the valley voltage switching. This ensures QR operation, minimizes switching losses, and reduces EMI. Figure 17 shows divider resistors R_{DET} and R_A. R_{DET} is recommended as 150kΩ to 220kΩ to achieve valley voltage switching. When V_{AUX} (in Figure 17) is negative, the DET pin voltage is clamped to 0.3V.

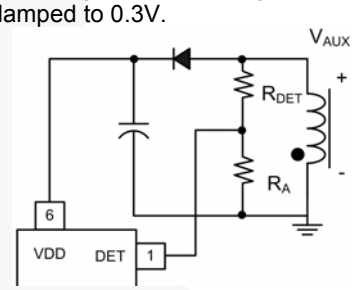


Figure 17. Valley Detect Section

The internal timer (minimum t_{OFF} time) prevents gate retriggering within 8μs after the gate signal going-low transition. The minimum t_{OFF} time limit prevents the system frequency being too high. Figure 18 shows a typical drain voltage waveform with first valley switching.

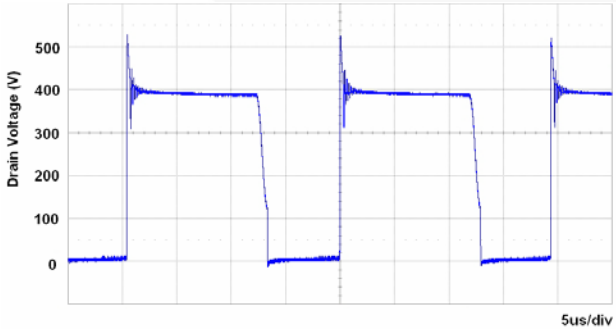


Figure 18. First Valley Switching

Green-Mode Operation

The proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency under light-load conditions. V_{FB}, which is derived from the voltage feedback loop, is taken as the reference. In Figure 19, once V_{FB} is lower than V_N, the $t_{OFF-MIN}$ time increases linearly with lower V_{FB}. The valley voltage detection signal does not start until the $t_{OFF-MIN}$ time finishes. Therefore, the valley detect circuit is activated until the $t_{OFF-MIN}$ time finishes, which decreases the switching frequency and provides extended valley voltage switching. However, in very light load condition, it might fail to detect the valley voltage after the $t_{OFF-MIN}$ expires. Under this condition, an internal $t_{TIME-OUT}$ signal initiates a new cycle start after a 9μs delay. Figure 20 and Figure 21 show the two different conditions.

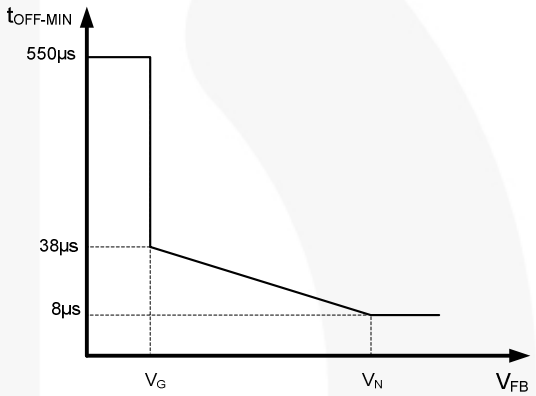


Figure 19. V_{FB} vs. $t_{OFF-MIN}$ Curve

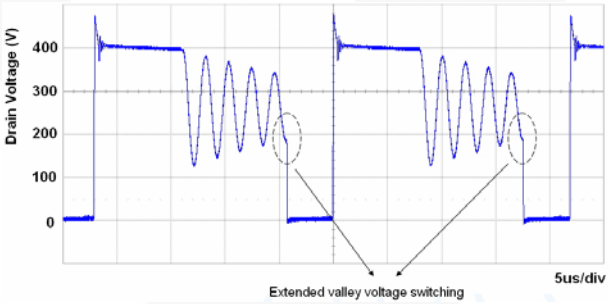


Figure 20. QR Operation in Extended Valley Voltage Detection Mode

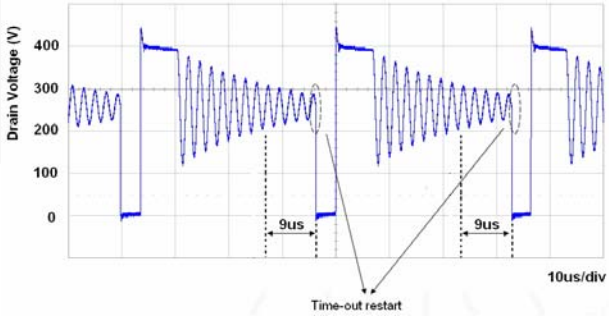


Figure 21. Internal $t_{TIME-OUT}$ Initiates New Cycle After Failure to Detect Valley Voltage (with 9μs Delay)

Current Sensing and PWM Current Limiting

Peak-current-mode control is utilized to regulate output voltage and provide pulse-by-pulse current limiting. The switch current is detected by a sense resistor into the CS pin. The PWM duty cycle is determined by this current sense signal and V_{FB}. When the voltage on CS pin reaches around $V_{LIMIT} = (V_{FB}-1.2)/3$, the switch cycle is terminated immediately. V_{LIMIT} is internally clamped to a variable voltage around 0.8V for output power limit.

Leading Edge Blanking (LEB)

Each time the power MOFFET switches on, a turn-on spike occurs on the sense resistor. To avoid premature termination of the switching pulse, lead-edge blanking time is built in. During the blanking period, the current limit comparator is disabled; it cannot switch off the gate driver.

Under-Voltage Lockout (UVLO)

The turn-on, PWM-off, and turn-off thresholds are fixed internally at 16/10/8V. During startup, the startup capacitor must be charged to 16V through the startup resistor to enable the IC. The hold-up capacitor continues to supply V_{DD} until energy can be delivered from the auxiliary winding of the main transformer. V_{DD} must not drop below 10V during this startup process. This UVLO hysteresis window ensures that hold-up capacitor is adequate to supply V_{DD} during startup.

Gate Output

The BiCMOS output stage is a fast totem-pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 18V Zener diode to protect power MOSFET transistors against undesired over-voltage gate signals.

Over-Power Compensation

To compensate this variation for wide AC input range, the DET pin produces an offset voltage to compensate the threshold voltage of the peak current limit to provide a constant-power limit. The offset is generated in accordance with the input voltage when PWM signal is enabled. This results in a lower current limit at high-line inputs than low-line inputs. At fixed-load condition, the CS limit is higher when the value of R_{DET} is higher. R_{DET} also affects the H/L line constant power limit.

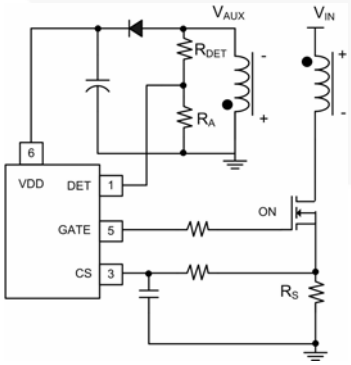


Figure 22. H/L Line Constant Power Limit Compensated by DET Pin

V_{DD} Over-Voltage Protection

V_{DD} over-voltage protection prevents damage due to abnormal conditions. Once the V_{DD} voltage is over the V_{DD} over-voltage protection voltage (V_{DD-OVP}) and lasts for t_{VDDOVP}, controller enters latch mode and stops all switching operation.

Output Over-Voltage Protection

The output over-voltage protection works by the sampling voltage, as shown in Figure 23, after switch-off sequence. A 4μs blanking time ignores the leakage inductance ringing. A voltage comparator and a 2.5V reference voltage develop an output OVP protection. The ratio of the divider determines the sampling voltage of the stop gate, as an optical coupler and secondary shunt regulator are used. If the DET pin OVP is triggered, power system enters latch-mode until AC power is removed.

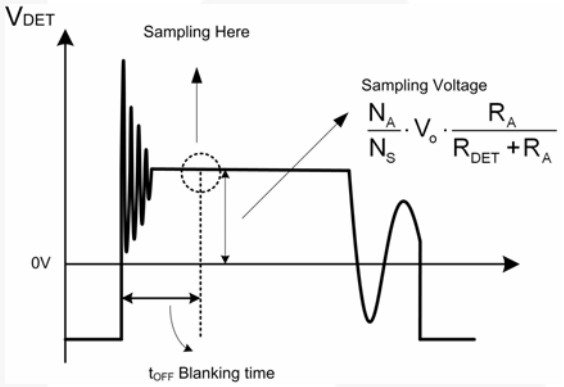


Figure 23. Voltage Sampled After 4μs Blanking Time After Switch-off Sequence

Short-Circuit and Open-Loop Protection

The FB voltage increases every time the output of the power supply is shorted or overloaded. If the FB voltage remains higher than a built-in threshold for longer than t_{D-OLP}, PWM output is turned off. As PWM output is turned-off, the supply voltage V_{DD} begins decreasing.

When V_{DD} goes below the PWM-off threshold of 10V, V_{DD} decreases to 8V, then the controller is totally shut down. V_{DD} is charged up to the turn-on threshold voltage of 16V through the startup resistor until PWM output is restarted. This protection feature continues as long as the overloading condition persists. This prevents the power supply from overheating due to overloading.

Physical Dimensions

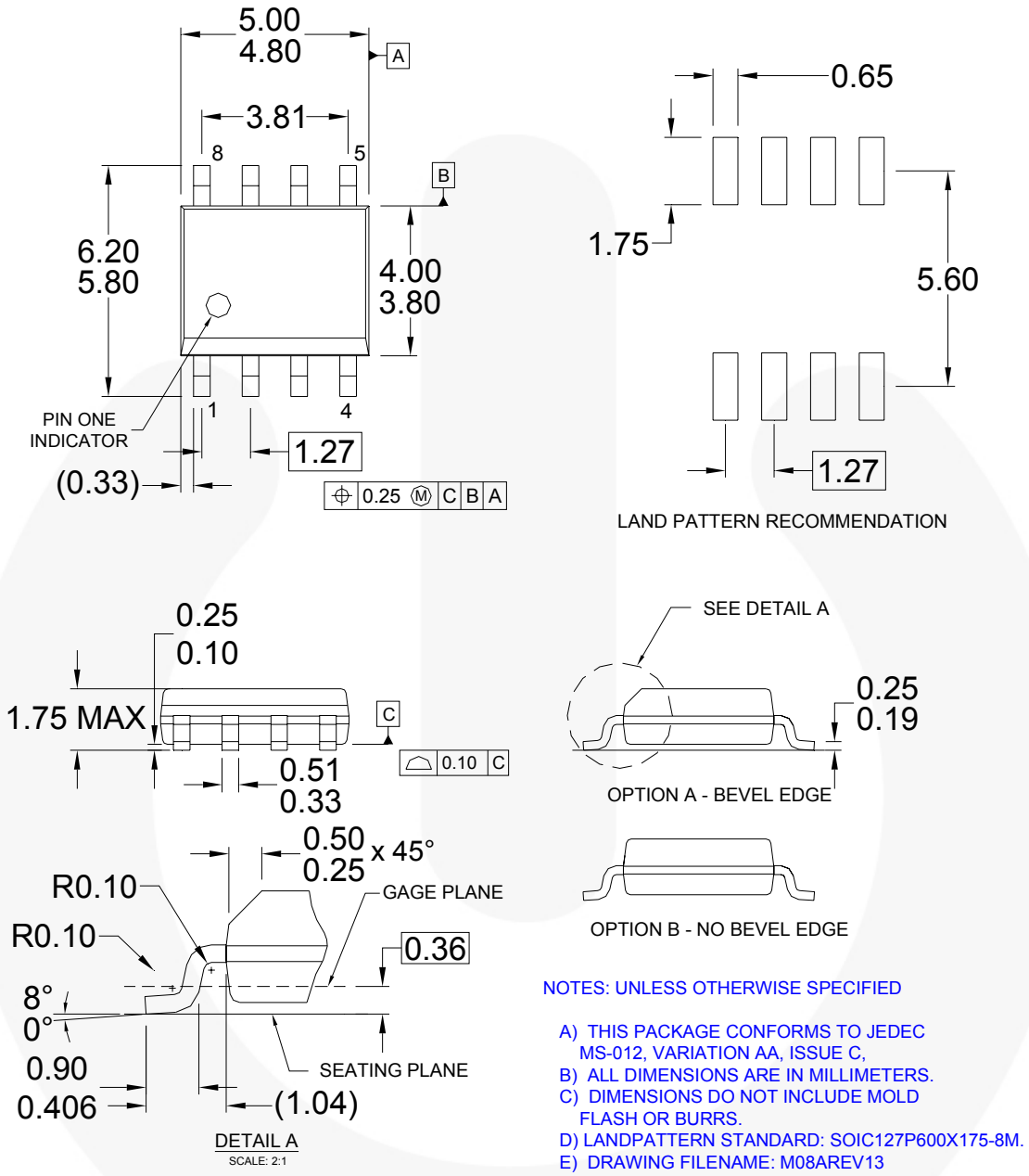


Figure 24. 8-Pin Small Outline Package (SOP)

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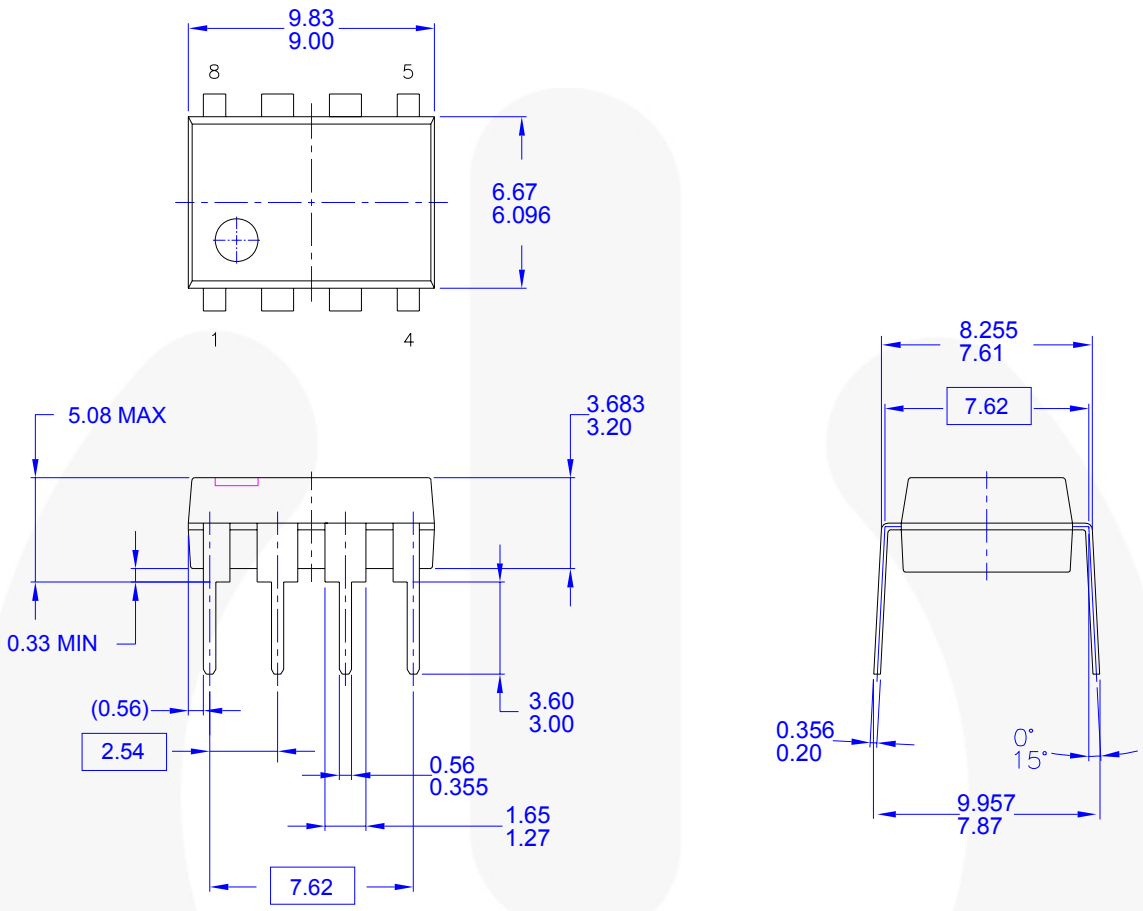
Physical Dimensions (Continued)



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BA

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

E) DRAWING FILENAME AND REVSION: MKT-N08FREV2.

Figure 25. 8-Pin Dual Inline Package (DIP-8)

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Rev. I37