FAIRCHILD SEMICONDUCTOR®

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FAN3988
USB/Charger and Over-Voltage Detection Device

Features

- Charger/USB Detection Device
- Charger/USB Device Detection Flag
- Over-/Under-Voltage Detection Flag
- V_{BUS} Supply: 2.7V to 20V
- C_{ON} of 1.5pF
- 6 MLP Package

Applications

- Mobile Phones
- Handheld Devices

Description

The FAN3988 is a USB-connection-monitoring device used to determine if a standard USB device or a battery-changing device is connected.

The FAN3988 sets the FLAG1 pin to logic HIGH or LOW as an indicator to the system controller that a standard USB device or a charger is connected to the USB port. The FAN3988 also monitors the V_{BUS} for over- or under-voltage conditions. The FLAG2 pin is set LOW if V_{BUS} is less than 3.3V or greater than 6.0V.

The FAN3988 is packaged in a very small 6-lead MLP package suitable for small board space applications, such as mobile phones.

Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	Packing Method	Quantity
FAN3988IL6X_F113	-40°C to +85°C	Green	6-Lead Molded Leadless Package (MLP)	Reel	3000

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

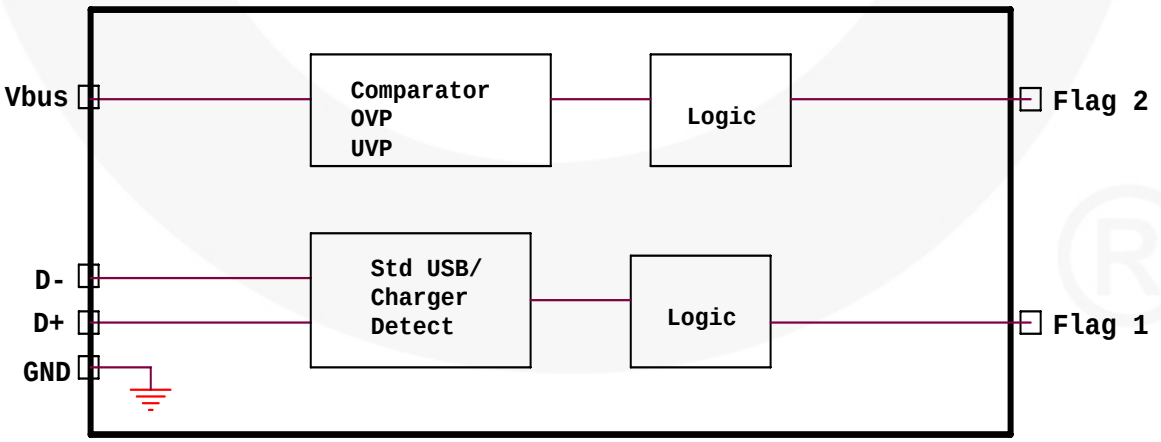


Figure 1. Block Diagram

Pin Configuration

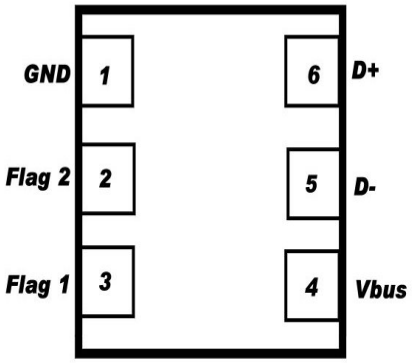


Figure 2. Pin Configuration (Top View)

Figure 3. Pin Configuration (Bottom View)

Pin Definitions

Pin#	Name	Type	Description
1	GND	Input	Device ground
2	Flag2	Output	Over/under-voltage flag output
3	Flag1	Output	Charger/standard USB device detect flag
4	V_{BUS}	Input	Power input from charger, USB device, or handheld battery
5	D-	Input	USB data input
6	D+	Input	USB data input

Truth Table

Connection State	V_{BUS}	D-	D+	FLAG1	FLAG2
STD USB Device	0V	R to GND	R to GND	LOW	LOW
USB Charger	5V	Short to D+	Short to D-	HIGH	HIGH
V_{BUS} GT 6V	GT 6V	Short to D+	Short to D-	HIGH	LOW
V_{BUS} LT 3.3V	LT 3.3V	Short to D+	Short to D-	HIGH	LOW
PC Data/Charger	5V	Open	Open	LOW	HIGH

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_S	DC Supply Voltage	-0.3	20.0	V
V_{IO}	Analog and Digital I/O	-0.3	V_{CC}+0.3	V

Reliability Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			+150	°C
T_{STG}	Storage Temperature Range	-65		+150	°C
Θ_{JA}	Thermal Resistance, JEDEC Standard, Multilayer Test Boards, Still Air		41		°C/W

ESD Information

Symbol	Parameter	Max.	Unit
ESD	Human Body Model, JESD22-A114	5	kV
	Charged Device Model, JESD22-C101	2	kV

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Temperature Range	-40		+85	°C
V_{CC}	Supply Voltage Range	2.7	5.0	20.0	V

DC Electrical Characteristics

T_A = 25°C, V_{CC} = 5.0V, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Supply						
V_S	Supply Voltage Range	V_S Range	2.7	5.0	20.0	V
I_{CC}	Quiescent Supply Current	V_S = +5.0V, D+ D- Shorted		1.2	2.0	mA
t_{SUPPLY}	Power-Up Stabilization Time	V_S = +5.0V, D+ D- Shorted		10		ms
Input Characteristics						
C_{D+}	Input Capacitance			1.5	2.0	pF
C_{D-}	Input Capacitance			1.5	2.0	pF
I_{off} D+	Off Leakage Current	V_{BUS} = 0V or 5V V_{IN} on D+ = 5V		1		µA
I_{off} D-	Off Leakage Current	V_{BUS} = 0V or 5V V_{IN} on D- = 5V		1		µA
Output Characteristics						
OV_{DETECT}	Over-Voltage Threshold Detect	V_S = +5.0V, Flag2 = LOW	5.8	6.0	6.5	V
OV_{HYST}	Over-Voltage Hysteresis	Voltage Sweep through Upper and Lower Trip Points		100		mV
UV_{DETECT}	Under-Voltage Threshold Detect	V_S = +5.0V, Flag2 = LOW	3.0	3.3	3.6	V
UV_{HYST}	Under-Voltage Hysteresis	Voltage Sweep through Upper and Lower Trip Points		100		mV
V_{OH} FLAG1/ FLAG2	Minimum HIGH Output Voltage	V_S = +5.0V, I_{OH} = -20µA	2.4			V
V_{OL} FLAG1/ FLAG2	Maximum LOW Output Voltage	V_S = +5.0V, I_{OL} = 20µA			0.3	V
t_{Off}	Flag2 HIGH to LOW	100pF Load		10		ns
t_{on}	Flag2 LOW to HIGH	100pF Load		44		ns

Typical Performance Characteristics

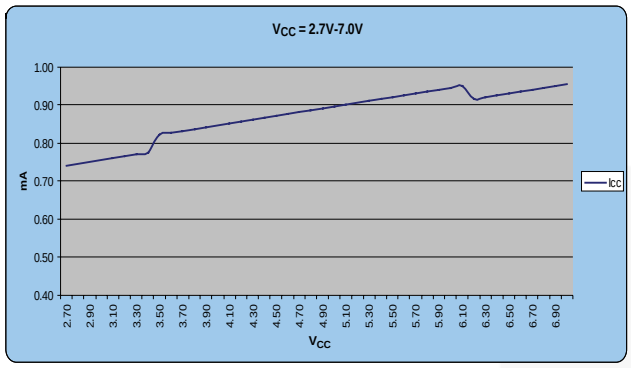


Figure 4. I_{CC} vs. V_{CC} (2.7V-7.0V) No Load

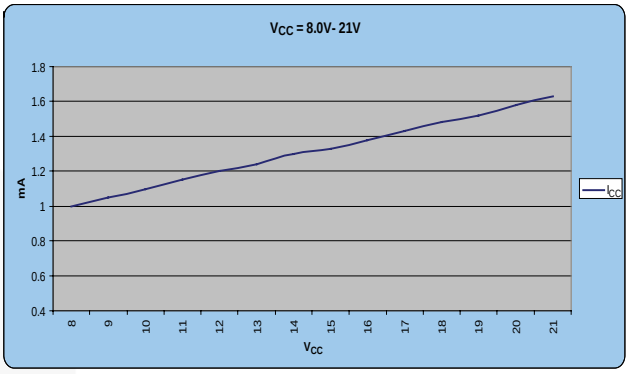


Figure 5. I_{CC} vs. V_{CC} (8.0V-21V) No Load

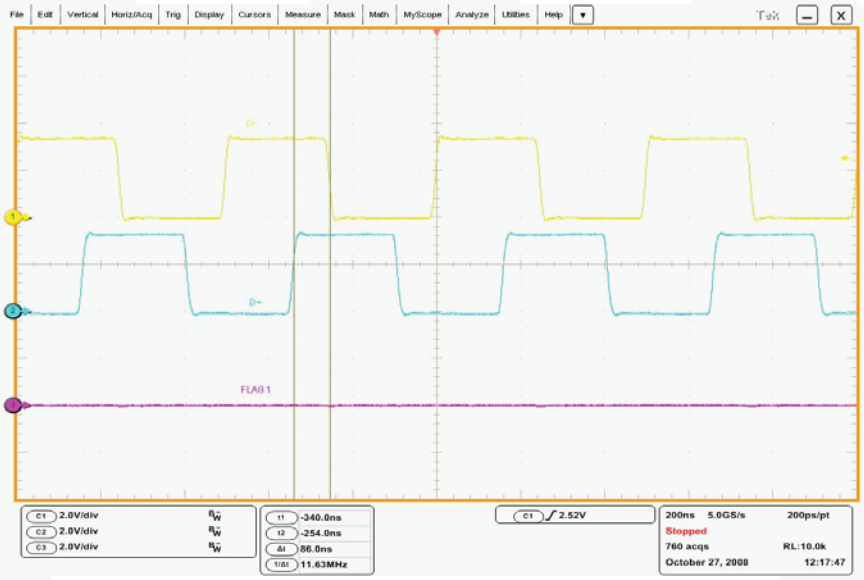


Figure 6. No Fault on Flag 1, Skew=65ns

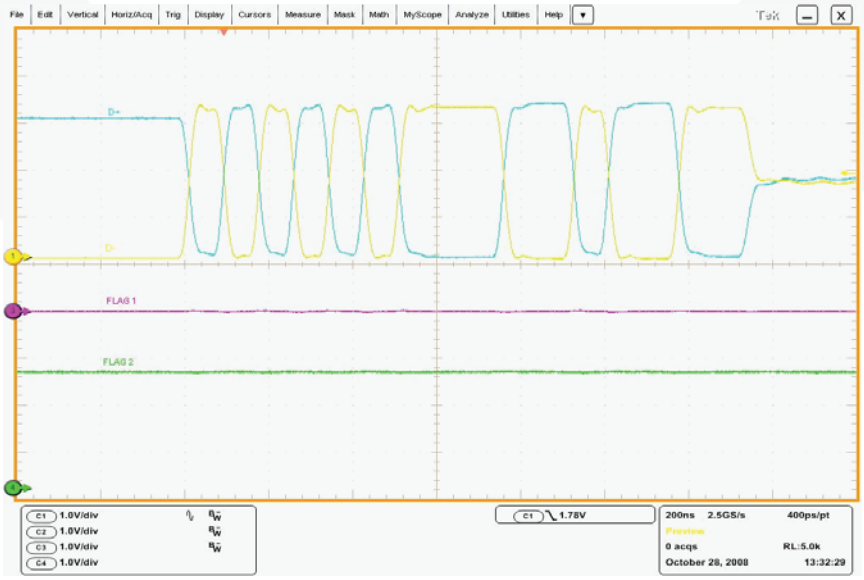


Figure 7. PC Data Running D+/D- (Flag 1 and Flag 2 at Correct Levels)

Typical Applications Circuit

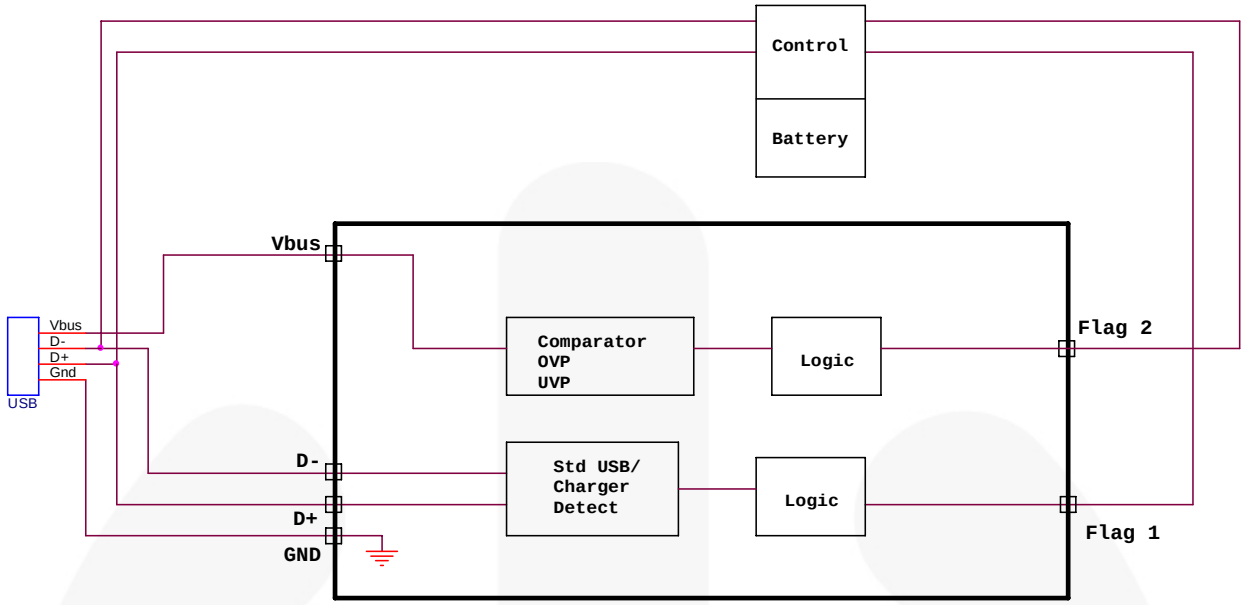


Figure 8. Mobile Phone System Example

Application Information

The FAN3988 has three purposes: (1) to monitor V_{BUS} and set a flag if 6.4V>V_{BUS}<3.0V; (2) to set a flag when a charging device is connected to D+/D-; and (3) to set a flag if a standard USB device is connected to D+/D-.

The FAN3988 with no USB charging device connected does not have power on V_{BUS}. The only way to power V_{BUS} is from an external charging source. When using an external charger, the FAN3988 powers up through an on-board LDO and supplies power to the complete device. After a 160ms delay, Flag 1 and Flag 2 go to a logic level determined by the conditions on the V_{BUS} and D+/D- inputs. The default state on the D+/D- switch (after power-up) is closed. If the D+/D- lines are shorted, Flag 1 is set HIGH, indicating a valid charging device is present. Flag 2 also goes HIGH, indicating that the voltage on V_{BUS} is correct (6.4V>V_{BUS}<3.0V).

When a standard USB device is connected (like a headset), the baseband chip detects a standard USB device through D+/D- lines and Flag 2 stays LOW, indicating a non-valid V_{BUS} voltage. Since there is no power to the FAN3988, Flag 1 stays LOW, indicating a standard USB device is present.

If Flag 2 were to go LOW during normal operation, this would indicate an invalid voltage on the V_{BUS} line and the baseband chip would prevent an improper voltage being sent directly to the battery.

PCB Layout Guidelines

Pad1

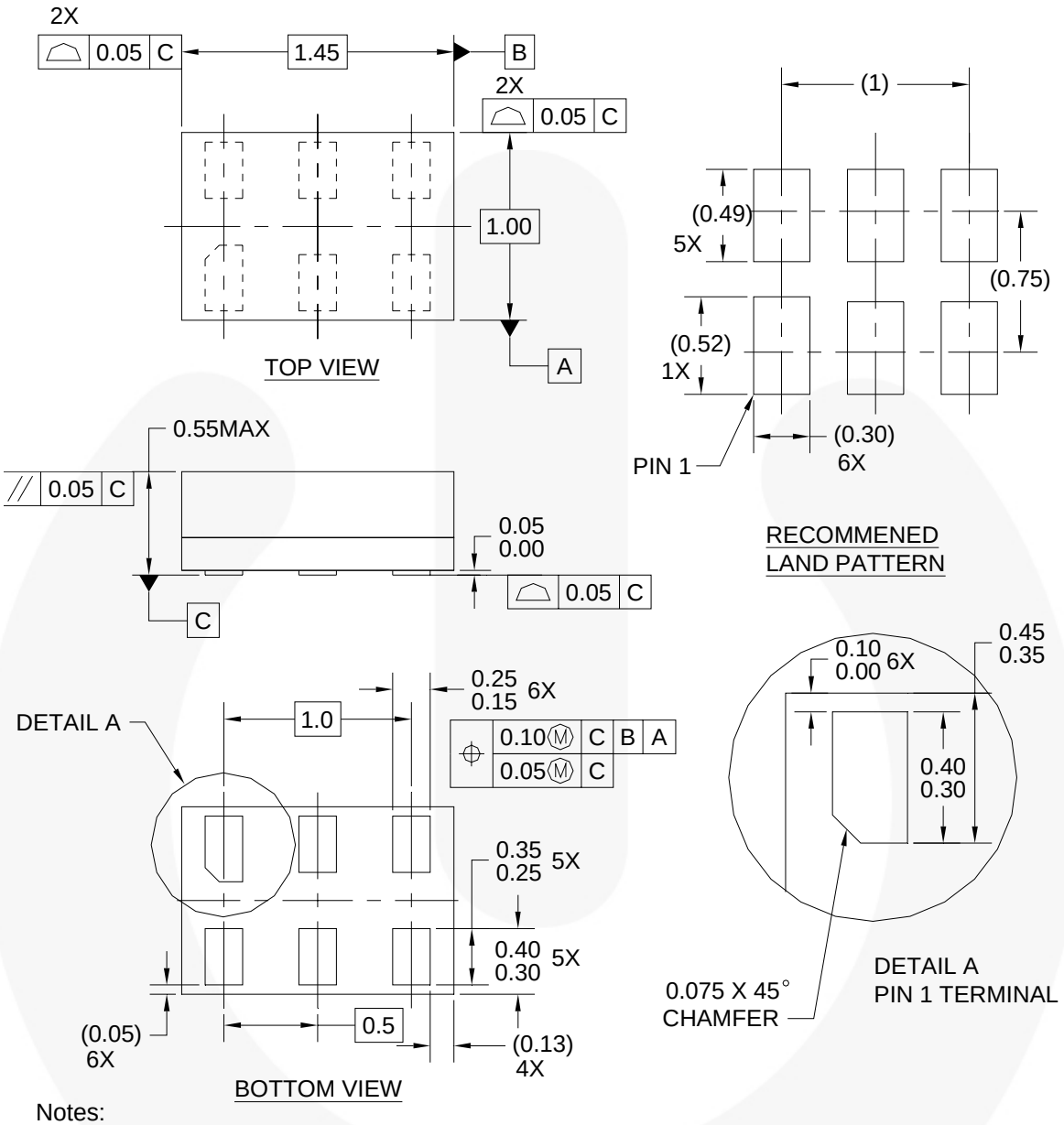
This exposed DAP is connected to an internal die substrate at ground potential. The pad should be left floating or can be connected to the ground plane. This pad should never be connected to the power plane.

Figure 9. PCB Layout

Note:

1. *Please reference Fairchild Semiconductor application note AN-5067 - PCB Land Pattern Design and Surface Mount Guidelines for MLP Packages, available at:* *http://www.fairchildsemi.com/an/AN/AN-5067.pdf*

Physical Dimensions



Notes:

1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06AREVC

Figure 10. 6-Lead Molded Leadless Package (MLP)

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