FAIRCHILD SEMICONDUCTOR®

February 2007

# FAN73832
# Half-Bridge Gate-Drive IC

## Features

- Floating Channel for Bootstrap Operation to +600V
- Typically 350mA/650mA Sourcing/Sinking Current Driving Capability for Both Channels
- Extended Allowable Negative $V_S$ Swing to -9.8V for Signal Propagation at $V_{DD}$=$V_{BS}$=15V
- High-Side Output in Phase of IN Signal
- Built-in UVLO Functions for Both Channels
- Built-in Common-Mode dv/dt Noise Canceling Circuit
- Internal 400ns Minimum Dead-Time at $R_{DT}$=20KΩ
- Programmable Turn-on Delay-Time Control (Dead-Time)

## Applications

- SMPS
- Motor Drive Inverter
- Fluorescent Lamp Ballast
- HID Ballast

## Description

The FAN73832 is a half-bridge, gate-drive IC with shut-down and programmable dead-time control functions for driving MOSFETs and IGBTs, operating up to +600V.

Fairchild's high-voltage process and common-mode noise canceling technique provide stable operation of high-side driver under high dv/dt noise circumstances.

An advanced level-shift circuit allows high-side gate driver operation up to $V_S$=-9.8V (typical) for $V_{BS}$=15V.

The UVLO circuits for both channels prevent malfunction when $V_{DD}$ and $V_{BS}$ are lower than the specified thresh-old voltage.

Output drivers typically source/sink 350mA/650mA, respectively, which is suitable for all kinds of half- and full-bridge inverters.

**8-SOP**

**8-DIP**

## Ordering Information

| Part Number | Package | Pb-Free | Operating Temperature Range | Packing Method |
|---|---|---|---|---|
| FAN73832M(1) | 8-SOP | Yes | -40°C ~ 125°C | Tube |
| FAN73832MX(1) | | | | Tape & Reel |
| FAN73832N | 8-DIP | | | Tube |

**Note:**

1. These devices passed wave soldering test by JESD22A-111.

## Typical Application Diagrams

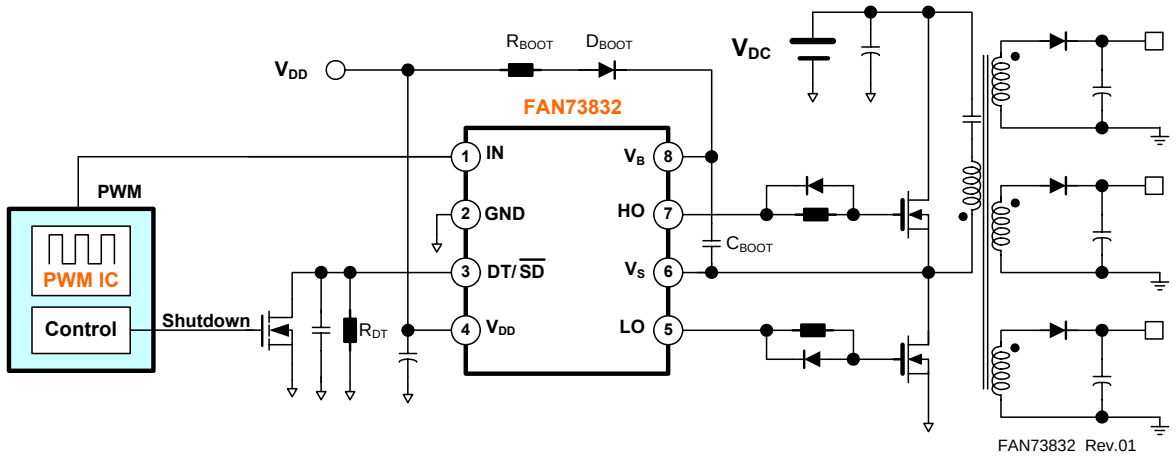


**Figure 1. Application Circuit for Half-Bridge Switching Power Supply**

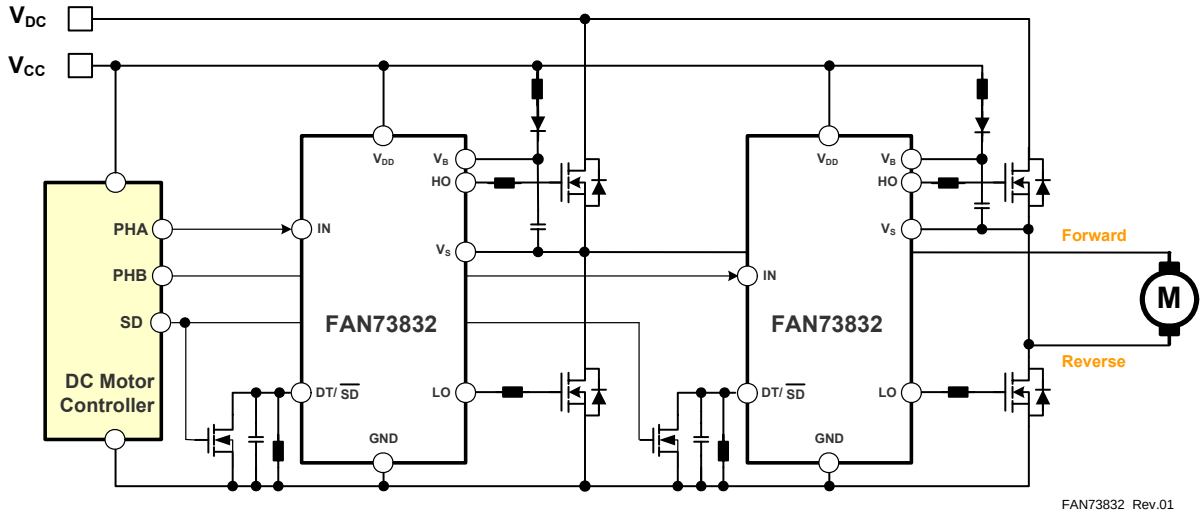


**Figure 2. Application Circuit for Full-Bridge DC Motor Driver**

## Internal Block Diagram

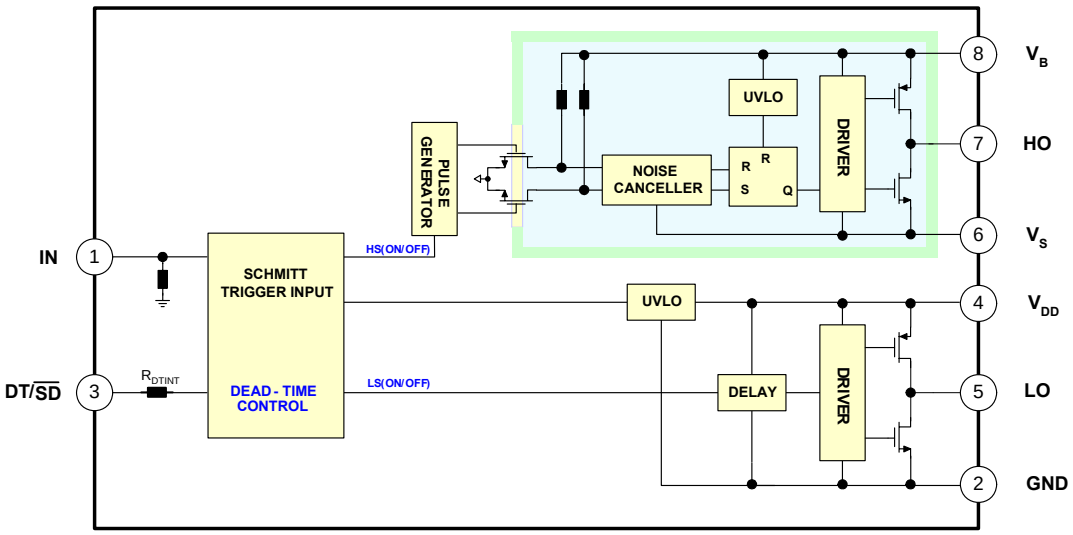


**Figure 3. Functional Block Diagram of FAN73832**

## Pin Assignments

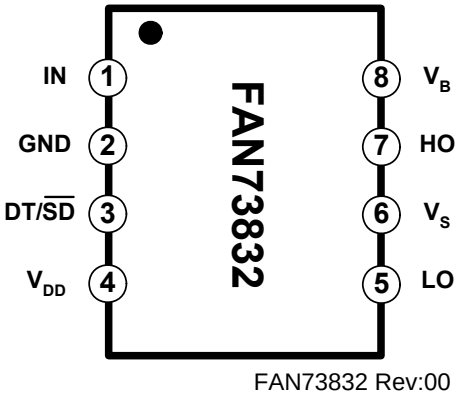


**Figure 4. Pin Configuration (Top View)**

## Pin Definitions

| Pin # | Name | Description |
|---|---|---|
| 1 | IN | Logic Input |
| 2 | GND | Ground |
| 3 | DT/$\overline{SD}$ | Dead-Time Control with External Resistor and Shutdown Function |
| 4 | $V_{DD}$ | Low-Side Supply Voltage |
| 5 | LO | Low-Side Driver Output |
| 6 | $V_S$ | High-Side Floating Supply Return |
| 7 | HO | High-Side Driver Output |
| 8 | $V_B$ | High-Side Floating Supply |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $T_A$=25°C unless otherwise specified.

| Symbol | Parameter | | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_S$ | High-side offset voltage | | $V_B$-25 | $V_B$+0.3 | V |
| $V_B$ | High-side floating supply voltage | | -0.3 | 625 | V |
| $V_{HO}$ | High-side floating output voltage HO | | $V_S$-0.3 | $V_B$+0.3 | V |
| $V_{DD}$ | Low-side and logic-fixed supply voltage | | -0.3 | 25 | V |
| $V_{LO}$ | Low-side output voltage LO | | -0.3 | $V_{DD}$+0.3 | V |
| $V_{IN}$ | Logic input voltage (IN) | | -0.3 | $V_{DD}$+0.3 | V |
| $V_{DT/\overline{SD}}$ | Dead-time and shutdown control voltage | | -0.3 | 5.0 | V |
| GND | Logic ground | | $V_{DD}$-25 | $V_{DD}$+0.3 | V |
| $dV_S/dt$ | Allowable offset voltage slew rate | | | 50 | V/ns |
| $P_D$[2][3][4] | Power dissipation | 8-SOP | | 0.625 | W |
| | | 8-DIP | | 1.25 | |
| $\theta_{JA}$ | Thermal resistance, junction-to-ambient | 8-SOP | | 200 | °C/W |
| | | 8-DIP | | 100 | |
| $T_J$ | Junction temperature | | | 150 | °C |
| $T_{STG}$ | Storage temperature | | | 150 | °C |

**Notes:**

2. Mounted on 76.2 x 114.3 x 1.6mm PCB (FR-4 glass epoxy material).
3. Refer to the following standards:
   JESD51-2: Integral circuits thermal test method environmental conditions - Natural convection
   JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages
4. Do not exceed $P_D$ under any circumstances.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_B$ | High-side floating supply voltage | | $V_S$+15 | $V_S$+20 | V |
| $V_S$ | High-side floating supply offset voltage | | 6-$V_{DD}$ | 600 | V |
| $V_{DD}$ | Low-side supply voltage | | 15 | 20 | V |
| $V_{HO}$ | High-side (HO) output voltage | | $V_S$ | $V_B$ | V |
| $V_{LO}$ | Low-side (LO) output voltage | | GND | $V_{DD}$ | V |
| $V_{IN}$ | Logic input voltage (IN) | | GND | $V_{DD}$ | V |
| $T_A$ | Ambient temperature | | -40 | 125 | °C |

## Electrical Characteristics

$V_{BIAS}$ ($V_{DD}$, $V_{BS}$)=15.0V, $R_{DT}$=20KΩ,$T_A$=25°C, unless otherwise specified. The $V_{IN}$ and $I_{IN}$ parameters are referenced to GND. The $V_O$ and $I_O$ parameters are referenced to $V_S$ and COM and are applicable to the respective outputs HO and LO.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT SECTION** | | | | | | |
| $I_{QBS}$ | Quiescent $V_{BS}$ supply current | $V_{IN}$=0V or 5V | | 35 | 90 | µA |
| $I_{QDD}$ | Quiescent $V_{DD}$ supply current | $V_{IN}$=0V or 5V, $R_{DT}$=20KΩ | | 300 | 450 | |
| $I_{SD}$(5) | Shutdown supply current | DT/$\overline{SD}$=GND | | 650 | 900 | |
| $I_{PBS}$ | Operating $V_{BS}$ supply current | $f_{IN}$=20kHz, rms value | | 400 | 700 | |
| $I_{PDD}$ | Operating $V_{DD}$ supply current | $f_{IN}$=20kHz, rms value | | 650 | 850 | |
| $I_{LK}$ | Offset supply leakage current | $V_B$=$V_S$=600V | | | 10 | |
| **POWER SUPPLY SECTION** | | | | | | |
| $V_{DDUV+}$ $V_{BSUV+}$ | $V_{DD}$ and $V_{BS}$ supply under-voltage positive going threshold | | 10.7 | 11.6 | 12.5 | V |
| $V_{DDUV-}$ $V_{BSUV-}$ | $V_{DD}$ and $V_{BS}$ supply under-voltage negative going threshold | | 10.0 | 10.8 | 11.6 | V |
| $V_{DDUVH}$ $V_{BSUVH}$ | $V_{DD}$ supply under-voltage lockout hysteresis | | | 0.8 | | V |
| **DEAD-TIME CONTROL SECTION** | | | | | | |
| $R_{DTINT}$ | Internal dead-time setting resistance | | | 20 | | KΩ |
| $V_{DT}$ | Normal voltage at DT | $R_{DT}$=20KΩ | | 3.0 | | V |
| **GATE DRIVER OUTPUT SECTION** | | | | | | |
| $V_{OH}$ | High-level output voltage, $V_{BIAS}$-$V_O$ | $I_O$=20mA | | | 1.0 | V |
| $V_{OL}$ | Low-level output voltage, $V_O$ | | | | 0.6 | V |
| $I_{O+}$ | Output high short-circuit pulse current | $V_O$=0V, $V_{IN}$=5V with PW<10µs | 250 | 350 | | mA |
| $I_{O-}$ | Output low short-circuit pulsed current | $V_O$=15V, $V_{IN}$=0V with PW<10µs | 500 | 650 | | mA |
| $V_S$ | Allowable negative $V_S$ pin voltage for IN signal propagation to HO | | | -9.8 | -7.0 | V |
| **LOGIC INPUT SECTION (INPUT and SHUTDOWN)** | | | | | | |
| $V_{IH}$ | Logic "1" input voltage | | 2.9 | | | V |
| $V_{IL}$ | Logic "0" input voltage | | | | 1.2 | V |
| $I_{IN+}$ | Logic "1" input bias current | $V_{IN}$=5V | | 50 | 100 | µA |
| $I_{IN-}$ | Logic "0" input bias current | $V_{IN}$=0V | | | 2.0 | µA |
| $\overline{SD+}$ | Shutdown "1" input voltage | | | | 1.2 | V |
| $\overline{SD-}$ | Shutdown "0" input voltage | | 2.9 | | | V |
| $R_{PD}$ | Input pull-down resistance | | | 100 | | KΩ |

**Note:**

5. This parameter guaranteed by design.

## Dynamic Electrical Characteristics

$V_{BIAS}$ ($V_{DD}$, $V_{BS}$)=15.0V, $V_S$=GND, $C_L$=1000pF, $R_{DT}$=20KΩ and $T_A$ = 25°C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{ON}$ | Turn-on propagation delay | $V_S$=0V, $R_{DT}$=20KΩ | | 580 | 730 | ns |
| $t_{OFF}$ | Turn-off propagation delay | $V_S$=0V or 600V(5), $R_{DT}$=20KΩ | | 180 | 230 | |
| $t_R$ | Turn-on rise time | $C_L$=1000pF | | 50 | 100 | |
| $t_F$ | Turn-off fall time | $C_L$=1000pF | | 30 | 80 | |
| $t_{SD}$(5) | Shutdown propagation delay | | | 100 | 180 | |
| DT1, DT2 | Dead-time LO OFF to HO ON & HO OFF to LO ON | $R_{DT}$ =20KΩ | 300 | 400 | 500 | ns |
| | | $R_{DT}$ = 200KΩ | 1.20 | 1.68 | 2.30 | µs |
| DMT | Dead-time matching | $R_{DT}$ = 20KΩ | | 0 | 60 | ns |
| | | $R_{DT}$ =200KΩ | | 0 | 150 | |

**Note:**

5. These parameters guaranteed by design.

## Typical Characteristics

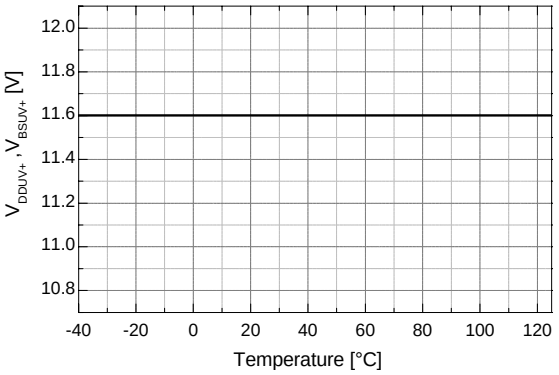


**Figure 5. $V_{DD}/V_{BS}$ UVLO (+) vs. Temperature**

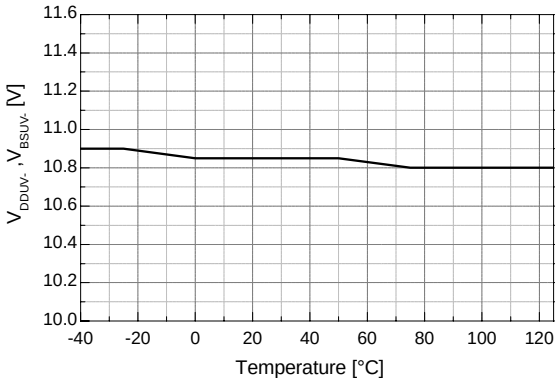


**Figure 6. $V_{DD}/V_{BS}$ UVLO (-) vs. Temperature**

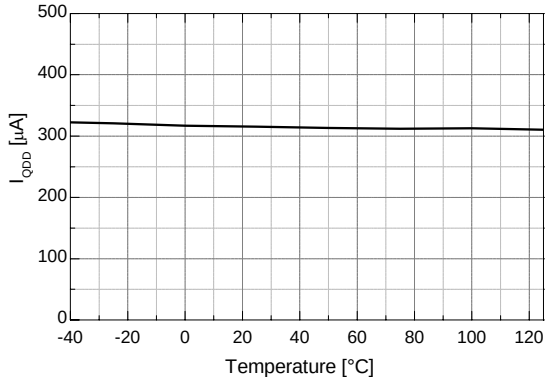


**Figure 7. $V_{DD}$ Quiescent Current vs. Temperature**

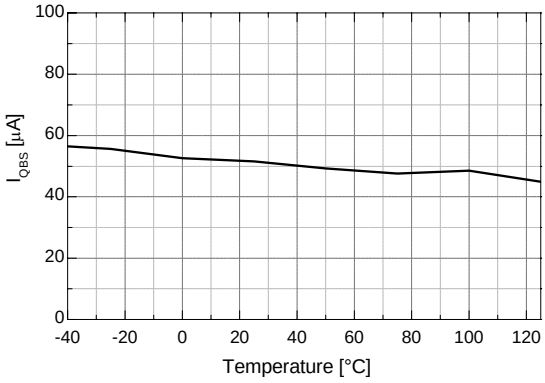


**Figure 8. $V_{BS}$ Quiescent Current vs. Temperature**

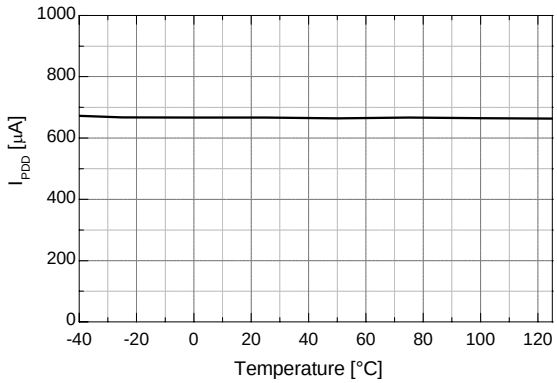


**Figure 9. $V_{DD}$ Operating Current vs. Temperature**

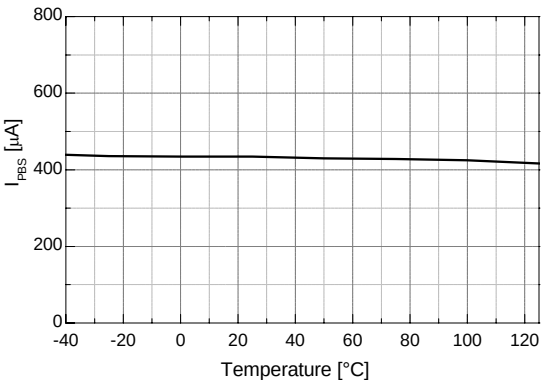


**Figure 10. $V_{BS}$ Operating Current vs. Temperature**

## Typical Characteristics (Continued)

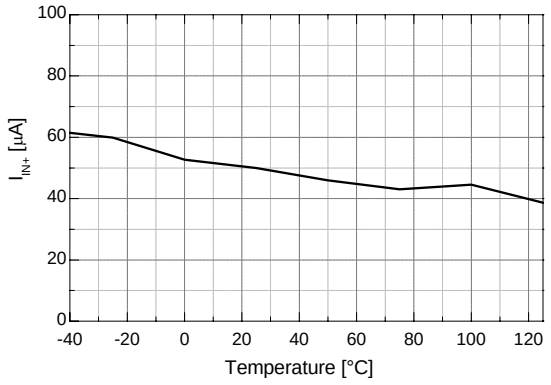


**Figure 11. Logic Input Current vs. Temperature**

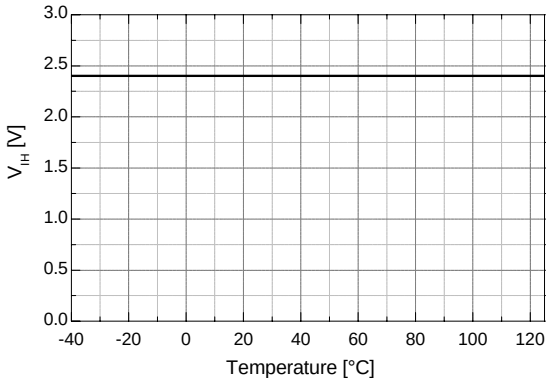


**Figure 12. Logic Input High Voltage vs. Temperature**

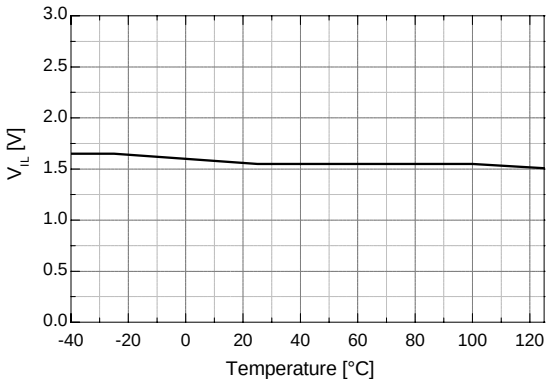


**Figure 13. Logic Input Low Voltage vs. Temperature**

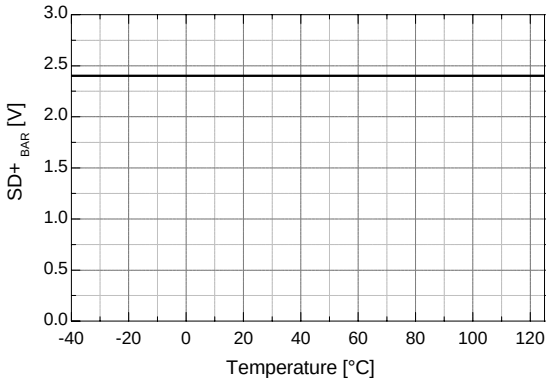


**Figure 14. $\overline{SD}$ Positive Threshold vs. Temperature**

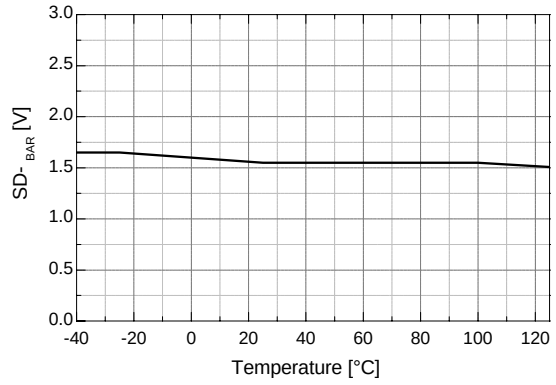


**Figure 15. $\overline{SD}$ Negative Threshold vs. Temperature**

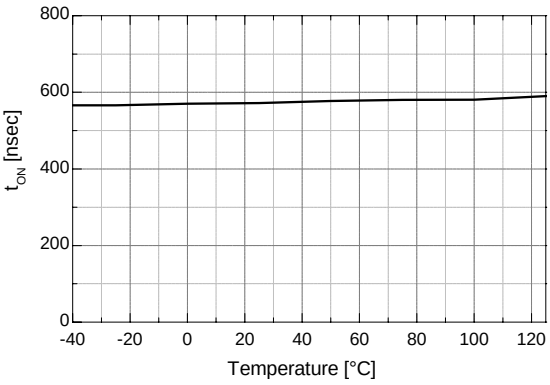


**Figure 16. Turn-on Delay Time vs. Temperature**

## Typical Characteristics (Continued)

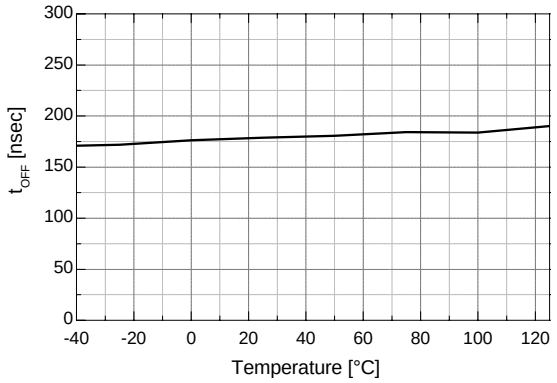


**Figure 17. Turn-off Delay Time vs. Temperature**

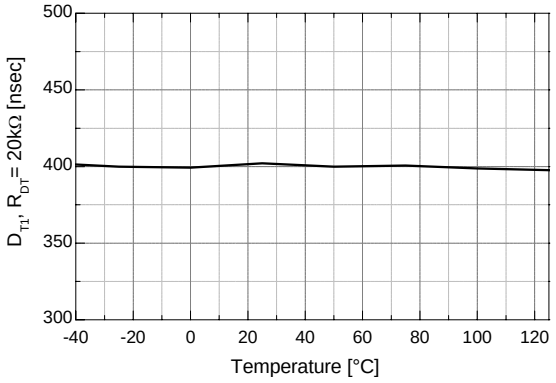


**Figure 18. Dead--Time ($R_{DT}$=20kΩ) vs. Temperature**

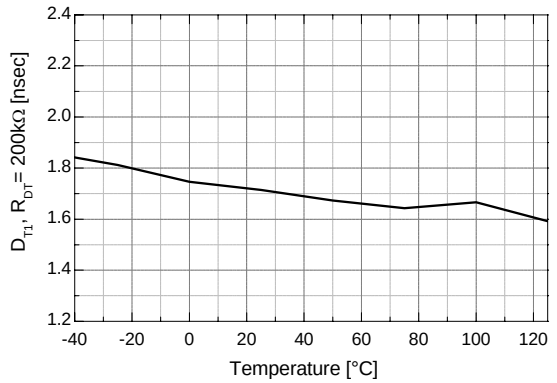


**Figure 19. Dead Time ($R_{DT}$=200kΩ) vs. Temperature**

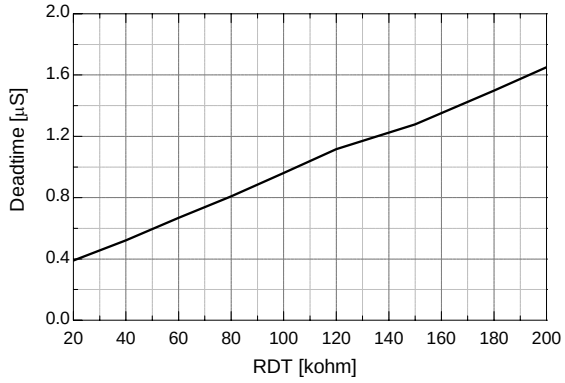


**Figure 20. $R_{DT}$ vs. Dead-Time**

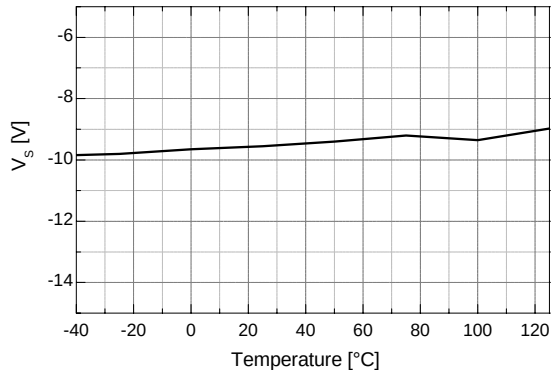


**Figure 21. Allowable Negative $V_S$ Voltage for Signal Propagation to High Side vs. Temperature**

## Switching Time Definitions

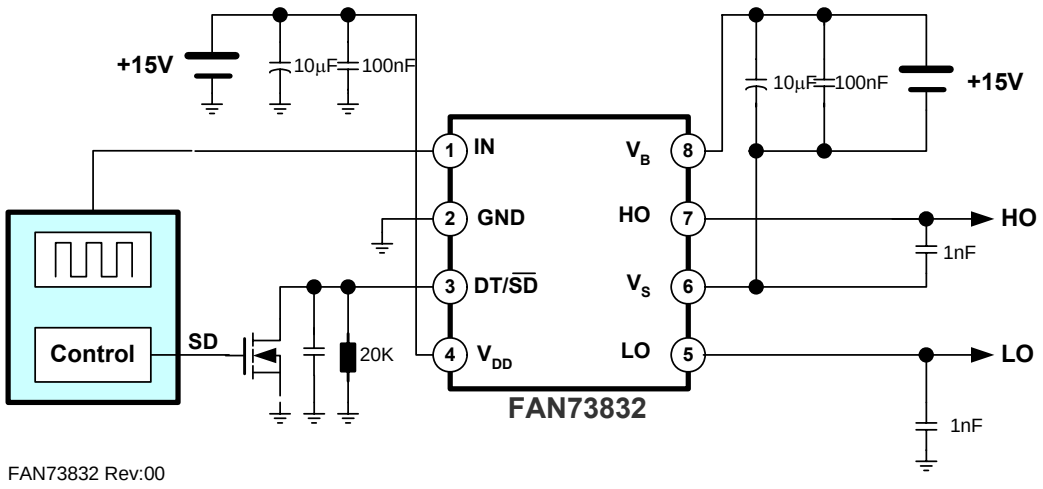


**Figure 22. Switching Time Test Circuit**

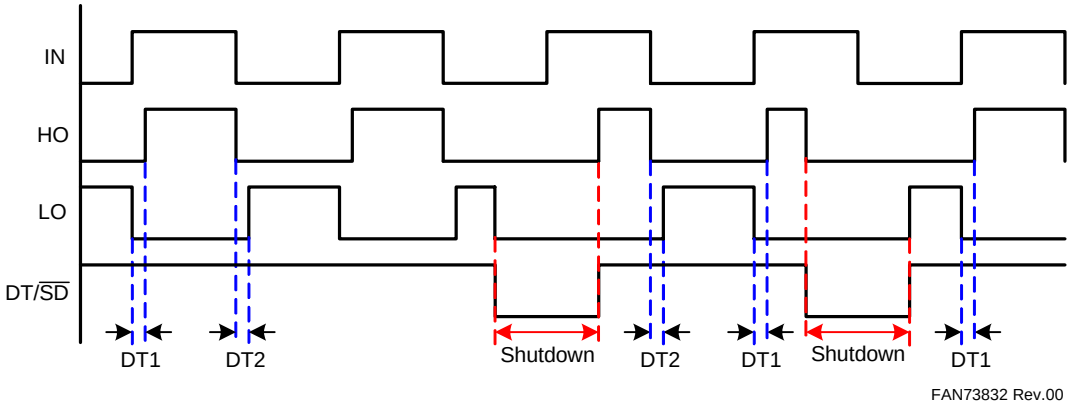


**Figure 23. Input / Output Waveforms**

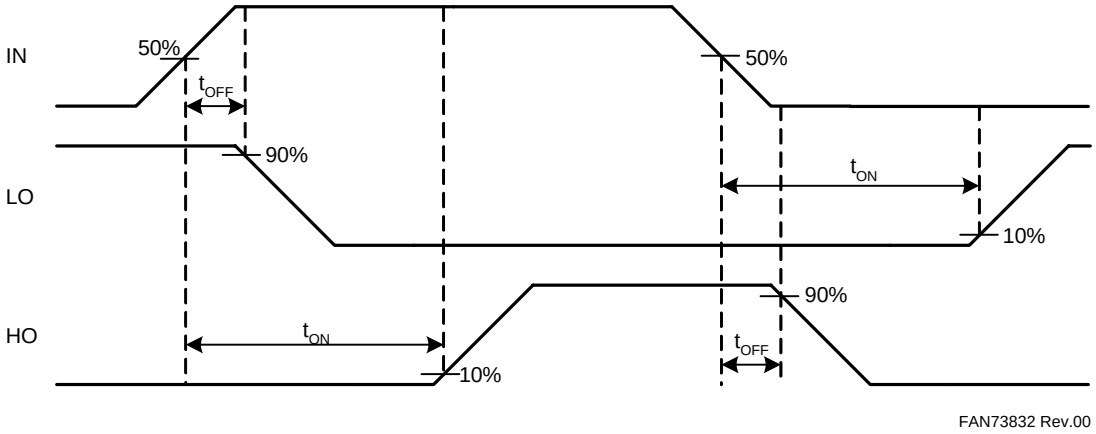


**Figure 24. Switching Time Waveform Definitions**

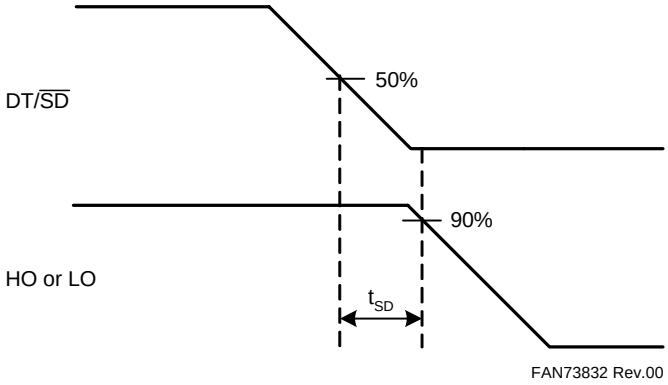


**Figure 25. Shutdown Waveform Definition**

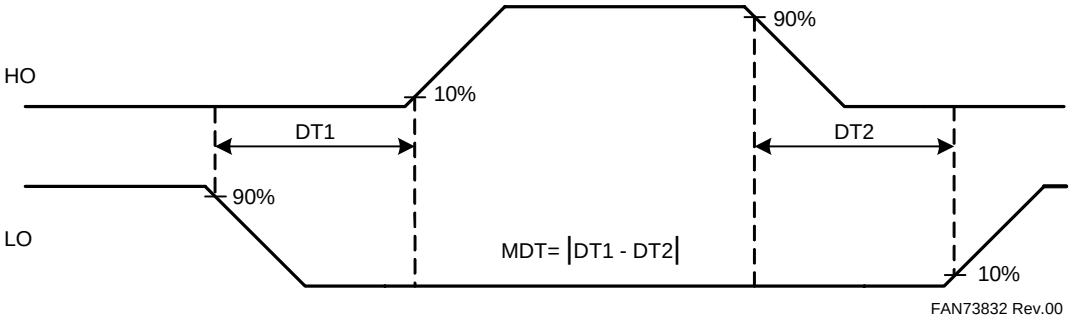


**Figure 26. Dead-Time Control Waveform Definition**

## Typical Application Information

### 1. Normal Operating Consideration

The FAN73832 is a single PWM input, half-bridge, gate-drive IC with programmable dead-time and shutdown functions.

The dead-time is set with a resistor ($R_{DT}$) at the DT/$\overline{SD}$ pin. The wide dead-time programming range provides the flexibility to optimize drive signal timing for a selection of switching devices (MOSFET or IGBT) and applications.

The turn-on time delay circuitry (Dead-Time) accommodates resistor values from 20kΩ to 200kΩ with a dead-time proportional to the $R_{DT}$ resistance.

If the DT/$\overline{SD}$ pin voltage decreases below 1.2V in the normal operation, the IC enters shutdown mode.

The external dead-time setting resistor ($R_{DT}$) is at least above 20KΩ for normal operation in typical applications.

### 2. Under-Voltage Lockout (UVLO)

The FAN73832 has an under-voltage lockout (UVLO) protection circuit for high- and low-side channels to prevent malfunction when $V_{DD}$ and $V_{BS}$ are lower than the specified threshold voltage. The UVLO circuitry monitors the supply voltage ($V_{DD}$) and bootstrap capacitor voltage ($V_{BS}$) antepenult.

### 3. Layout Consideration

For optimum performance of the high- and low-side gate drivers, considerations must be taken during printed circuit board (PCB) layout.

#### 3.1 Supply Capacitors

If the output stages are able to quickly turn-on a switching device with a high value of current, the supply capacitors must be placed as close as possible to the device pins ($V_{DD}$ and GND for the ground-tied supply, $V_B$ and $V_S$ for the floating supply) to minimize parasitic inductance and resistance.

#### 3.2 Gate Drive Loop

Current loops behave like an antenna, able to receive and transmit noise. To reduce the noise coupling/emission and improve the power switch turn-on and off performances, gate drive loops must be reduced as much as possible.

#### 3.3 Ground Plane

Ground plane must not be placed under or nearby the high-voltage floating side to minimize noise coupling.

## Mechanical Dimensions

### 8-SOP

Dimensions are in millimeters (inches) unless otherwise noted.

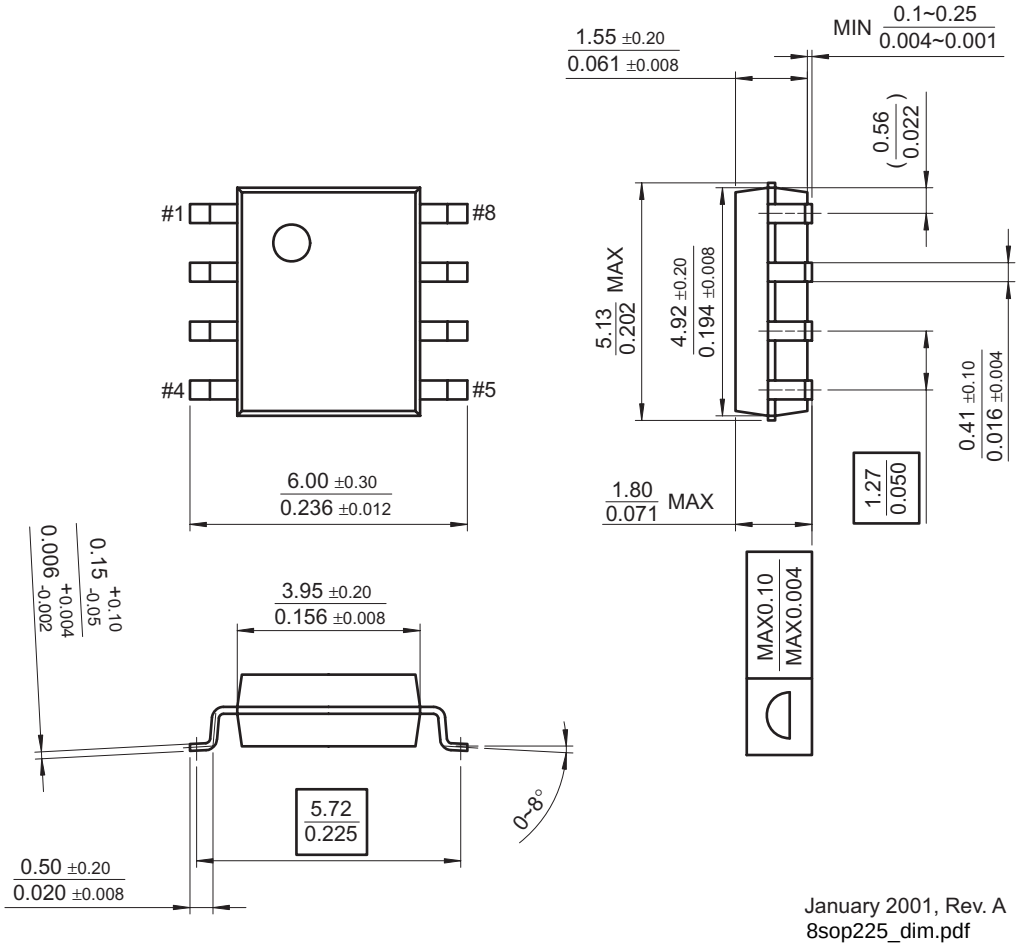


**Figure 27. 8-Lead Small Outline Package (SOP)**

## Mechanical Dimensions (Continued)

### 8-DIP

Dimensions are in millimeters (inches) unless otherwise noted.

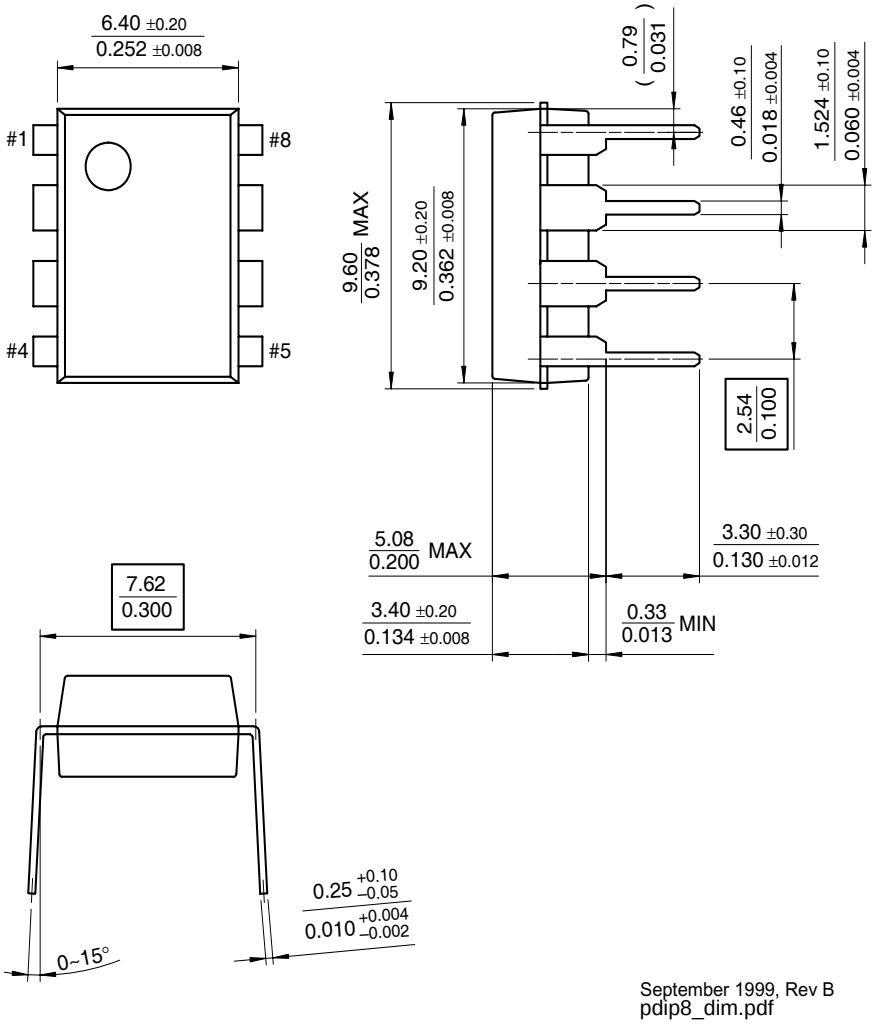


**Figure 28. 8-Lead Dual In-Line Package (DIP)**

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Current Transfer Logic™
DOME™
E²CMOS™
EcoSPARK®
EnSigna™
FACT Quiet Series™
FACT®
FAST®
FASTr™
FPS™
FRFET®
GlobalOptoisolator™
GTO™
HiSeC™
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## PRODUCT STATUS DEFINITIONS

**Definition of Terms**

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