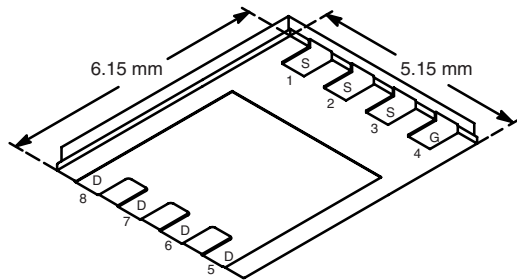




N-Channel 80 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
80	0.0059 at V _{GS} = 10 V	60	23 nC
	0.0067 at V _{GS} = 7.5 V	60	
	0.0085 at V _{GS} = 4.5 V	60	

PowerPAK® SO-8



Bottom View

Ordering Information: SiR880DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

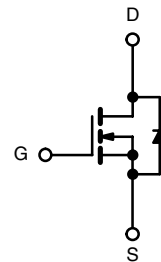
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC


RoHS
 COMPLIANT
 HALOGEN
 FREE

APPLICATIONS

- Fixed Telecom
- POL
- DC/DC Converter
- Primary Side Switch



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	80	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	60 ^a	A
		T _C = 70 °C	60 ^a	
		T _A = 25 °C	23 ^{b, c}	
		T _A = 70 °C	18.4 ^{b, c}	
Pulsed Drain Current	I _{DM}	100		
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	60 ^a	
		T _A = 25 °C	5.6 ^{b, c}	
Single Pulse Avalanche Current	I _{AS}	35		
Single Pulse Avalanche Energy	E _{AS}	61	mJ	
Maximum Power Dissipation	P _D	T _C = 25 °C	104	W
		T _C = 70 °C	66.6	
		T _A = 25 °C	6.25 ^{b, c}	
		T _A = 70 °C	4.0 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{d, e}		260		

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	t ≤ 10 s	R _{thJA}	15	20	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	0.9	1.2	

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 54 °C/W.

SiR880DP

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SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	80			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		36		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 5.8		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.2		2.8	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		0.0049	0.0059	Ω
		$V_{GS} = 7.5\text{ V}, I_D = 20\text{ A}$		0.0054	0.0067	
		$V_{GS} = 4.5\text{ V}, I_D = 15\text{ A}$		0.0070	0.0085	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$		64		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		2440		pF
Output Capacitance	C_{oss}			1525		
Reverse Transfer Capacitance	C_{rss}			100		
Total Gate Charge	Q_g	$V_{DS} = 40\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		49	74	nC
		$V_{DS} = 40\text{ V}, V_{GS} = 7.5\text{ V}, I_D = 20\text{ A}$		37.2	56	
Gate-Source Charge	Q_{gs}	$V_{DS} = 40\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		23	35	
Gate-Drain Charge	Q_{gd}			7.6		
Gate Resistance	R_g			9.2		
Turn-On Delay Time	$t_{d(on)}$	$f = 1\text{ MHz}$	0.4	2.1	4.2	Ω
Rise Time	t_r					
Turn-Off Delay Time	$t_{d(off)}$					
Fall Time	t_f					
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 40\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong 20\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		12	24	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			38	70	
Fall Time	t_f			11	22	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 40\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong 20\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		30	55	
Rise Time	t_r			26	50	
Turn-Off Delay Time	$t_{d(off)}$			40	75	
Fall Time	t_f			12	24	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			60	A
Pulse Diode Forward Current ^a	I_{SM}				100	
Body Diode Voltage	V_{SD}	$I_S = 5\text{ A}$		0.75	1.1	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 20\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		56	100	ns
Body Diode Reverse Recovery Charge	Q_{rr}			66	120	nC
Reverse Recovery Fall Time	t_a			23		ns
Reverse Recovery Rise Time	t_b			33		

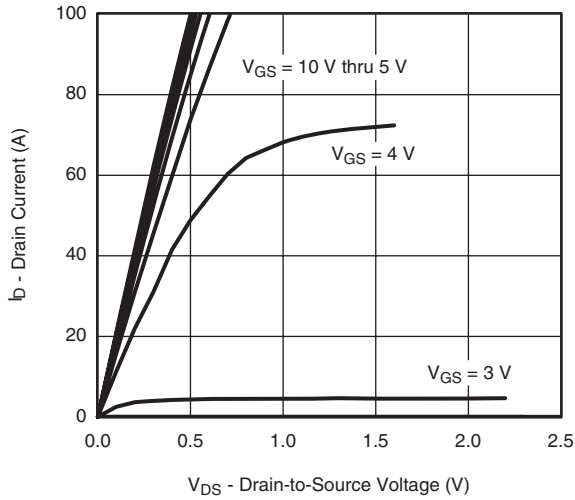
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

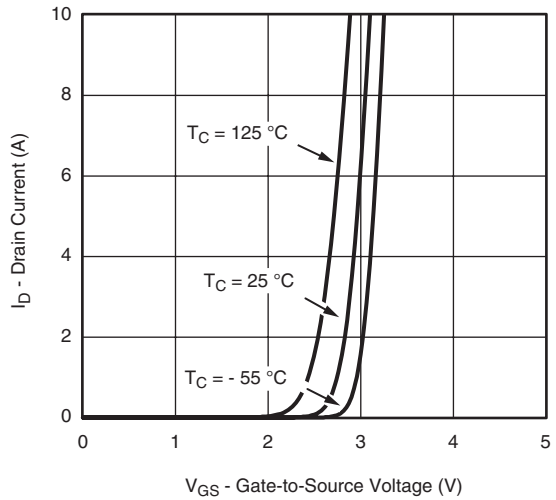
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



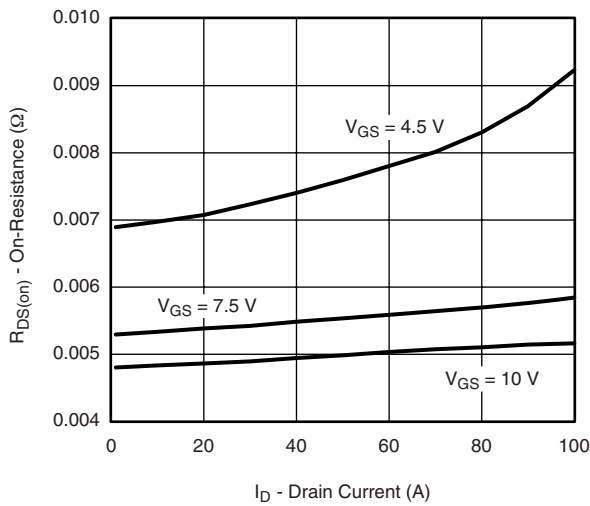
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



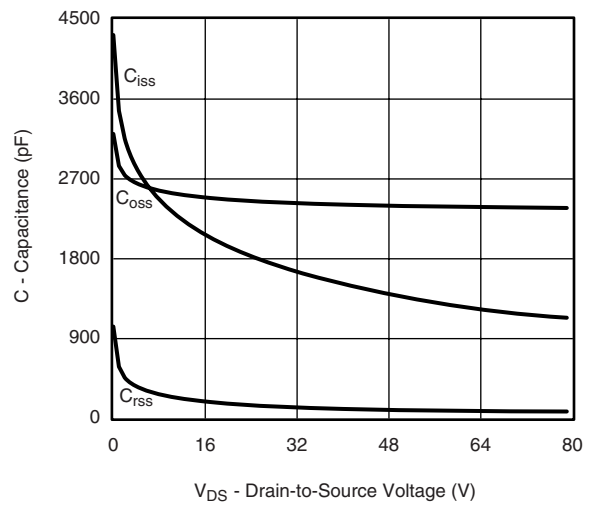
Output Characteristics



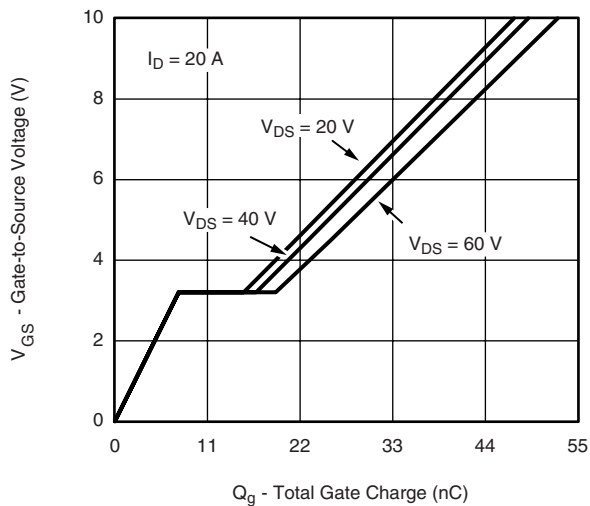
Transfer Characteristics



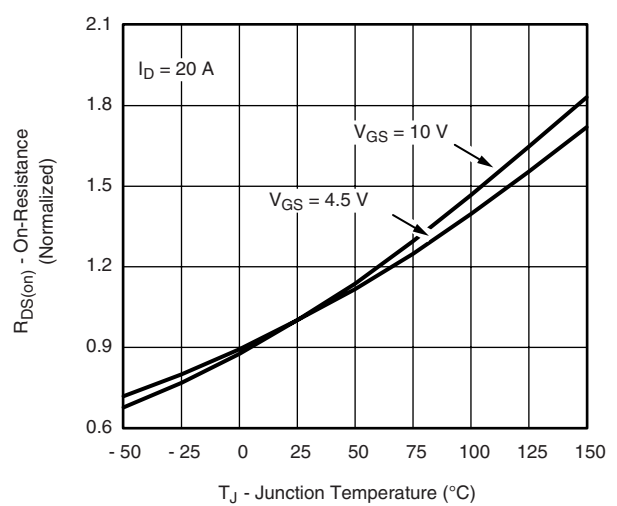
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge



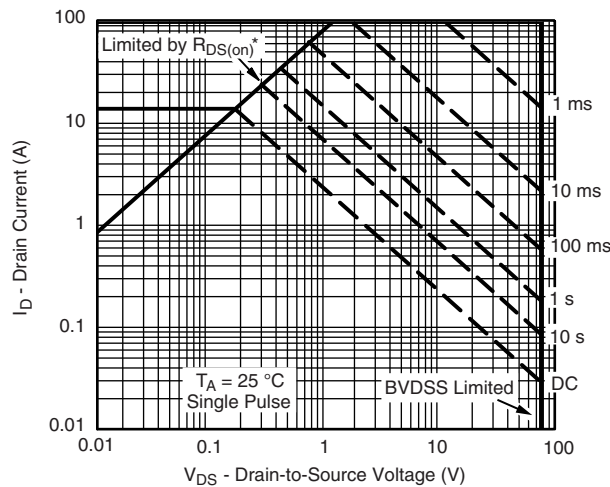
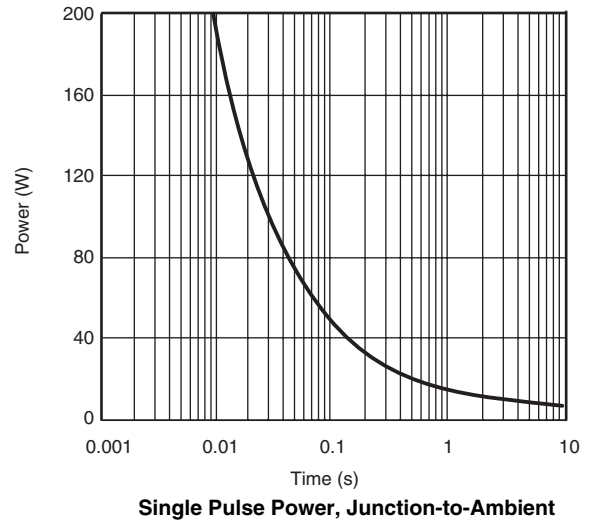
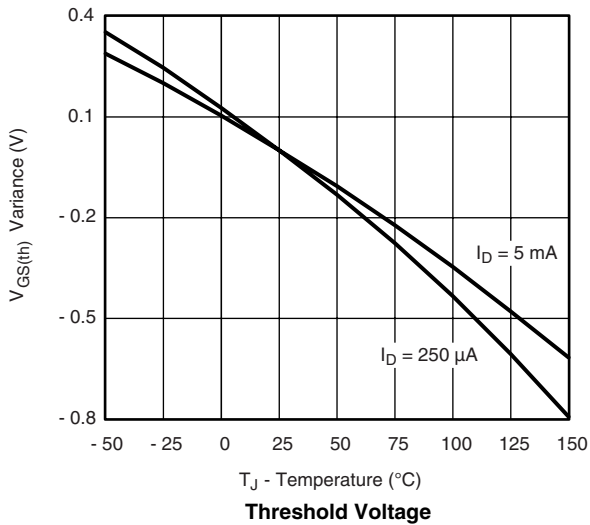
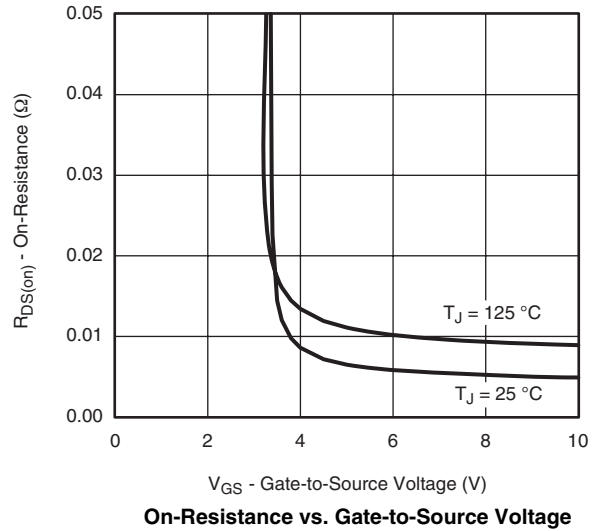
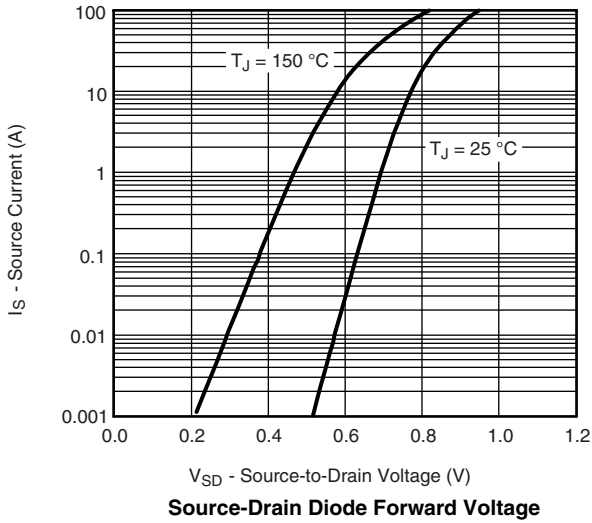
On-Resistance vs. Junction Temperature

SiR880DP



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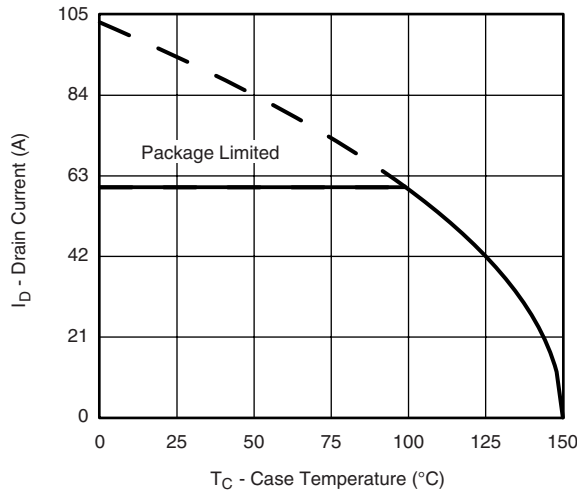
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



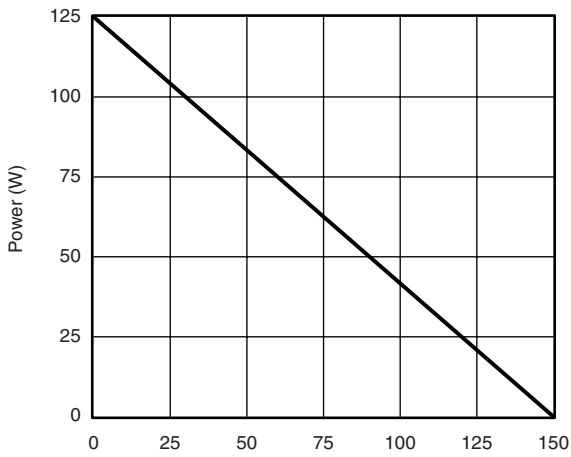
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified
Safe Operating Area, Junction-to-Ambient



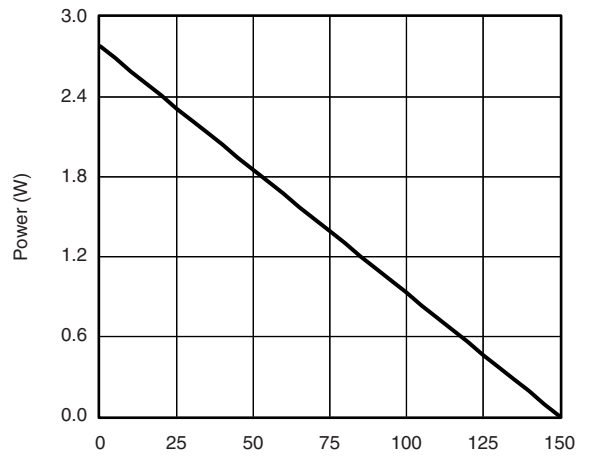
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



Power, Junction-to-Case



Power, Junction-to-Ambient

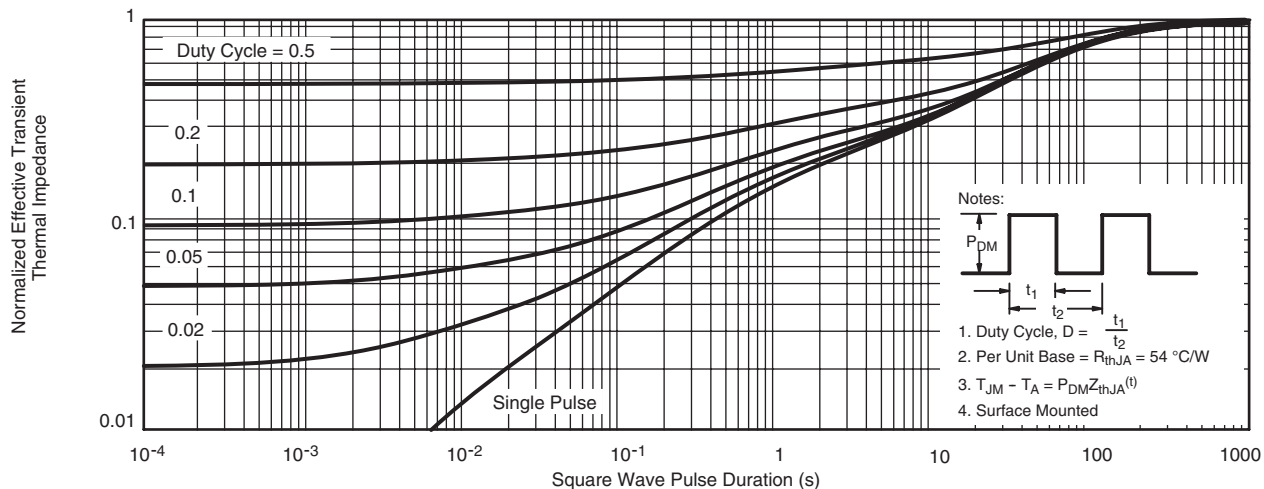
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

SiR880DP

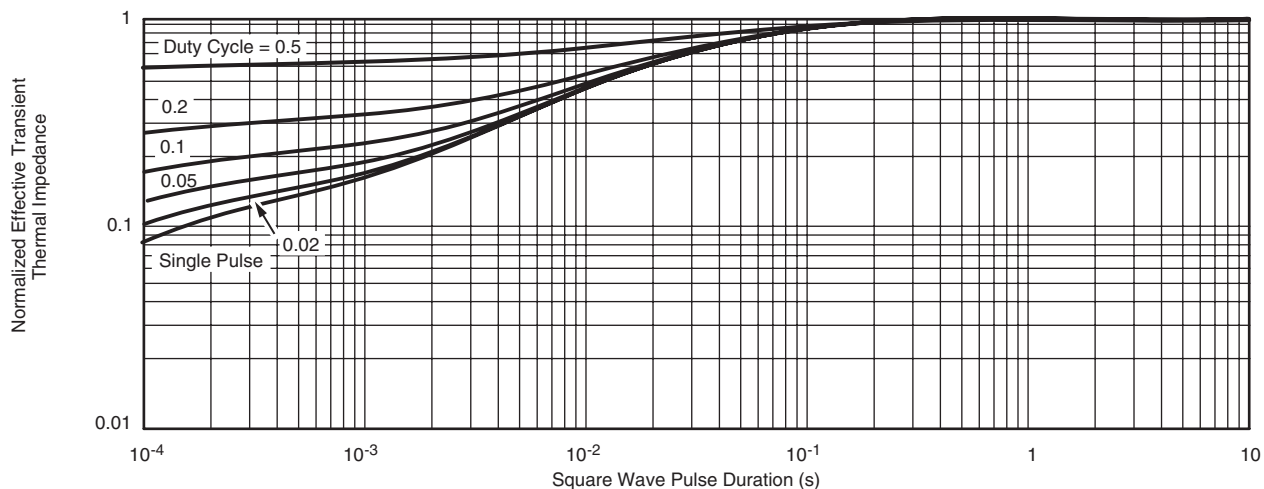


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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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