

## N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)
40	0.0023 at V <sub>GS</sub> = 10 V	60	45.5 nC
	0.00265 at V <sub>GS</sub> = 4.5 V	60	

### FEATURES

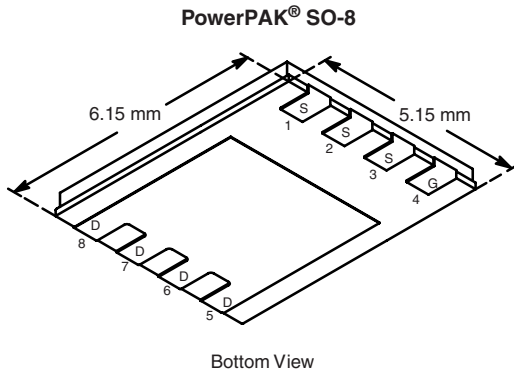
- Halogen-free
- TrenchFET<sup>®</sup> Gen III Power MOSFET
- 100 % R<sub>G</sub> Tested
- 100 % UIS Tested



RoHS  
COMPLIANT

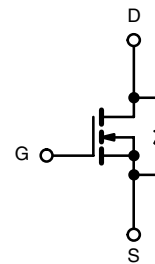
### APPLICATIONS

- Secondary Side Synchronous Rectification
- Power Supply



Bottom View

Ordering Information: SiR470DP-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	40	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	60 <sup>a</sup>
		T <sub>C</sub> = 70 °C	60 <sup>a</sup>
		T <sub>A</sub> = 25 °C	38.8 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	31 <sup>b, c</sup>
Pulsed Drain Current	I <sub>DM</sub>	100	A
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	
		T <sub>A</sub> = 25 °C	5.6 <sup>b, c</sup>
Single Pulse Avalanche Current	I <sub>AS</sub>	50	mJ
Single Pulse Avalanche Energy	E <sub>AS</sub>	125	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	104
		T <sub>C</sub> = 70 °C	66.6
		T <sub>A</sub> = 25 °C	6.25 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	4.0 <sup>b, c</sup>
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 10 s	R <sub>thJA</sub>	15	20	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	0.9	1.2	

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 54 °C/W.

## SiR470DP

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SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	40			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		38		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-6.7		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0		2.5	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	30			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		0.0019	0.0023	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		0.0022	0.00265	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$		190		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		5660		pF
Output Capacitance	$C_{oss}$			720		
Reverse Transfer Capacitance	$C_{rss}$			327		
Total Gate Charge	$Q_g$	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		102	155	nC
		$V_{DS} = 20\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		45.5	70	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 20\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		13.8		
Gate-Drain Charge	$Q_{gd}$			14.4		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	0.2	1.0	2	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		16	30	ns
Rise Time	$t_r$			11	20	
Turn-Off Delay Time	$t_{d(off)}$			50	80	
Fall Time	$t_f$			9	18	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		40	75	
Rise Time	$t_r$			31	60	
Turn-Off Delay Time	$t_{d(off)}$			85	150	
Fall Time	$t_f$			39	75	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			60	A
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$				100	
Body Diode Voltage	$V_{SD}$	$I_S = 5\text{ A}$		0.73	1.1	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		39	75	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			53	105	nC
Reverse Recovery Fall Time	$t_a$			24		ns
Reverse Recovery Rise Time	$t_b$			15		

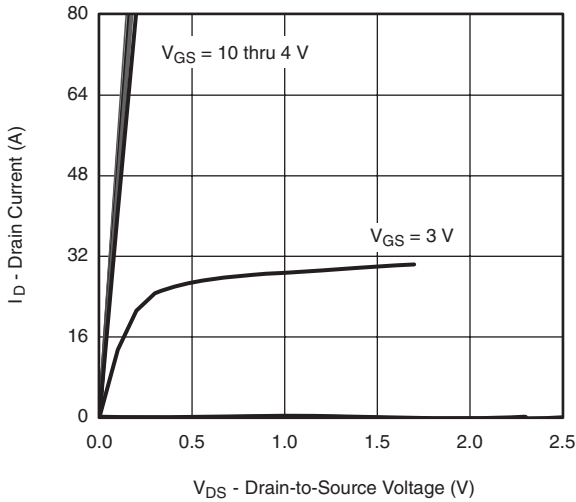
Notes:

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.

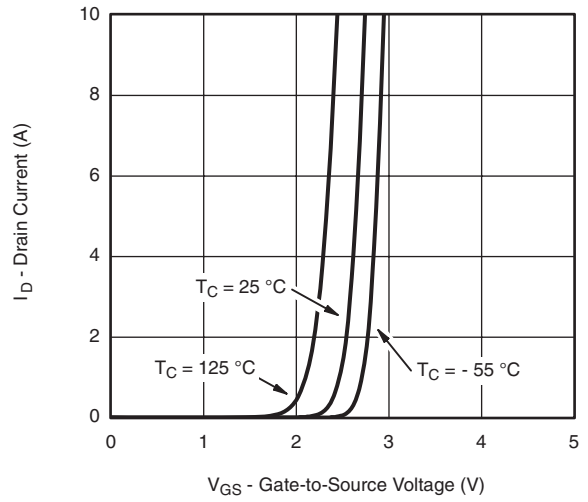
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



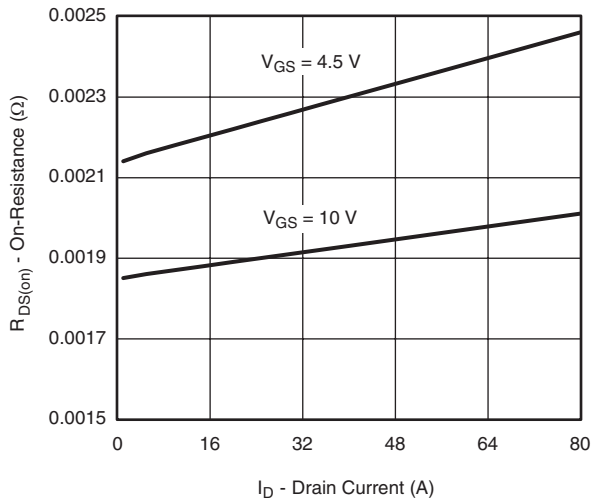
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



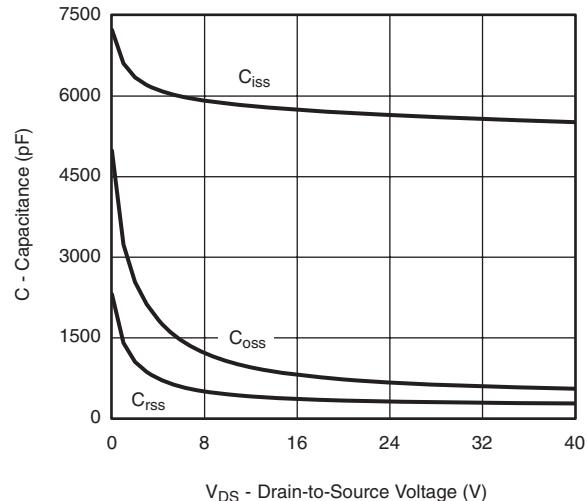
**Output Characteristics**



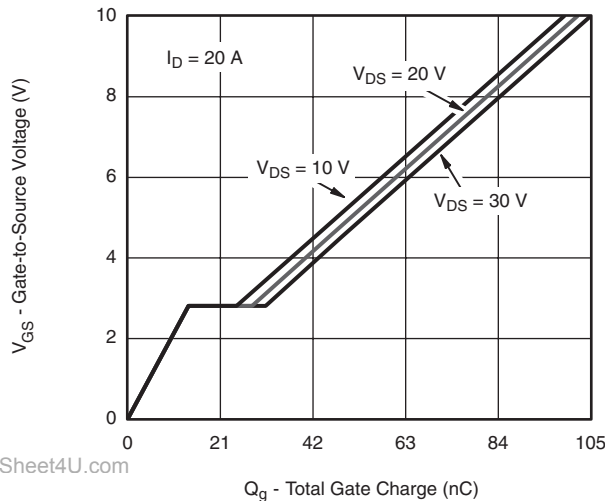
**Transfer Characteristics**



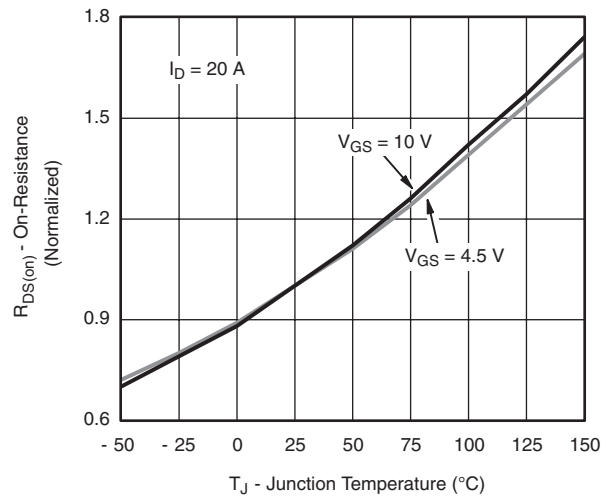
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**



**Gate Charge**



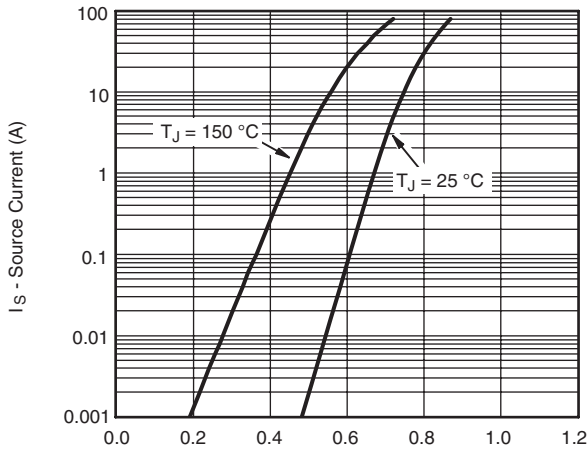
**On-Resistance vs. Junction Temperature**

# SiR470DP

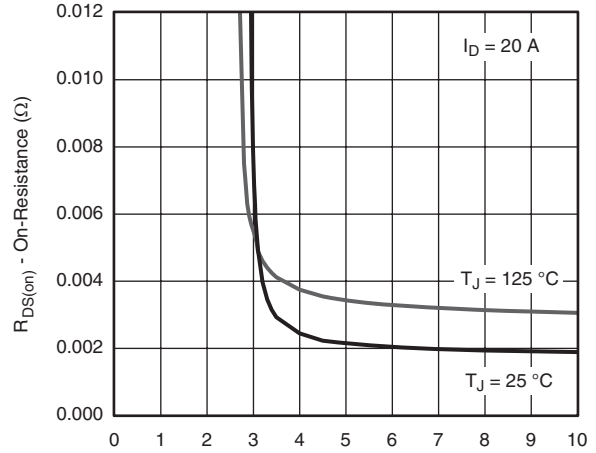
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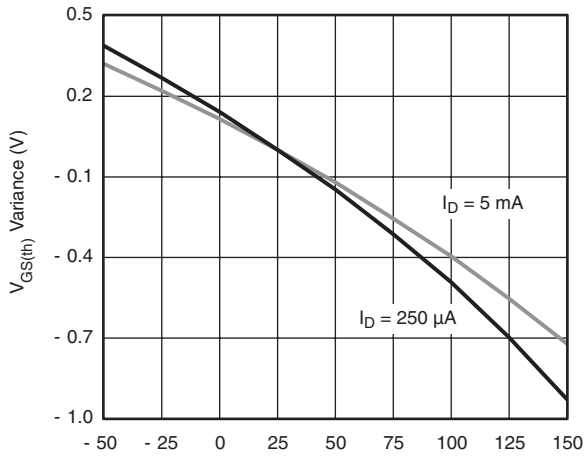
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



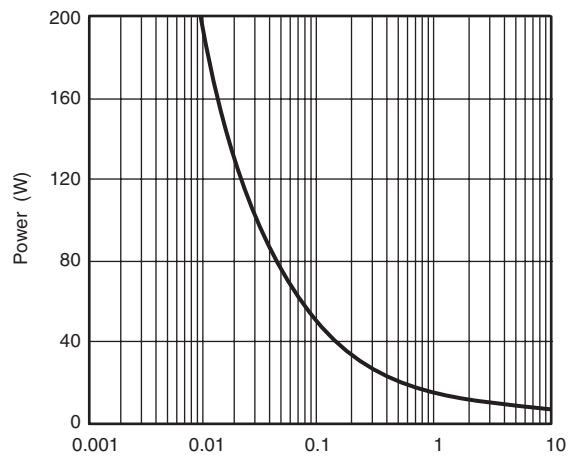
$V_{SD}$  - Source-to-Drain Voltage (V)  
Source-Drain Diode Forward Voltage



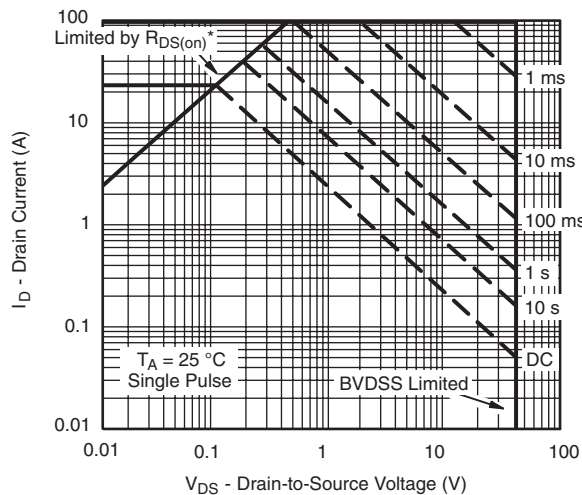
$V_{GS}$  - Gate-to-Source Voltage (V)  
On-Resistance vs. Gate-to-Source Voltage



$T_J$  - Temperature ( $^\circ\text{C}$ )  
Threshold Voltage



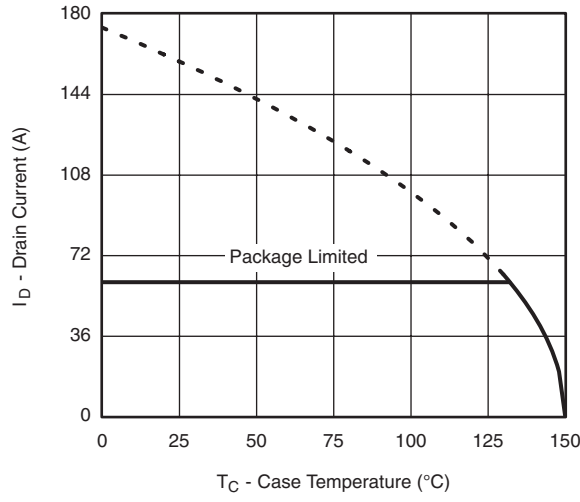
Single Pulse Power, Junction-to-Ambient



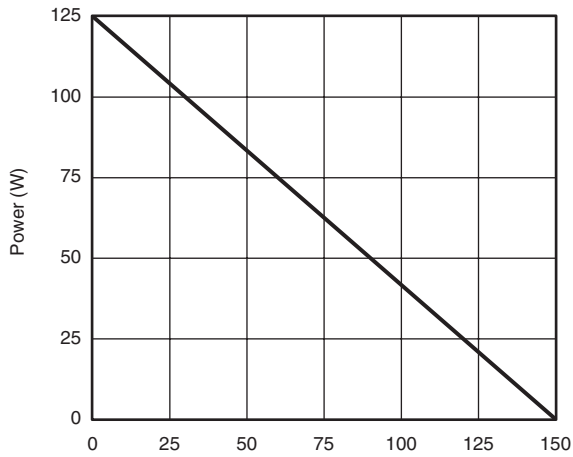
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified  
Safe Operating Area, Junction-to-Ambient



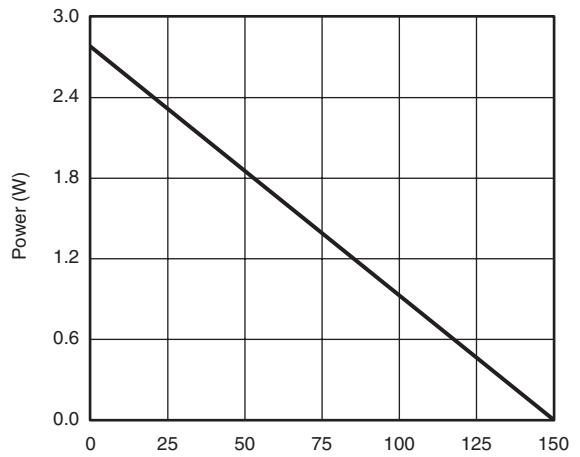
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**Current Derating\***



**Power, Junction-to-Case**



**Power, Junction-to-Ambient**

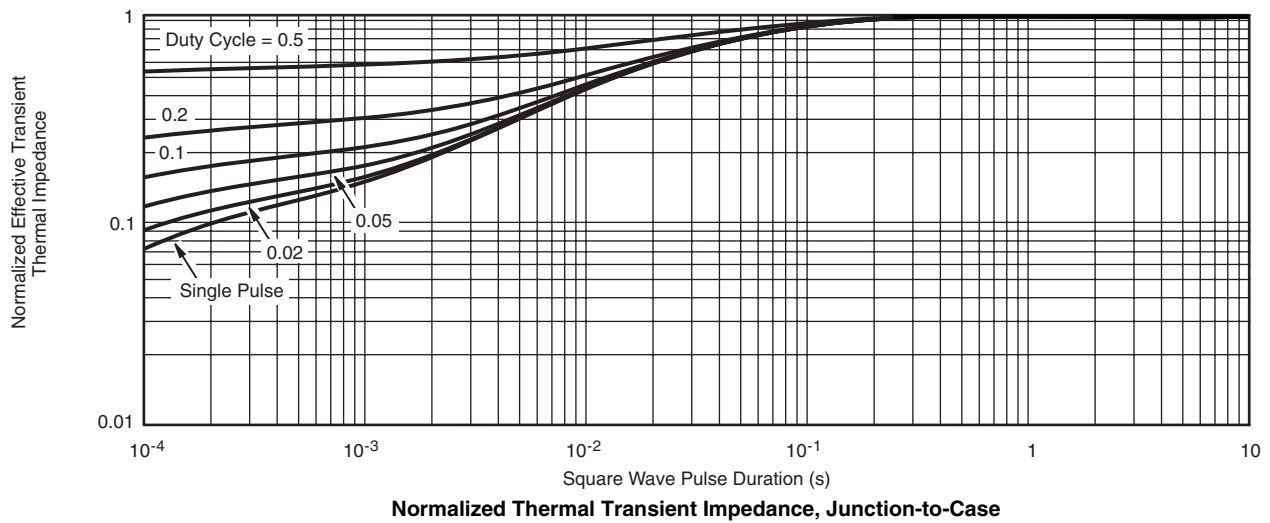
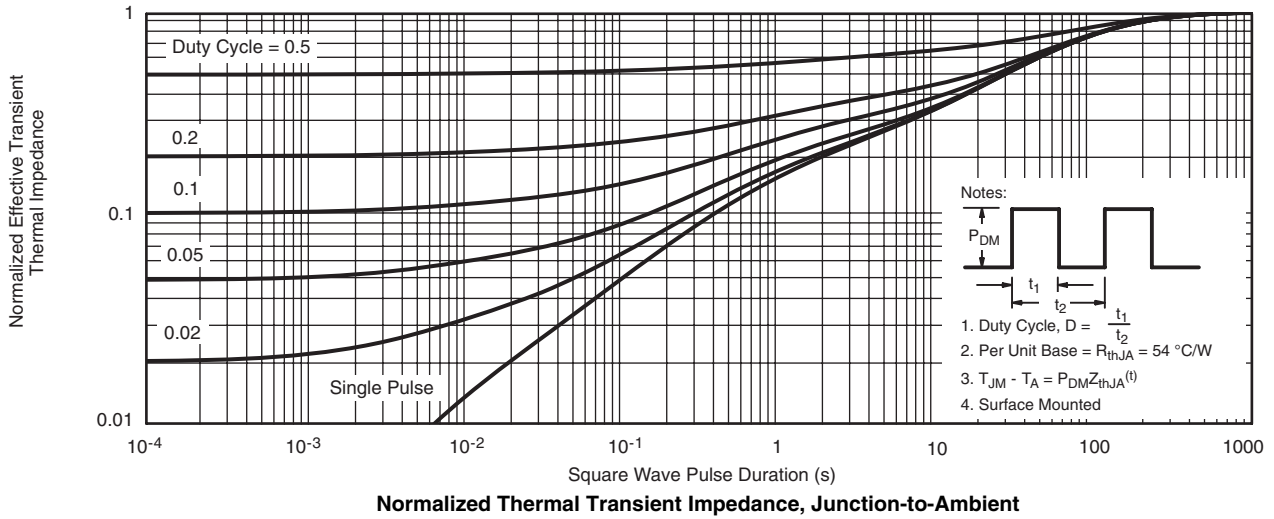
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

# SiR470DP



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## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





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