Design Considerations for Interfacing SDRAM with MC68VZ328

Application Note

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PRELIMINARY

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Abstract and Contents

The MC68VZ328 (DragonBall™ VZ) adds support for Synchronous DRAM (SDRAM) directly in its DRAM controller. This application note will provide information on the setup and use of the DragonBall VZ to access SDRAM. This is a pre-publication draft.

This application note will run through all aspects of the DragonBall VZ operation that relates to SDRAM.

1 Introduction

This application note provides information for users who are preparing to use Synchronous DRAM (SDRAM) with the MC68VZ328 (VZ). This document is a pre-publication draft.

The following issues are covered in this application note:

1. Physical interface between SDRAM and MC68VZ328.
2. Relevant control registers for SDRAM operation in the MC68VZ328 memory controller.
3. SDRAM Initialization sequences.
4. SDRAM Power control features.
5. SDRAM Logic Analyser Captures.

It is assumed that users have a basic understanding of the DragonBall processors and SDRAM operation. A large amount of abbreviations are used throughout this application note. Please refer to MC68VZ328 User's Manual (order number MC68VZ328UM/D) for details if needed.

1.1 Terminology

Unless otherwise specified, the following terms and abbreviation are as defined below.

Table 1. Terminology

Terms	Description
CPU	The 68K core in the DragonBall Processor.
LCDC	LCD Controller module in the DragonBall Processor.
*UDS	Upper Data Strob signal from the 68K core, this is muxed with Port K3 (PK3/$\overline{\text{UDS}}$)
*SDCS0	SDRAM Chip Select 0, muxed with Port B4 (PB4/$\overline{\text{CSD0}}$/$\overline{\text{CAS0}}$/$\overline{\text{SDCS0}}$)
*SDCAS	SDRAM CAS Signal, muxed with Port B3 (PB3/$\overline{\text{CSC1}}$/$\overline{\text{RAS1}}$/$\overline{\text{SDCAS}}$)
*SDRAS	SDRAM RAS Signal, muxed with Port B2 (PB2/$\overline{\text{CSC0}}$/$\overline{\text{RAS0}}$/$\overline{\text{SDRAS}}$)
*SDWE	SDRAM Write Enable Signal, muxed with Port B1 (PB1/$\overline{\text{CSB1}}$/$\overline{\text{SDWE}}$)
SDCLK	SDRAM Clock Signal, muxed with Port M0 (PM0/SDCLK)
SDCE	SDRAM Clock Enable Signal, muxed with Port M1 (PM1/SDCE)
SDA10	SDRAM Address Line 10 Signal, muxed with Port M4 (PM4/SDA10)

2 Physical Interface Between SDRAM and MC68VZ328

Recommended pin connections between the Dragon Ball VZ to SDRAM are shown below:

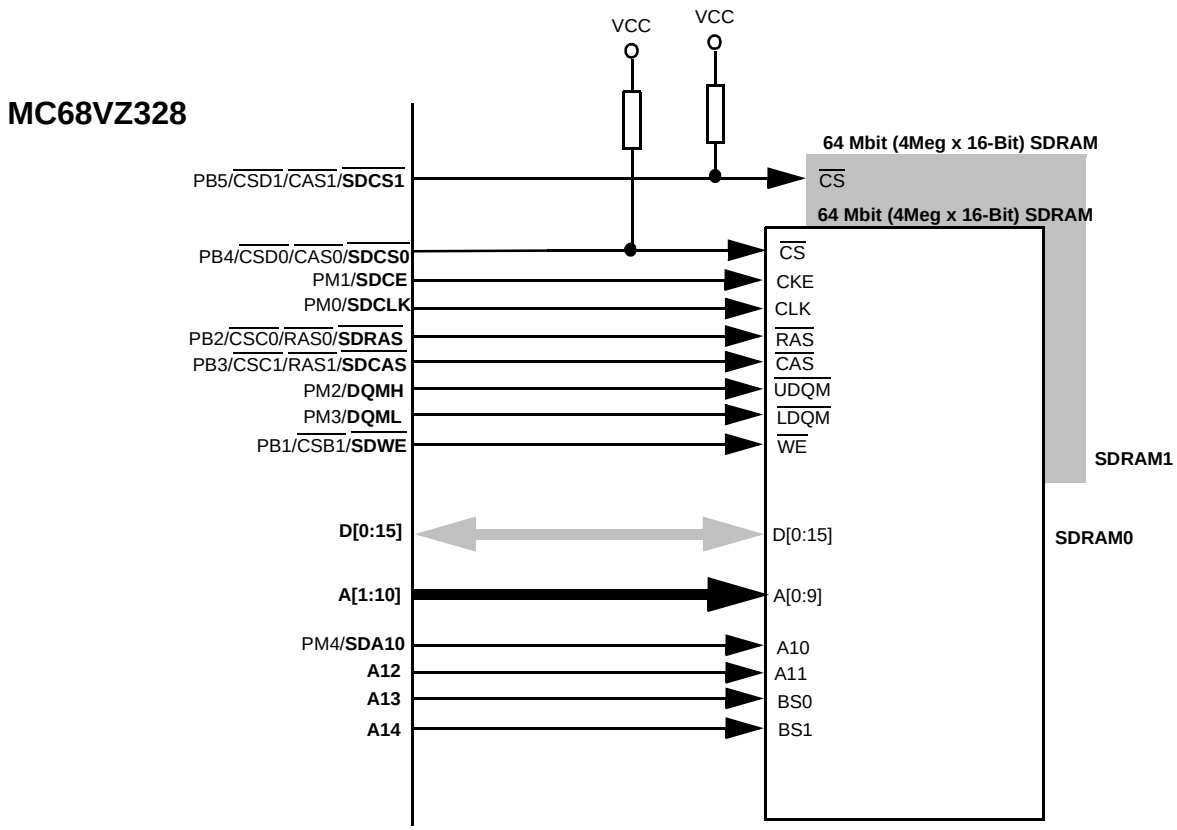

Figure 1. Pin Connection from VZ to SDRAM

The above configuration was taken from the DragonBall VZ Application Development System which provides for two (2) 64 Mbit SDRAM (4 M x 16-bit).

Each Chip-Select line can address up to 16 Mbytes of memory. Chip-select D0 can be configured to use the address space of Chip-Select D1 for a total address space of 32MByte. See section 3.1.2 for details on using 32MByte SDRAM.

2.1 Address Lines

One of the trickier steps in connecting the SDRAM are the address lines. Of particular importance is address line PM4/SDA10 which should always be connected to A10 on the SDRAM chip to ensure proper SDRAM operation.

NOTE: SDA10 & SDRAM Precharge

SDA10 can be kept high during precharge command to tell the SDRAM to indicate precharge all bank

Below are some examples of address line configuration for different sizes of SDRAM:

Table 2. Address Line Configurations (8-bit or 16-bit)

	VZ Pins			
SDRAM Pins	**16Mbit**	**64Mbit**	**128Mbit**	**256Mbit**
A[0:9]	A[1:10]	A[1:10]	A[1:10]	A[1:10]
A10	SDA10	SDA10	SDA10	SDA10
A11[1]	A12	A12	A13	A12
A12	X	X	X	A13
BS0	X	A13	A12	A15
BS1	X	A14	A15	A16

Note: X = "No Connect"
Note 1: For 16Mbit SDRAM, A11 is used for Bank Select and maybe labeled as such.

These configurations apply to both 8-bit and 16-bit SDRAM. The reason for this is because differences between 8-bit and 16-bit addressing can be configured by setting the DRAM Memory Configuration Register (DRAMMC). See section 7.3 of the VZ User Manual for details on configuring this register. For details on address bus signals, see section 2.4 of the VZ User Manual.

2.2 Data Lines

One item worth noting for the data bus is that 8-bit SDRAMs should connect their data signals to D[15:8]. For details on data bus signals, see section 2.5 of the VZ User Manual.

2.3 Interface Lines

For details on SDRAM interface signals, see section 2.15 of the VZ User Manual.

3 SDRAM Control Registers

This section will cover the relevant registers involved in SDRAM operations. The following registers have an effect on SDRAM operation:

Table 3. SDRAM Registers

Name	Address	Description	VZ Manual
CSGBD	0x(FF)FFF106	Chip-Select Group D Base Address	Table 6-5
CSD	0x(FF)FFF116	Chip-Select Register D	Table 6-10
CSCTRL1	0x(FF)FFF10A	Chip-Select Control Register 1	Table 6-12
CSCTRL2	0x(FF)FFF10C	Chip-Select Control Register 2	Table 6-13
DRAMMC	0x(FF)FFFC00	DRAM Memory Configuration Reg.	Table 7-6
DRAMC	0x(FF)FFFC02	DRAM Control Register	Table 7-7
SDCTRL	0x(FF)FFFC04	SDRAM Control Register	Table 7-8
SDPWDN	0x(FF)FFFC06	SDRAM Power-down Register	Table 7-10

For certain registers, only a number of fields are of relevance to SDRAM operation. The table below lists the relevant fields for each register.

Table 4. SDRAM Registers Relevant Fields

Name	Description	Relevant Fields
CSD	Chip-Select Register D	COMB, DRAM, BSW, WS3-1, SIZ, EN
CSCTRL1	Chip-Select Control Register 1	DSIZ3
CSCTRL2	Chip-Select Control Register 2	ECDD, ECDT
DRAMC	DRAM Control Register	EN, RM, CLK, PGSZ, LSP, RST

3.1 Chip-Select Registers

When VZ is configured to use SDRAM, chip-select group D[1:0] are used for SDRAM chip-selects. At the same time, chip-select group C[1:0] becomes the $\overline{\text{SDCAS}}$ and $\overline{\text{SDRAS}}$ signals. During this time, all chip-select group C registers are ignored.

3.1.1 Chip-Select Group D Base Address Register (CSGBD)

This register holds the base address for SDRAM. The value in this register represents A[28:14] of the address bus. So a value of 0x0800 will put the SDRAM at 0x01000000.

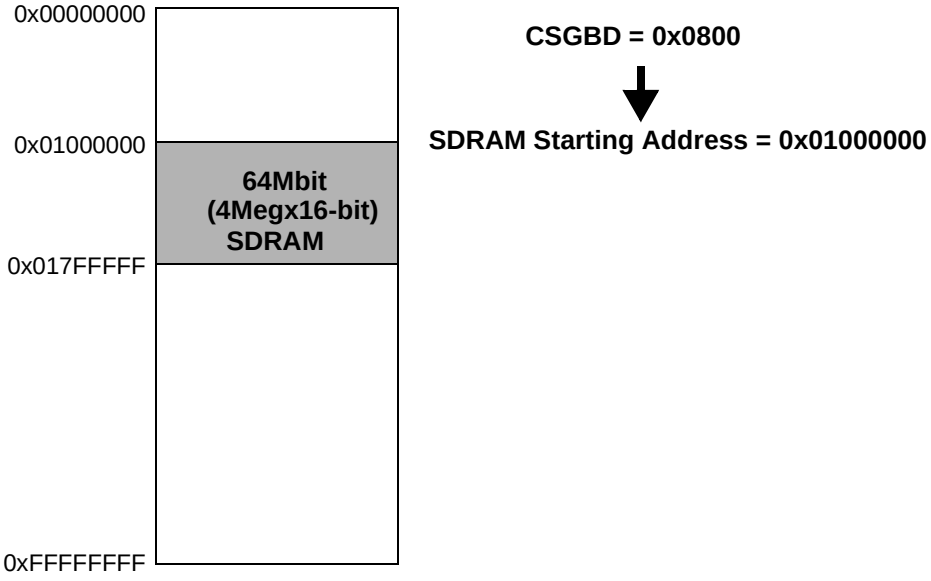

Figure 2. Chip-Select Base Address Register

3.1.2 Chip-Select Register D (CSD) & Chip-Select Control Register 1 (CSCTRL1)

The CSD register is used to determines three things:

- If chip-select group C will be used as CAS and RAS.
- The bus width of the SDRAM.
- The size for each SDRAM chip-select.
  (With the influence of CSCTRL1)

By default, CSD register is set to use CAS[1:0] and RAS[1:0] function muxed to PB[5:4] and PB[3:2] respectively. This is determined by the **DRAM bit (bit9)** of the CSD register.

The second is the **BSW bit (bit7)** which is ’0’ for 8-bit SDRAM and ’1’ for 16-bit SDRAM.

For the size of each SDRAM chip-select, the **SIZ field (bits[3:1])** is employed. The values represented by these bits need to be combined with the DSIZ3 bit of the CSCTRL1 register to configure the chip-select size.

Table 5. SDRAM Chip-Select Size

DSIZ3[1]	SIZ [3:1]			SDRAM Size
0	0	0	0	32K
0	0	0	1	64K
0	0	1	0	128K
0	0	1	1	256K
0	1	0	0	512K
0	1	0	1	1MB
0	1	1	0	2MB
0	1	1	1	4MB

Table 5. SDRAM Chip-Select Size

DSIZ3[1]	SIZ [3:1]			SDRAM Size
1	0	0	0	8MB
1	0	0	1	16MB[2]
1) This bit resides in the CSCTRL1 register. 2) Use this setting for 32MB SDRAM as well.				

NOTE: 32 MB SDRAM Chip-Select Size

For 32MB SDRAM, the chip-select size is first set to 16 MB, and then the COMB bit (bit10) of the CSD register is set to '1'. The COMB bit effectively combines the memory space of CSD1 to that of CSD0 allowing CSD0 to address a full 32MB.

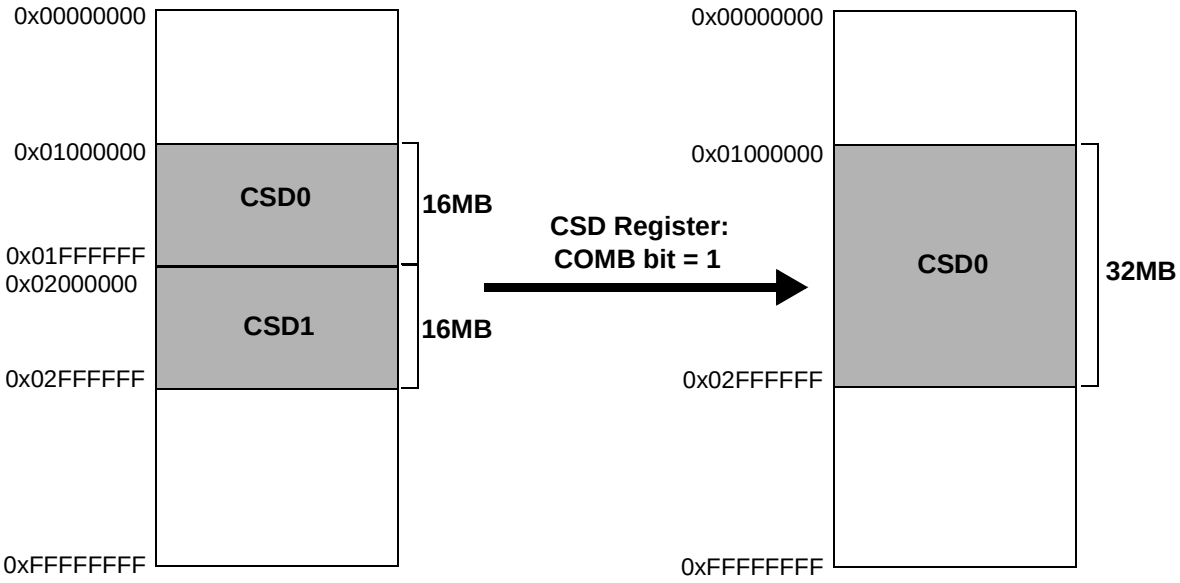

Figure 3. Combining CSD0 and CSD1 for 32MB SDRAM

The **EN bit** of the CSD register should be set to one to enable this chip-select. Also, the WS3-1 bits can be used to introduce a number of wait states if required.

3.1.3 Chip-Select Control Register 2 (CSCTRL2)

The DragonBall VZ chip-select module incorporates an Early Cycle Detect (ECD) feature for dynamic memory. In a normal CS (without ECD) scenario, the CS signal is preceeded by an internal Address Strob (ASB) signal from the 68K core. The ECD feature works off the fact that the ASB is itself preceeded by an "early" ASB signal from the 68K core. By using the "early" ASB signal to derive the CS signal, both read and write cycles to SDRAM can be shortened by one clock cycle.

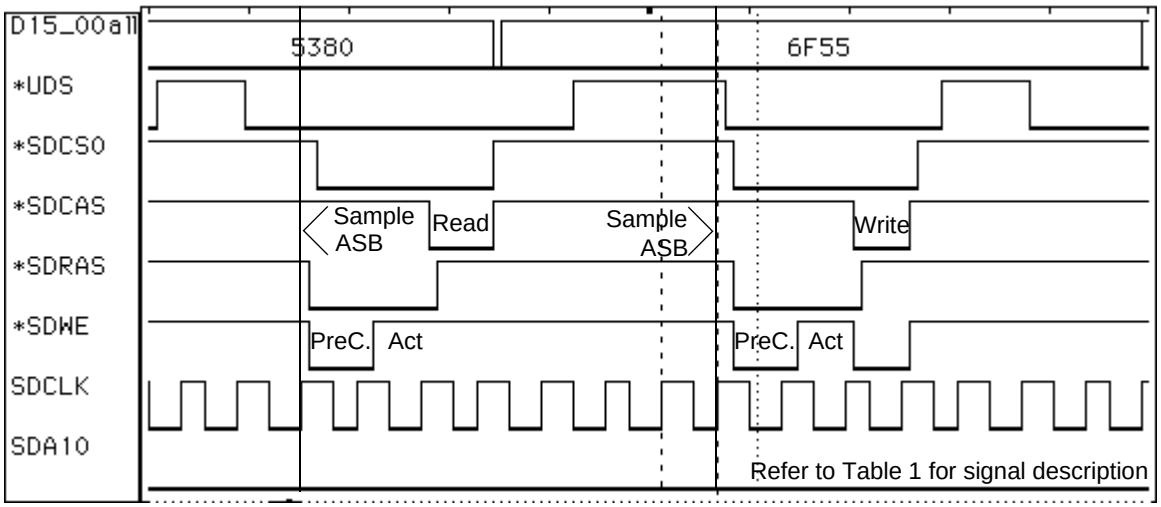

Figure 4. Normal SDRAM Read/Write

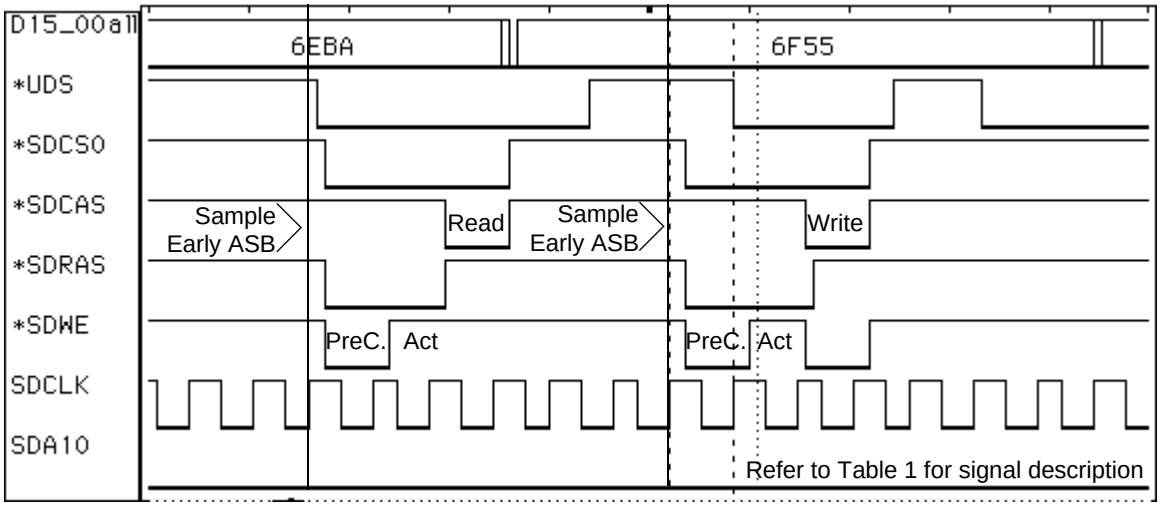

Figure 5. SDRAM Read/Write with ECD

Using the PK3/UDS signal as a reference in Figure 4 and Figure 5, setting the ECDD bit can improve SDRAM operation during CPU access to the SDRAM by asserting SDCSx early. LCDC DMA access is not affected by the ECD feature since the CPU is not involved during the access.

For more information on ECD settings, see section 6.3.6 in the VZ User Manual

3.2 DRAM Controller Registers

The DragonBall VZ DRAM Controller is designed to support SDRAM up to 32MB. Four registers handle the configuration and operation of SDRAM.

3.2.1 DRAM Memory Configuration Register (DRAMMC)

The DRAM Controller uses address multiplexing to support different types of SDRAM. For recommendations on how address lines should be configured with the SDRAM, follow tables 7-1 through 7-5 in the DragonBall VZ User Manual.

This register also controls the refresh cycle timing, see section 7.2.3 in the VZ user manual for details. For typical applications, the default value for the REF bits will suffice.

3.2.2 DRAM Control Register (DRAMC)

The DRAMC contains the following features that are relevant to SDRAM operations:

- Master DRAM Controller enable
- Page size of SDRAM
- SDRAM Refresh mode
- Light Sleep option
- Reset Burst Refresh option

Of these features, the first two options require attention before the SDRAM is initialized.

After the DRAM controller is enabled through the **EN bit (bit 15)** of the DRAMC, the page size of the SDRAM should be set in the **PGSZ field (bits 9-8)**. The page size of a particular SDRAM can be found by the number of column addresses for each bank. The amount of memory space covered by the column addresses is the page size. For 8-bit SDRAM, the number should be divide by two before applying to the PGSZ field.

Example:

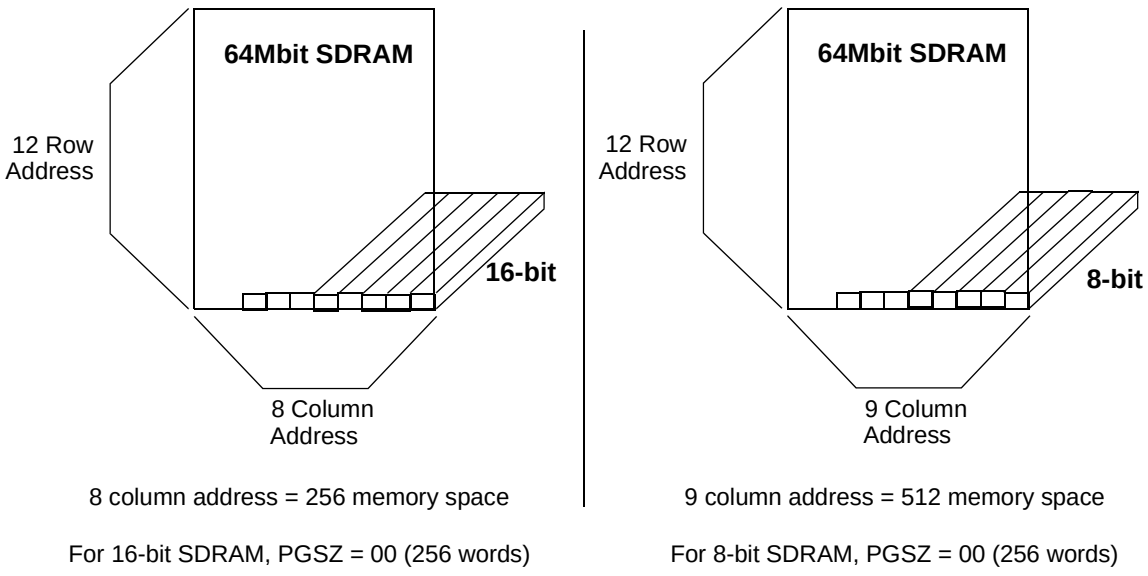

Figure 6. Calculating Page Size

The **RM bit** controls the SDRAM refresh mode between Auto-Refresh and Self-Refresh mode. See section 7.3.2 in the VZ user manual for details on other options.

3.2.3 SDRAM Control Register (SDCTRL)

SDRAM control register provides features specific to SDRAM operation. This section will run through those features in detail.

The first register bit is the **SDEN bit (bit 15)** which needs to be set in order for SDRAM to be used. This bit should be set before the EN bit in the DRAMC to ensure SDRAM support once the controller is enabled.

Along with the SDEN bit, a few other settings have to be checked as well. This includes the CAS Latency or **CL bit** and the Bank Address Line settings (BNKADDH & BNKADDL).

The CAS Latency of a SDRAM should always be set in the SDRAM's mode register before using the SDRAM. The DragonBall VZ support CAS latency of 2 or 1 cycle.

NOTE: SDRAM CAS Latency

Although most SDRAM does not specify support for CAS latency below 2 clock counts. Testing shows that a number of those SDRAM have no problems while running in CAS latency 1 mode.

The number of SDRAM banks is defined using the BNKADDH and BNKADDL bits. This "bank" refers to the internal arrangement of the SDRAM chip.

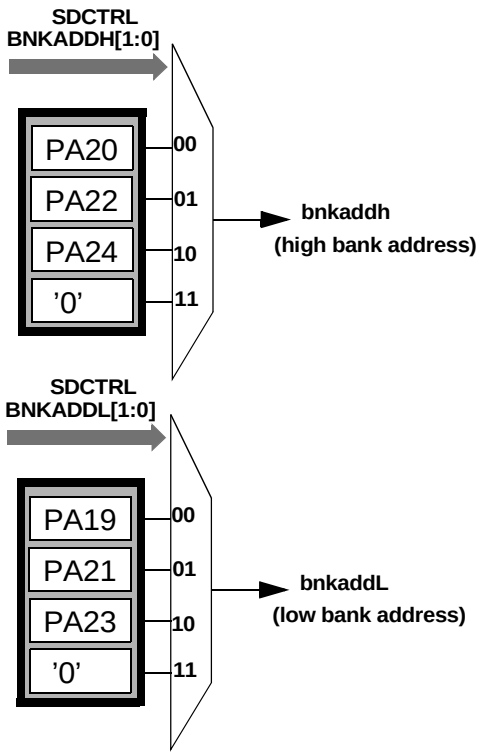

Figure 7. BNKADDH and BNKADDL Model

Figure 7 depicts the internal structure of the logic. Two multiplexors will derive the bank address based on the setting of the SDCTRL register bits BNKADDH[1:0] and BNKADDL[1:0]. The controller supports 4 banks, therefore there are two lines of bank address. However, bnkaddH and bnkaddL signals are used by internal bank register and page hit detection logic to track whether the current access is on the same page of previous access in the same bank. Each individual bank has its own logic.

For 2 bank device, only one mux from the pair is used. The other mux is programmed to '11' (outputs '0'). Therefore only two possible bank registers are present apparently. For 4 bank device, both two mux are used to form 2 line bank address (bnkaddH and bnkaddL) therefore all four bank registers are used. Users may want to treat multibank device as a one bank device. In this case the user should program both BNKADDH and BNKADDL to '11' (output '0'). The logic will see only one bank register apparently. Table 7-9 in the VZ user manual provides information on how to set these bits.

NOTE: VZ Silicon Bug in SDRAM Bank Handling

It is currently recommended that all BNKADDH/L bits be set to '1' for SDRAM to appear as one single bank. This is due to a silicon bug documented in the VZ design. Multibank setting under CAS latency 2 can cause the DragonBall VZ to stop responding to commands if the LCD and the CPU are accessing seperate banks.The erratum is listed in errata document which can be downloaded from www.motorola.com/dragonball

Continuous Page Mode or **CPM bit** in the SDCTRL register can also be enabled at this time. The CPM feature can accelerate SDRAM read/write cycles by eliminating unneeded precharge cycles. With CPM enabled, access to a page for the first time will generate a page-miss flag which will send a precharge then a read/write command. Subsequent access to the page will generate a page-hit flag which is followed immediately by the read/write command. Setting CPM is also another method in circumventing the multibank issue mentioned above.

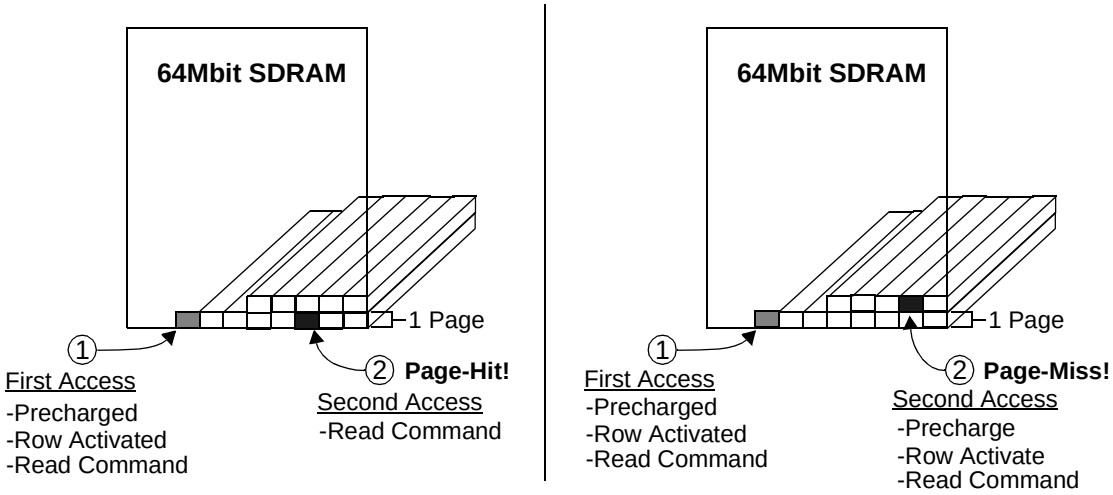

Figure 8. Continuous Page Mode

Before the SDRAM is fully operational, its has to go through an initialization sequence.

- Initiate an all bank precharge with the IP bit

  IP = 1, RE = 0, MR = 0

- Start SDRAM refresh cycles using the RE bit in the SDCTRL register

  IP = 0, RE = 1, MR = 0

- Set mode register of the SDRAM with the MR bit

  IP = 0, RE = 1, MR = 1

  The **MR bit** passes the CAS latency setting to the mode register of the SDRAM. The load mode register command programs the SDRAM to Cas latency 1 or 2 depending on the CL bit. The CL bit should be set to the proper latency period prior to setting the MR bit.

All the steps above has to be done in that order followed by a number of no-ops to allow the SDRAM to initialize properly.

See the next section for example code on SDRAM initialization.

3.2.4 SDRAM Power-down Register (SDPWDN)

The SDPWDN register controls how the SDRAM enters power-down mode. The power-down mode can reduce SDRAM power consumption by negating the SDCE signal when SDRAM is not being accessed. During power-down mode, refresh cycles continue to be issued to the SDRAM by the DRAM controller.

3.2.4.1 Active Power-down Mode

When the APEN bit is set, the SDCE will be negated after every access to the SDRAM.

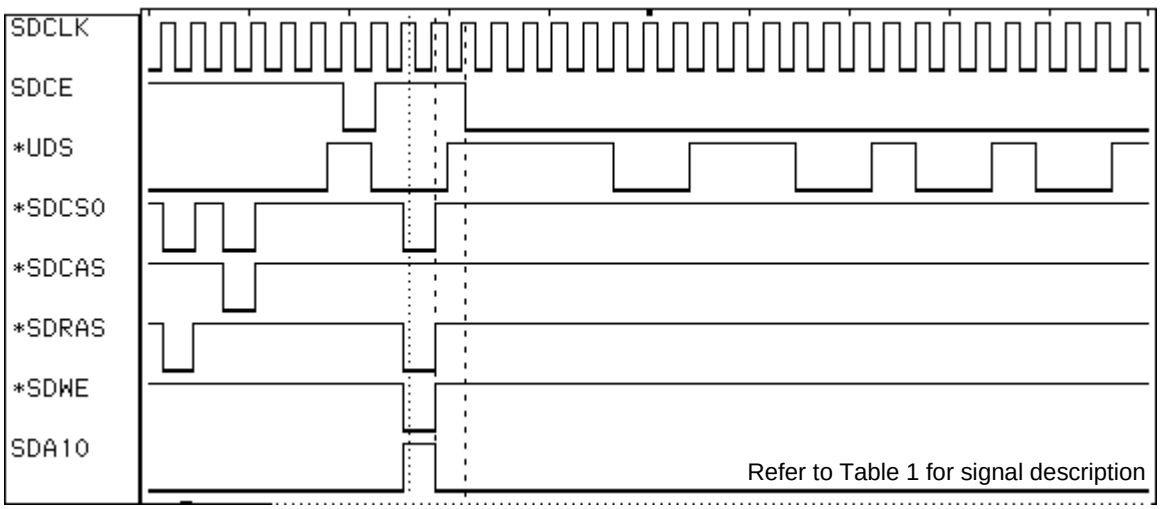

Figure 9. Active Power-down Mode

3.2.4.2 Precharge Power-down Mode

When the PDEN bit is set, the SDCE signal will negate when the SDRAM has been precharged and the PDTOUT time-out condition has been meet.

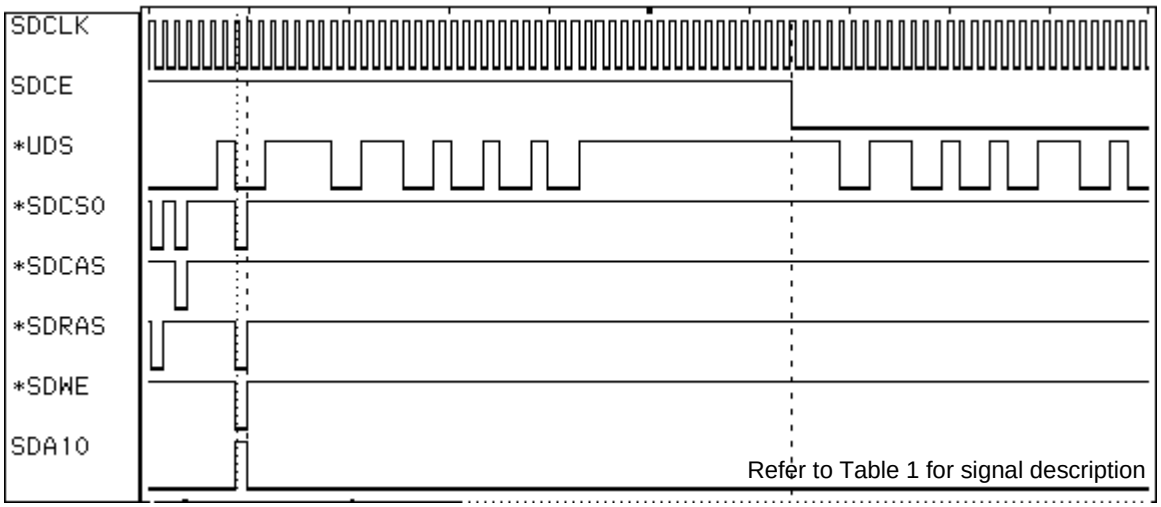

Figure 10. Precharge Power-down Mode

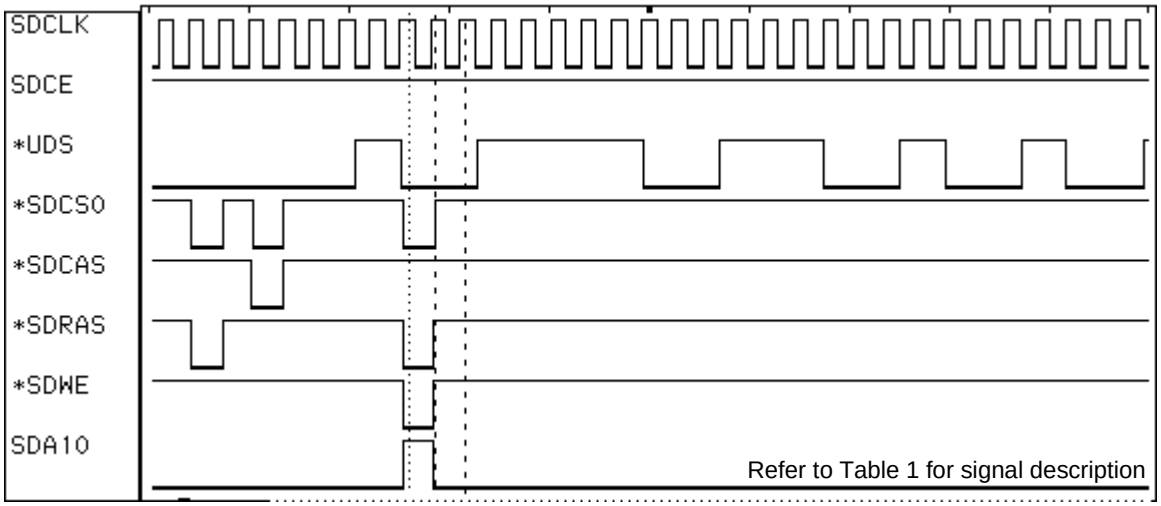

Figure 11. Power-down Mode Disabled

4 SDRAM Initialization Sequences

The following are the initialization sequences use by the VZ ADS board:

```
    ;*************************************
    ; SDRAM 64M-bit, Single Band, Latency 2
    ;*************************************
    move.w  #$0000,GRPBASED      ; Set SDRAM base address to 0x0
    move.w  #$0281,CSD
    move.w  #$0040,CSCR          ; Chip Sel Control Reg

    move.w  #$0000,DRAMC         ; Disable DRAM Controller
    move.w  #$C03F,SDCTRL                    ; Set CPM, CL1, Single Bank
    move.w  #$4020,DRAMMC                    ; Multiplexing for 64Mb SDRAM
    move.w  #$8000,DRAMC                     ; Enable DRAM Controller

    clr.w   d0                               ; Delay period for SDRAM
delay
    addi.w  #1,d0
    cmp.w   #$FFFF,d0
    bne     delay

    move.w  #$C83F,SDCTRL        ; Issue precharge comm
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    move.w  #$D03F,SDCTRL        ; Enable refresh
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    move.w  #$D43F,SDCTRL        ; Issue mode command
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
```

5 SDRAM Power Control Features

The DRAM controller can initiate two kinds of power control features:

- Self-refresh mode.
- Power-down mode.

SDRAM self-refresh mode is controlled by the RE bit in the DRAMC register. By setting the RE bit to ’1’, the DRAM controller will issue a self-refresh mode command.

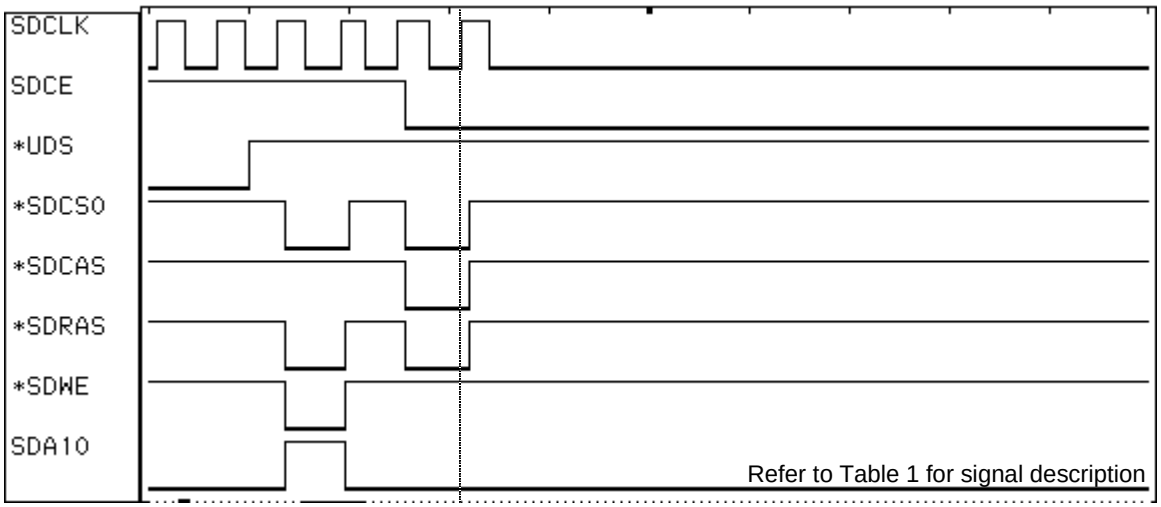

Figure 12. Self-refresh Event

The SDRAM draws the minimal amount of power when in self-refresh mode. The DRAM controller can also be disabled after the SDRAM enters self-refresh mode.

Power-down modes allows the SDRAM to be supended when not in use. It differs from self-refresh mode in that it does not require a wakeup period when access occurs. See section 3.2.4 of this document for details on power down modes.

6 SDRAM Logic Analyser Captures

The following logic analyser captures show SDRAM read and write cycles generated by a VZ ADS.

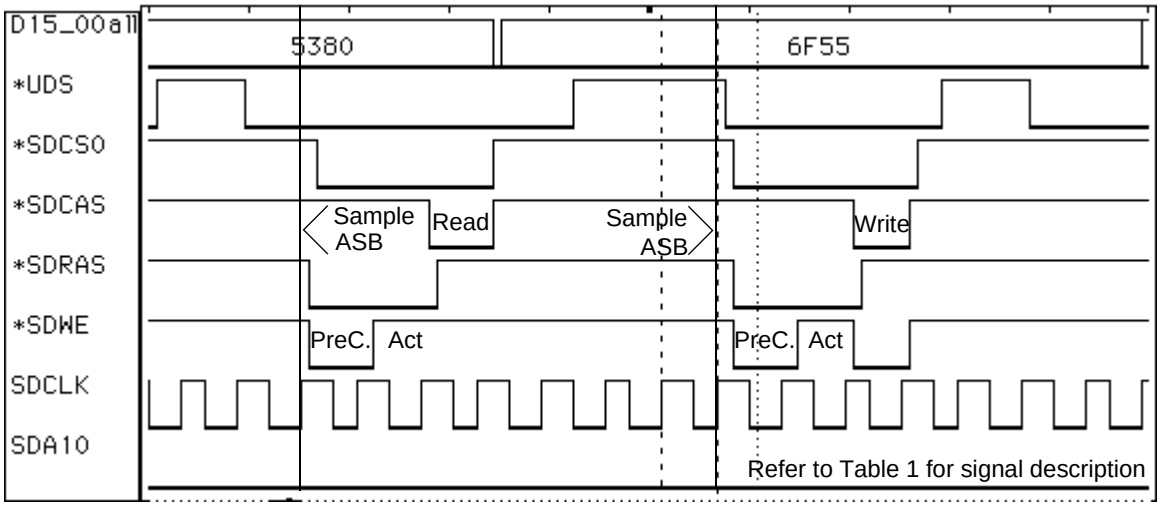

Figure 13. SDRAM Read/Write; CAS Latency = 1; Page-Miss Condition

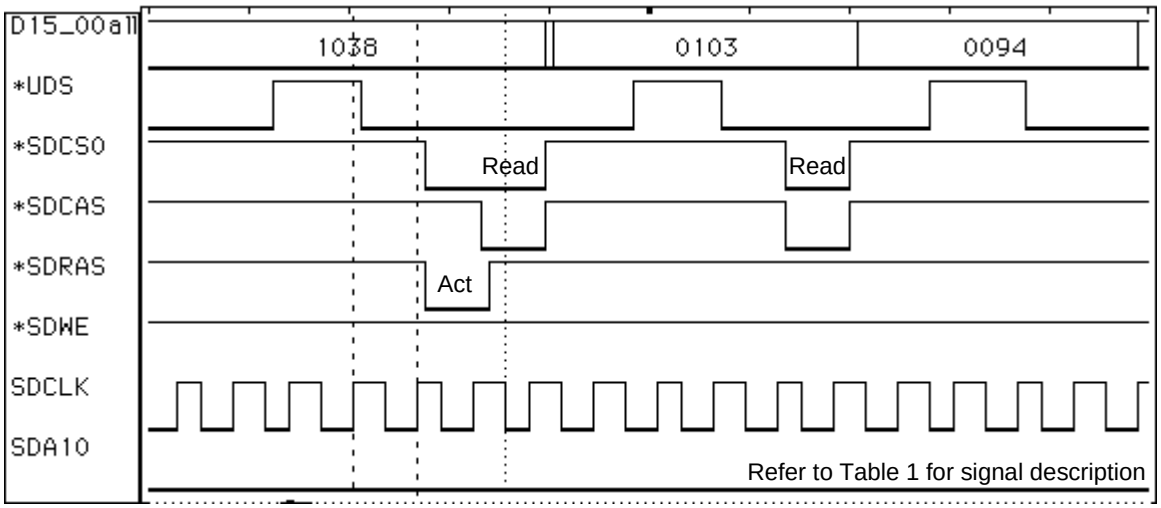

Figure 14. SDRAM Read; CAS Latency = 1; Page-Hit Condition

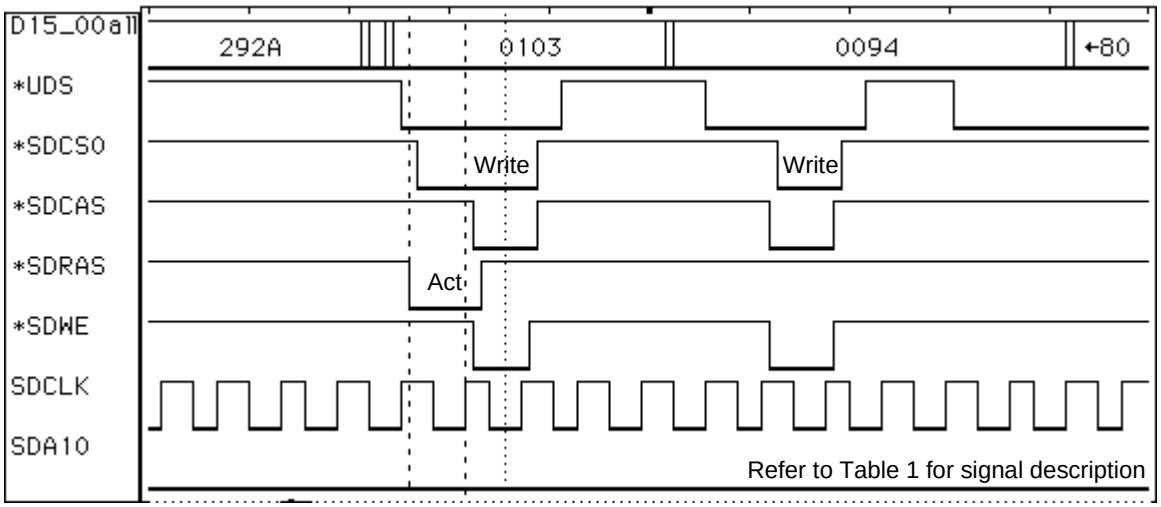

Figure 15. SDRAM Write; CAS Latency = 1; Page-Hit Condition

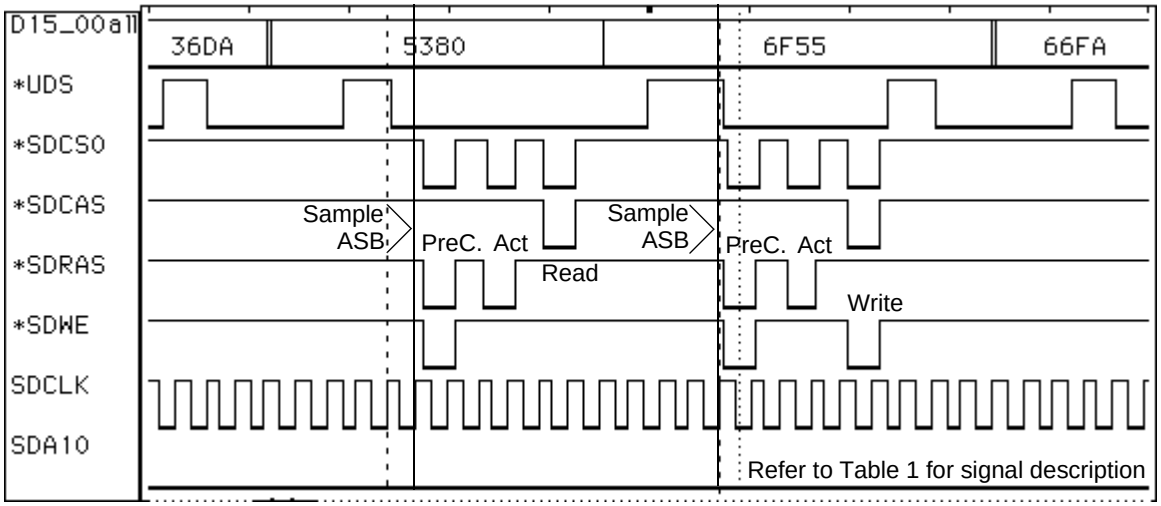

Figure 16. SDRAM Read/Write; CAS Latency = 2; Page-Miss Condition

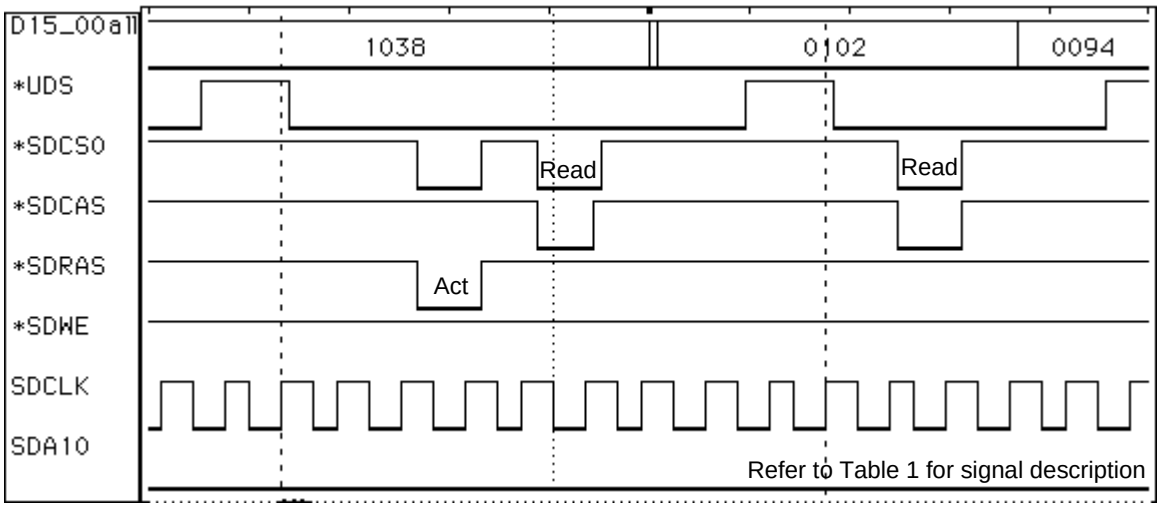

Figure 17. SDRAM Read; CAS Latency = 2; Page-Hit Condition

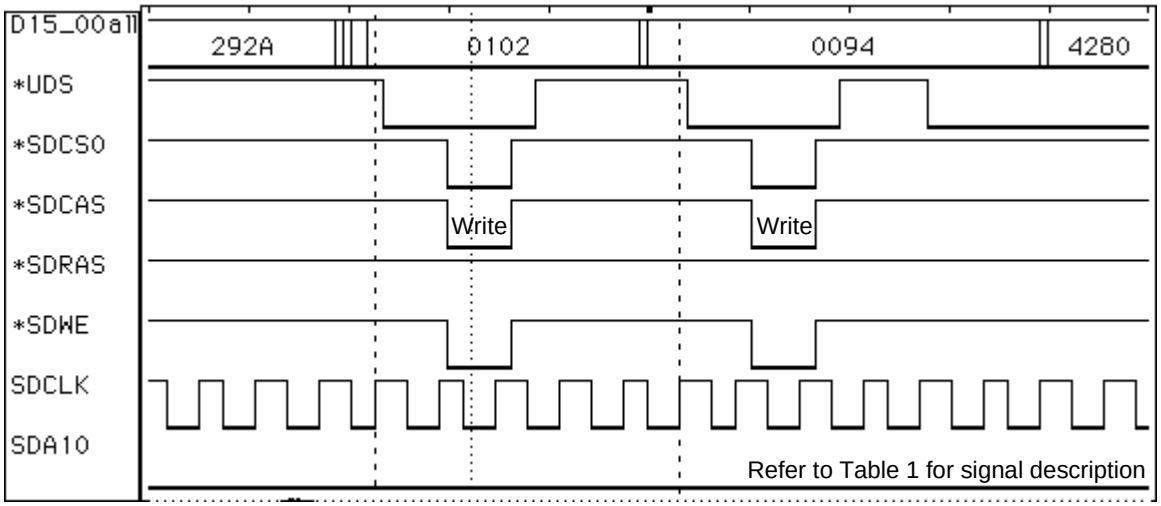

Figure 18. SDRAM Write; CAS Latency = 2; Page-Hit Condition

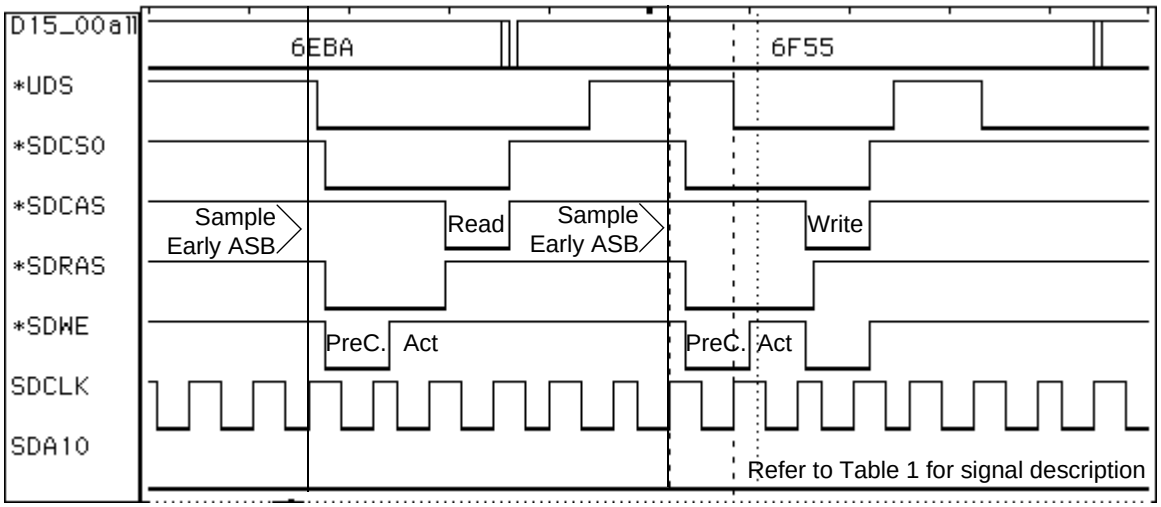

Figure 19. SDRAM Read/Write; CAS Latency = 1; Page-Miss Condition; with ECD

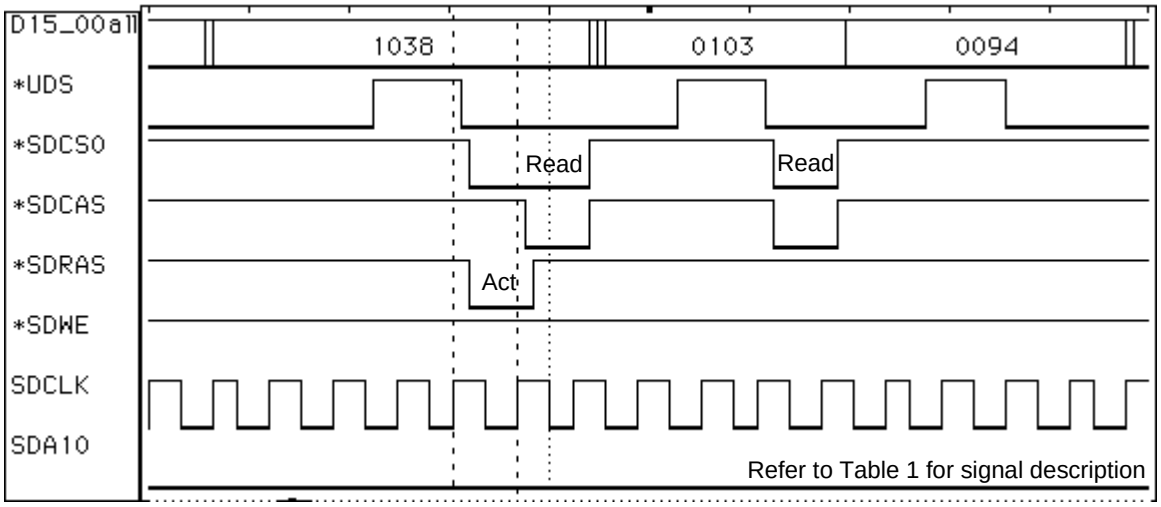

Figure 20. SDRAM Read; CAS Latency = 1; Page-Hit Condition; with ECD

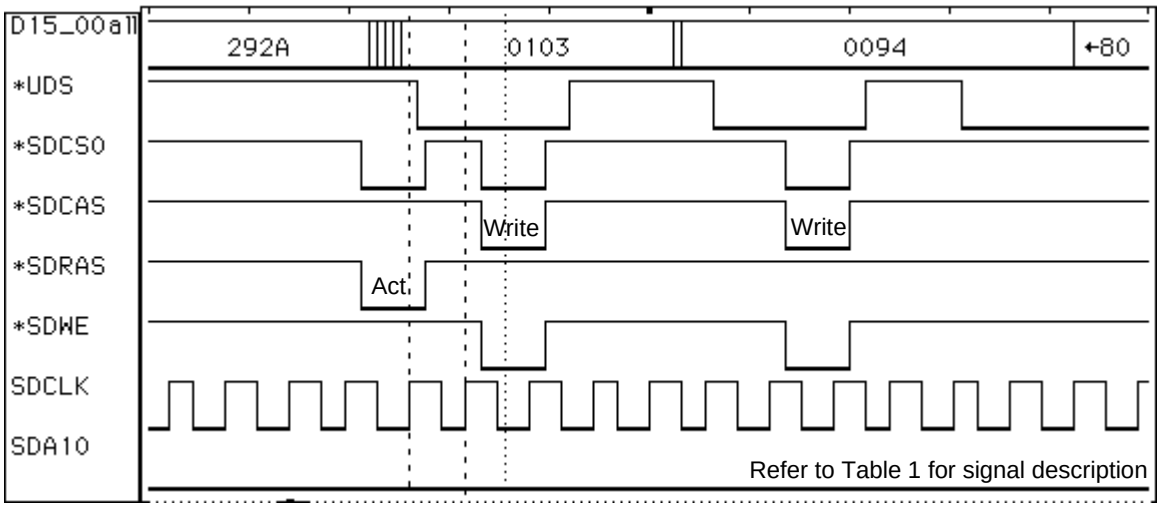

Figure 21. SDRAM Write; CAS Latency = 1; Page-Hit Condition; with ECD

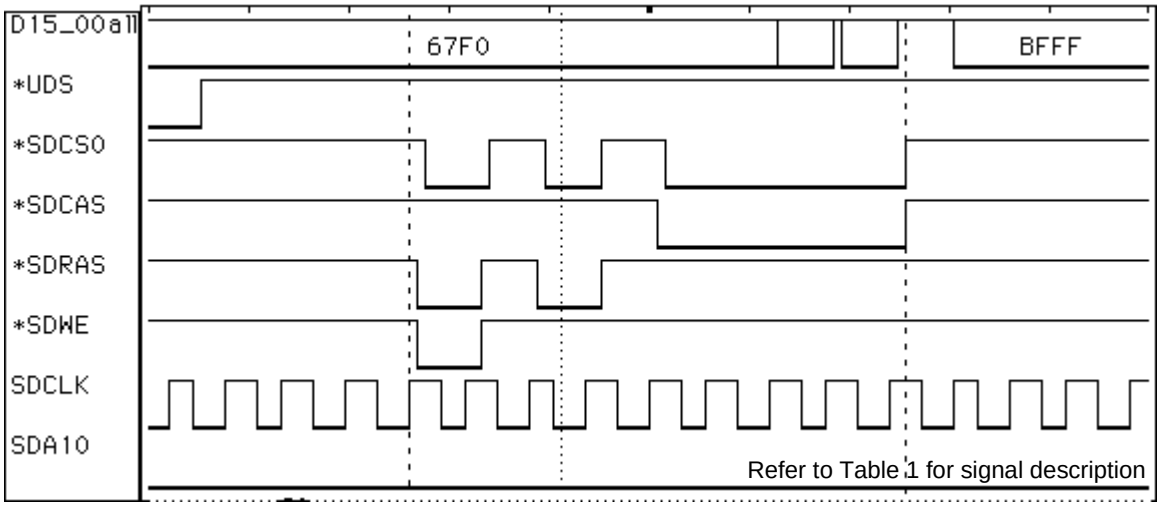

Figure 22. LCD DMA Read; CAS Latency = 2; Burst Length = 4