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APPLICATION NOTE

EMC Guidelines for MPC500-Based Automotive Powertrain Systems

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1 Introduction

An increasingly important consideration in the design of automotive powertrain systems is electromagnetic compatibility (EMC). EMC consists of four sub-groups: radiated emissions, conducted emissions, radiated susceptibility, and conducted susceptibility. This application note focuses on guidelines for reducing radiated emissions from MPC500-based powertrain systems. These guidelines are not a complete set of all known EMC techniques, instead they are some specific recommendations for MPC500-based systems. This application note should be used in conjunction with other more general sources of EMC guidelines, many such sources are suggested in the **4 References** section.

The reduction of radiated emissions from automotive modules is an effort to reduce the likelihood of electromagnetically interfering with the automobile's other electronic systems, such as its radio receiver. Electromagnetic interference (EMI) involves the coupling of a noise source to a victim receiver. For this discussion, the noise source is the automotive module and within the module the MCU can be a source of electrical noise.

Since the MPC500 family is packaged in a 27-mm x 27-mm PBGA and the maximum frequency of interest is 1000 MHz, the MCU itself is not a very efficient radiator. However, the MCU can couple noise onto the printed circuit board (PCB), and the PCB and attached cabling can be efficient radiators. Therefore, the goal is to reduce the amount of noise the MCU generates and to reduce the coupling of the MCU's noise onto the PCB.

In general, experiments have shown that the MPC500 family have four primary sources of noise: CLKOUT, ENGCLK, core power supply, and the ADDR/DATA bus pins. Of these, CLKOUT is usually the cause of any given EMI system problem and/or EMI module specification failure. Similarly, ENGCLK can be a significant noise source if driven at system frequency. However, ENGCLK is normally used at a much lower frequency and is therefore less of a concern. Simultaneous switching noise (SSN) due to the switching of digital logic on MCUs causes noise on the core power supply (V_{DDI} for MPC55x and V_{DD} for MPC56x). ADDR/DATA bus noise mainly increases the broad band emissions and is therefore less of an issue than the other three noise sources discussed.

2 Software Guidelines

2.1 CLKOUT

The CLKOUT driver has software selectable drive strengths which are controlled by the COM bits in the SCCR register. CLKOUT is enabled after reset and the default value of drive strength is determined by the BDRV bit in the hard reset configuration word. Many board applications are configured such that

this results in the selection of full drive strength. Full drive strength for CLKOUT assumes a load of 90 pF and is intended for test purposes only. Unless full drive strength is required for timing considerations, it is recommended that a reduced drive strength be used. The MPC55x and the MPC56x have half-drive strength options. The MPC56x also has a quarter-drive strength option with additional control bit, CQDS, in the SCCR register.

NOTE

The MPC555 K62N (Revision M) or later has a one-third instead of one-half drive strength option.

Additionally, the COM bits can be configured to disable the CLKOUT driver. If CLKOUT is not needed in the system, it is strongly recommended that it be disabled. The maximum output frequency for CLKOUT is equal to the system operating frequency.

2.2 ENGCLK

The ENGCLK driver has software selectable drive strength and frequency options. The frequency of ENGCLK is determined by the ENGDIV bits in the SCCR register. The default is set for a maximum division which results in the lowest possible frequency. The ENGCLK should be configured for the lowest possible frequency that is required by the system. Additionally, the ENGCLK driver has selectable output drive strength options which are controlled by the EECLK bits in the SCCR register. For the MPC55x, the ENGCLK can be enabled at full-drive strength (90 pF), enabled at half-drive strength (45 pF), or disabled.

NOTE

The MPC555 K62N (Revision M) or later has drive strengths of 50 pF (full) and 25 pF (half).

It is recommended that ENGCLK be disabled or used in half-drive strength mode. For the MPC56x, the ENGCLK driver can be enabled with a 2.6-V output, enabled with a 5.0-V output, or disabled. The MPC56x does not have a half-drive strength option. It is recommended that the ENGCLK be disabled or used with the 5.0-V output; the 5.0-V output drives slower than the 2.6-V output.

2.3 System Frequency

System frequency is determined by the crystal frequency and the PLL multiplication factor. The PLL multiplication factor is set by the MF bits in the PLPRCR register. In general, the lowest possible frequency should be used. However, since radiated emissions will occur at the fundamental frequency and harmonics of the fundamental some care should be taken to avoid having the second harmonic fall in the radio broadcast range.

2.4 Power Management

Many individual modules have the option to be disabled. Disabling a module reduces SSN currents because the transistors in the disabled module are no longer clocked. All modules which are not used should be disabled by setting the STOP bit in each module's MCR register.

2.5 Bus Configuration

Bus pins have two drive strength options: full-drive and reduced-drive. These options are controlled by the COM bits in the SCCR register. Reduced drive should be used unless full-drive strength is required to meet system timing specifications. Additionally, if the bus is not needed, the MCU should be configured for single-chip mode operation (i.e., address and data buses not used). Single-chip mode is configured by the hard reset configuration word. The bus also has a show cycle feature which when enabled drives the contents of the internal bus onto the external bus pins. Show cycles should be disabled.

2.6 Slew Rate

Slew rate is controlled by the SLRC[0:3] bits in the PDMCR register. Slow slew rate should be used unless insufficient for system timing requirements. The default configuration is for slow slew rate. Slow slew rate has a longer rise time than normal slew rate. Therefore, slow slew rate results in smaller amplitude harmonics.

2.7 Static Pin Configuration

Unused output pins should be driven low instead of driven high. In general, there is less voltage fluctuation on ground than on power. Therefore, conducted emissions out of the pin will be lower when the pin is driven low than when the pin is driven high.

3 Hardware Guidelines

3.1 Standard Decoupling

3.1.1 Capacitor Selection

All of the MPC500 family MCUs are mixed voltage parts. Each has some 5-V power supply balls for the high-voltage I/O pins. In addition, each has another supply voltage for its core operation and low-voltage I/O pins. These voltages are 3.3 V for the MPC55x and 2.6 V for the MPC56x. Since the low-voltage supply is noisier than the high-voltage supply, emphasis should be placed on decoupling the low-voltage supply.

Three different capacitor values should be used to decouple both the high-voltage and the low-voltage supplies. A good starting place is to use values of 10 µF, 0.1 µF, and 10 nF. Approximately 30 10-nF caps are needed for the high frequency decoupling. Only a few 0.1 µF and 10 µF caps are required for the low frequency decoupling. Low Equivalent Series Resistance (ESR) and low Equivalent Series Inductance (ESL) capacitors should be used. **Table 1** provides some example components available from AVX. Similar capacitors are also available from other manufacturers such as Murata, KEMET, and Vishay.

Table 1 AVX Capacitor Examples

Capacitor Value	AVX Part Number
10 nF	03065C103KAT1W
0.1 µF	06125C104KAT1W
10 µF	TAJE106K050R

3.1.2 Capacitor Layout

There should be at least one 0.1 µF and one 10 µF capacitor for each of the low-voltage and the high-voltage supplies. These capacitors should be placed next to the power entry point of the board and connected directly to the power and ground planes with multiple vias.

Of the 30 10 nF capacitors, eight should be used to decouple the high-voltage (5-V) power plane in the vicinity of the MCU. Place the capacitors as close as possible to the MCU surrounding the MCU uniformly. Each of the capacitors should connect to the 5-V power plane and the ground plane using multiple vias. The vias should be located in the solder pads for the capacitors (see **Figure 1**). Connect the high-voltage power balls (V_{DDH}) directly to the high-voltage power plane.

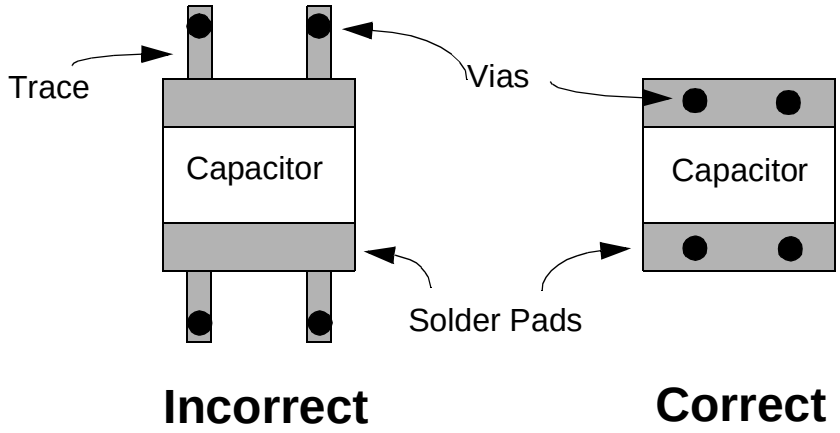

Figure 1 Vias for Decoupling Capacitors

The remaining 22 10 nF capacitors are required for decoupling the low-voltage (3.3-V or 2.6-V) MCU supply. The MPC55x and the MPC56x have different ball maps. Also, some application boards allow for component placements on both sides of the PCB whereas some only allow for component placement on one side of the PCB. Therefore, four different strategies for the layout of the remaining 22 capacitors are presented in order to accommodate all of the possibilities.

1. MPC55x Double-Sided Component Placement Application

The basic strategy in this situation is to connect all the low-voltage power supply balls (V_{DDI} and N_{VDDL}) to the low-voltage power supply plane. The plane is then decoupled by connecting the capacitors directly to the power and ground planes. Start by placing as many capacitors directly opposite the MCU (on the other side of the PCB) between the vias from the center and outer rows of balls (see **Figure 2**). Place any remaining capacitors on the opposite side of the PCB as the MCU just outside the vias from the outer row of balls uniformly distributed around the MCU. All V_{SS} balls should be connected directly to the ground plane.

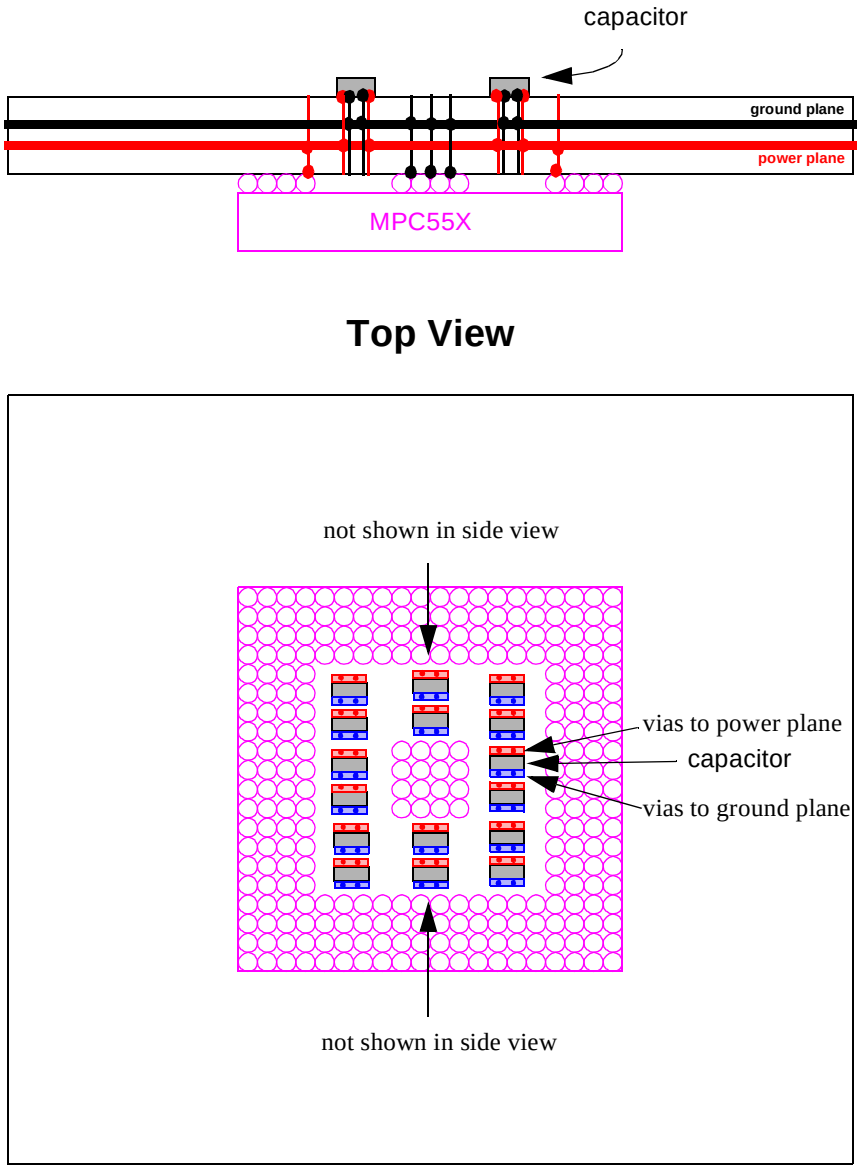

Figure 2 MPC55x Double-Sided Component Placement Application

2. MPC55x Single-Sided Component Placement Application

In this situation, the capacitors should be placed as close as possible, and on the same side of the PCB, as the MCU. Connect the MCU's low-voltage power supply balls (V_{DDI} and N_{VDDL}) to an isolated power island on the power plane layer. Then connect the power island to the caps with multiple vias. Finally, connect the capacitors to the main power plane with a small trace and multiple vias. The MCU's ground balls should be connected directly to the ground plane (i.e., there should not be an isolated ground is-

land). The negative side of the capacitors should be connected with multiple vias to the ground plane (see **Figure 3**).

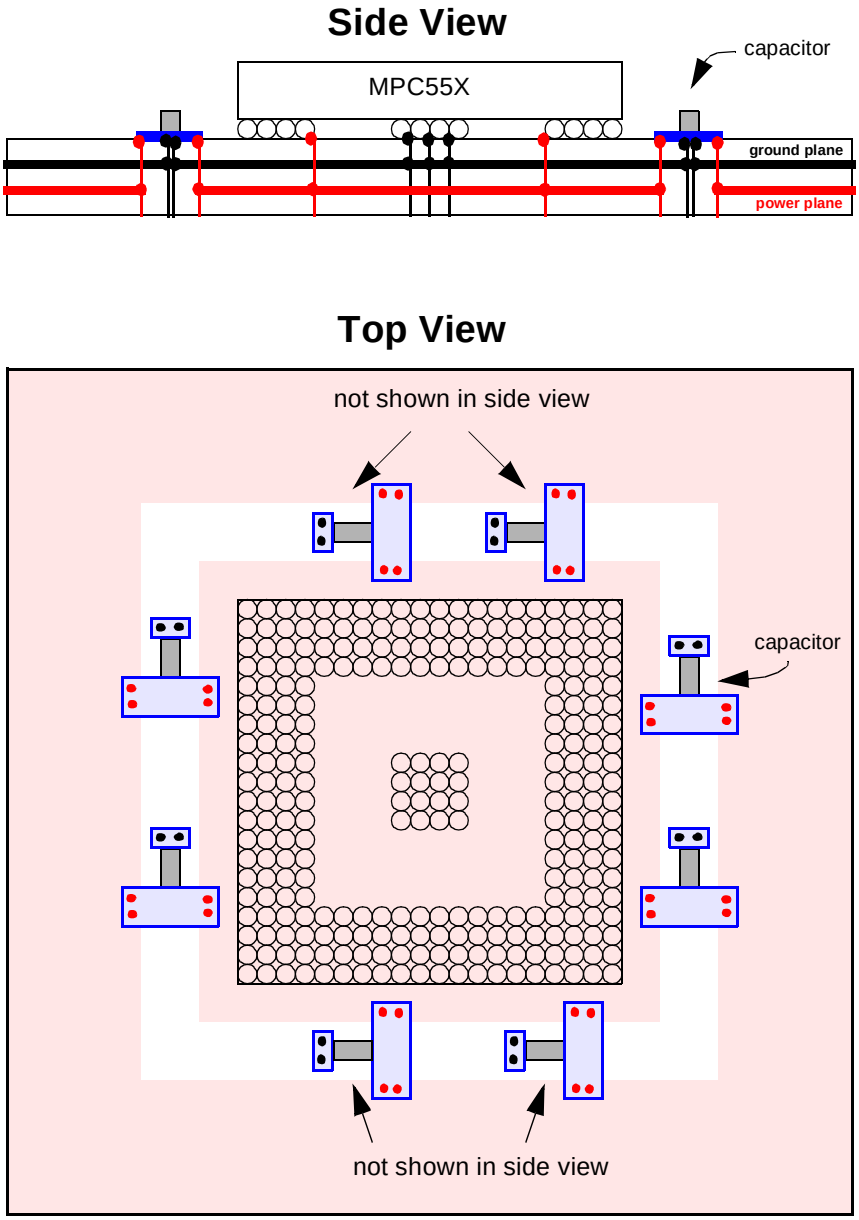

Figure 3 MPC55x Single-Sided Component Placement Application

3. MPC56x Double-Sided Component Placement Application

With this approach, the V_{DD} balls are treated differently than the N_{VDDL} and Q_{VDDL} balls.

There are a total of 16 V_{DD} balls, four in each corner of the BGA package. Each of the four corners of four balls should be decoupled with two 10 nF capacitors for a total of eight 10 nF capacitors. The VDD

balls should NOT be tied directly to the power plane, but instead should route up to the top layer and over to the 10 nF capacitors. After routing to the 10 nF capacitors, a connection to the power plane should be made with vias for each of the four areas.

The N_{VDDL} and Q_{VDDL} balls should be connected directly to the power plane and 10 10 nF capacitors are used to decouple the power plane in their immediate vicinity. See **Figure 4** for additional details.

The remaining 10 nF capacitors should be connected to the power and ground planes and the capacitors should be located as close as possible to the MCU. Also, the remaining capacitors should be evenly distributed around the MCU.

All V_{SS} balls should be tied directly to the ground plane.

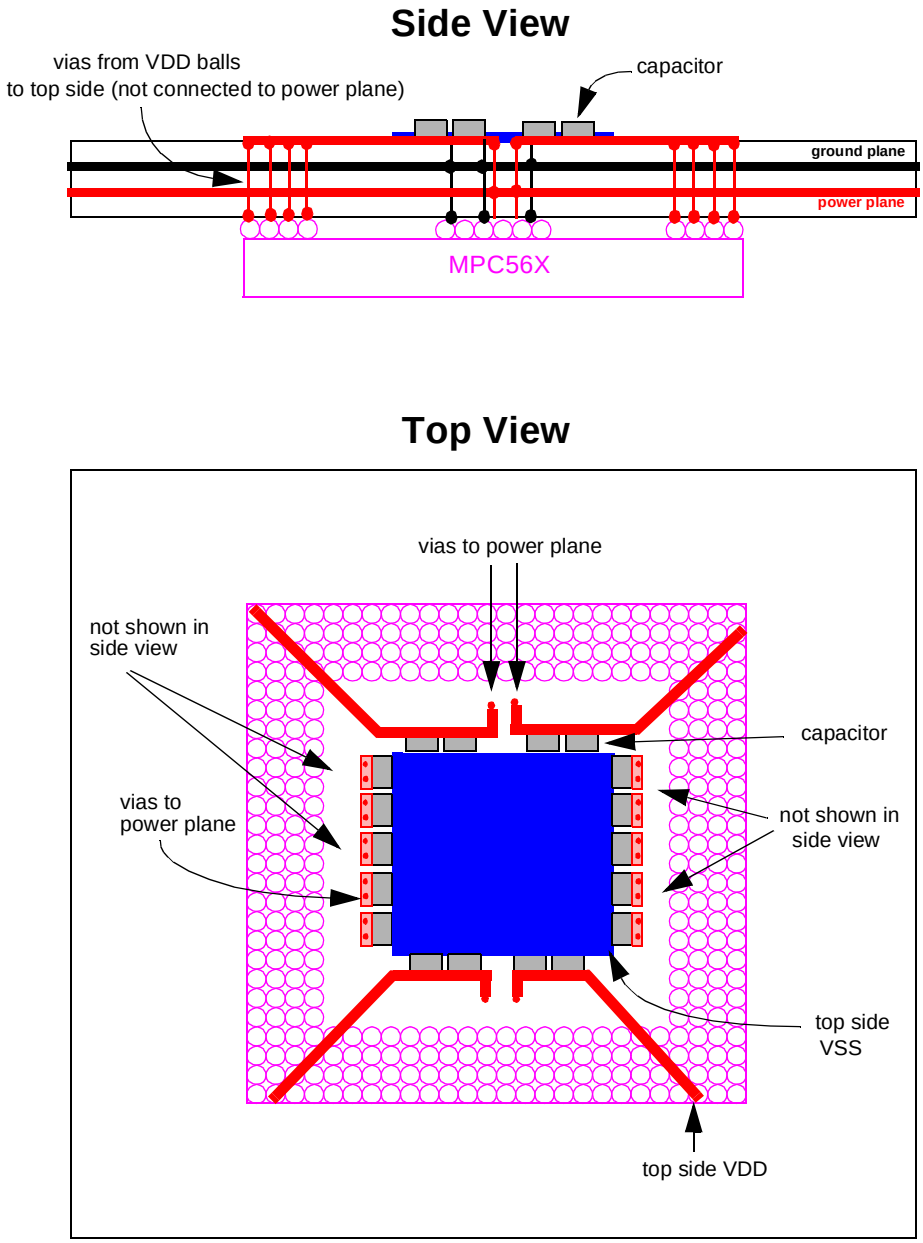

Figure 4 MPC56x Double-Sided Component Placement Application Example

4. MPC56x Single-Sided Component Placement Application

In this case, the V_{DD} balls are treated differently than the N_{VDDL} and Q_{VDDL} balls.

Each of the four V_{DD} balls in the corners of the BGA have corresponding V_{SS} balls. Place two 10 nF capacitors directly next to the MCU in the corners by the V_{DD} and V_{SS} balls. Have wide topside strips

which connect all four V_{DD} balls to the two capacitors. There should also be wide topside strips connecting all four V_{SS} balls to the capacitors. After the V_{DD} and V_{SS} strips pass the capacitors, they should be connected to the power and ground planes with vias. In addition, all V_{SS} balls should be connected directly to the ground plane.

The N_{VDDL} and Q_{VDDL} balls should be connected directly to the power plane. Place ten 10 nF capacitors as close as possible to the MCU (avoiding the corners where the V_{DD} capacitors are located). The capacitors should be connected directly to the power and ground planes with many vias. See **Figure 5** for additional details.

Place any remaining 10 nF capacitors as close to the MCU as possible and distribute around the MCU in a uniform manner. Connect these capacitors directly to the power and ground planes.

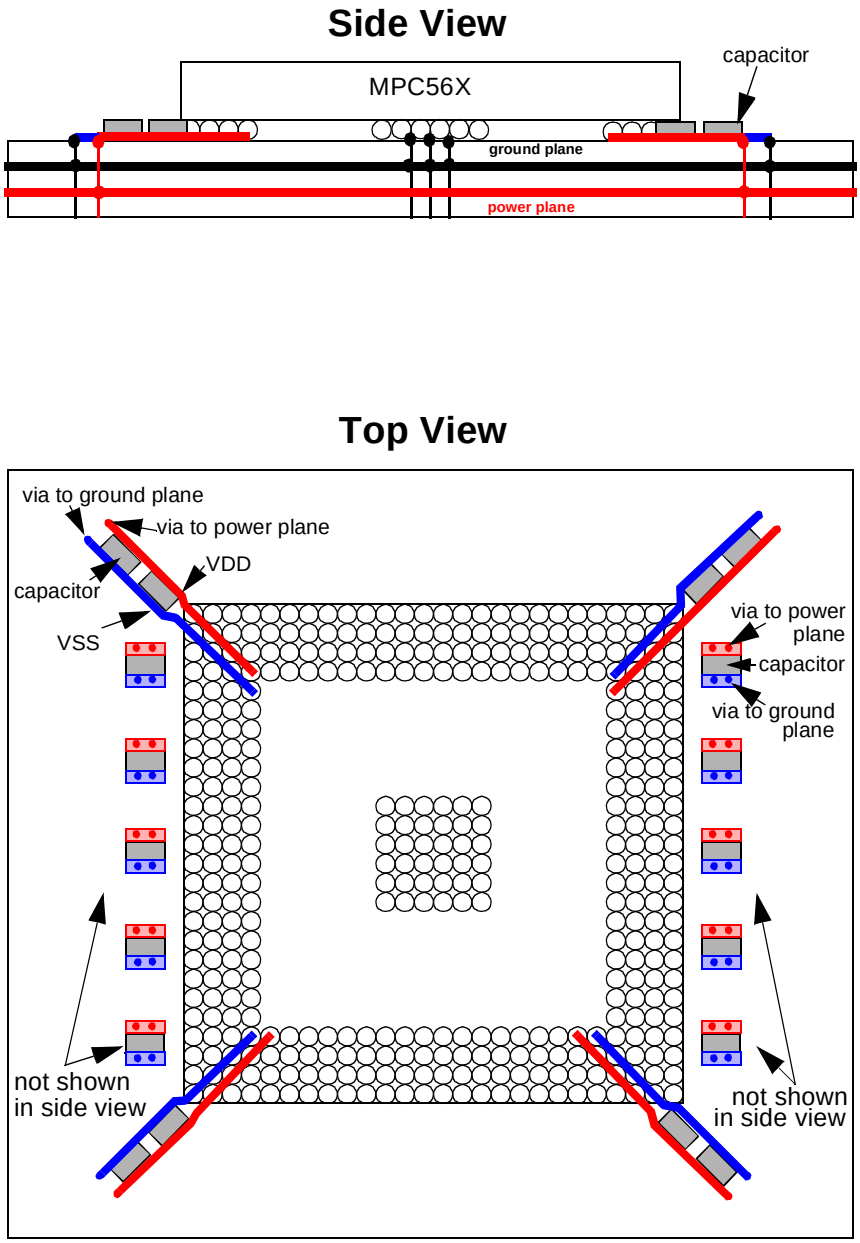

Figure 5 MPC56x Single-Sided Component Placement Application

3.2 Standard Grounding

Most MCU based systems will partition different classes of circuits with isolated grounds. The isolated grounds are then connected together at a single point, as shown in **Figure 6**. The different classes of circuits include digital, analog, high-current switching circuitry, I/O, and the main power supply.

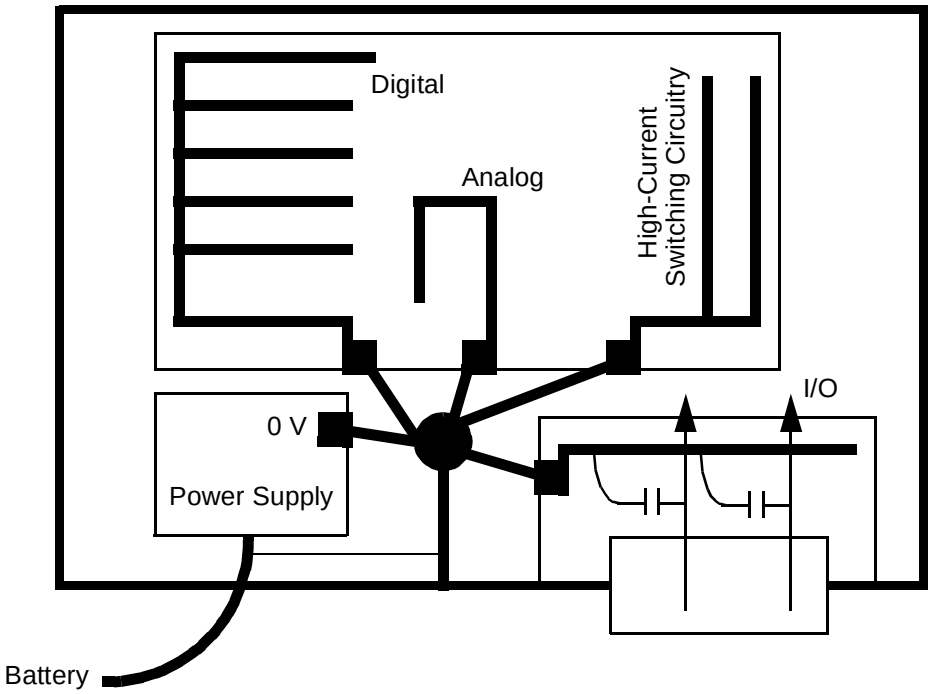

Figure 6 Typical MCU Application Grounding Example

3.3 Micro-Island Approach to Decoupling and Grounding

The micro-island approach to decoupling and grounding is the premier solution for high-speed digital noise isolation, and as such it tends to cost more to implement than standard decoupling and grounding. The micro-island technique aggressively seeks to isolate all high-speed digital noise to a micro-island instead of allowing it to propagate throughout the entire system. All high-speed digital components such as the MCU, crystal, and memory are grouped together in an isolated island and a moat surrounds the entire island. There are isolated power and ground islands which are also surrounded by moats; the ground island extends out further than the power island. Power entry to the micro-island is filtered using a three terminal EMI chip capacitor or a Π-filter consisting of a low-Q inductor or ferrite bead in combination with some capacitors. The micro-island is decoupled with 22 of the 0306-style 10 nF decoupling capacitors which are evenly distributed throughout the micro-island area. Any signal line leaving the micro-island area is filtered using resistors or ferrites. **Figure 7** contains additional details.

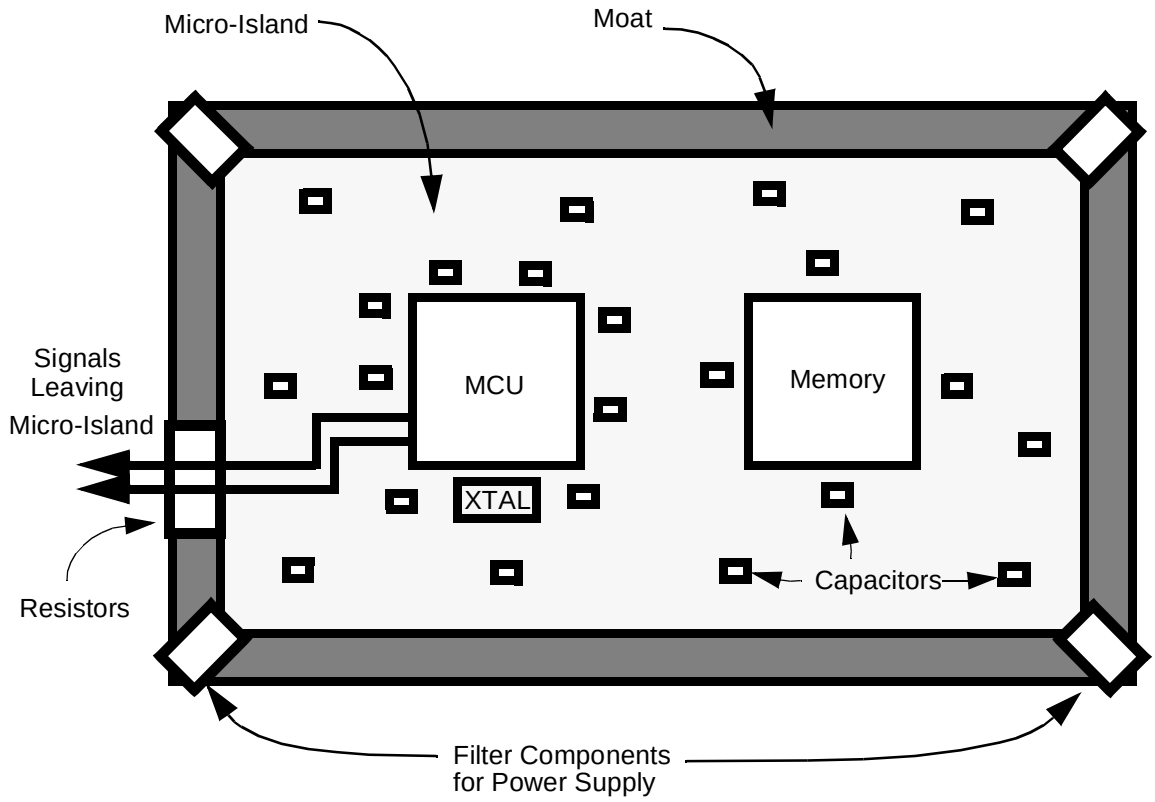

Figure 7 Typical Micro-Island Approach to Decoupling and Grounding

3.4 Signal Routing and Terminations

High-speed signals should be isolated as much as possible by using spacing and shielding of the signal traces. High-speed signals should also be routed with minimal lengths. Some high-speed signals such as CLKOUT and ENGCLK may require a termination resistor to avoid ringing and to help slow down the edge rate. The optimum value for the termination resistor will depend on the specific application, but starting with a value of 30 Ω is reasonable. The termination resistors should be located as close as possible to the MCU. Typically, the bus pins do not require termination resistors because the memory chip is placed within a few inches of the MCU and therefore the one-way propagation delay is less than one-fourth the signal rise time.

3.5 Layer Stack-Up and Vias

Most MPC500 family applications will require the use of a multi-layer board; four layer boards are the most common. For multi-layer boards, dedicated power and ground planes should be used. An example of a good four-layer stack-up is shown in **Figure 8**.

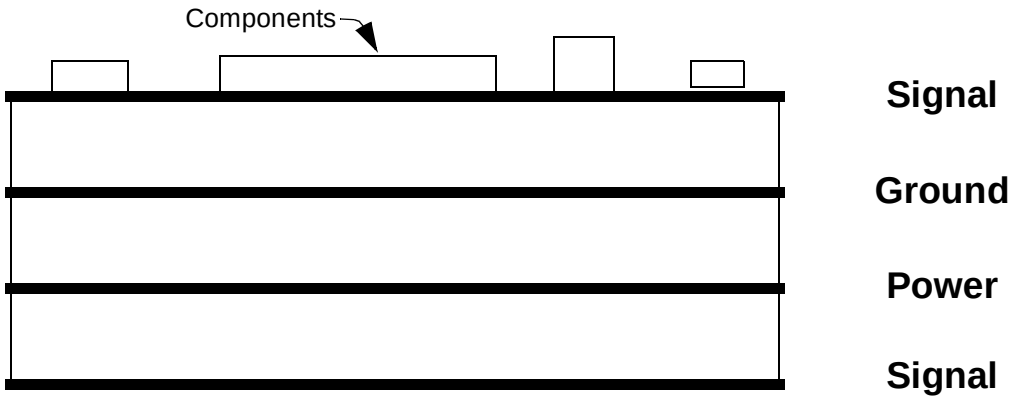

Figure 8 Layer Stack-Up Example

The use of many vias for power and ground connections is stressed throughout this document. However, care must be taken to avoid degradation of the power and ground planes by too many via anti-pads obstructing the flow of current in the plane (via anti-pads are the absence of metal surrounding a via). A general rule of thumb is to not allow three via anti-pads to merge (see **Figure 9**).

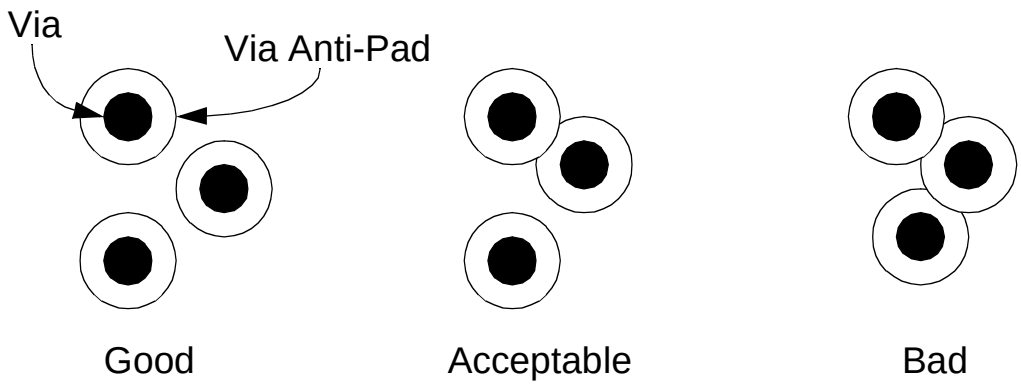

Figure 9 Via Example

3.6 Oscillator Circuit

The oscillator circuit consists of a bias resistor, the crystal, and two capacitors. The oscillator circuit provides a reference clock signal to the on-chip PLL. Use the lowest frequency crystal possible and set the multiplication factor bits to obtain the proper system operating frequency which is generated from the PLL. The oscillator circuit has currents flowing at the crystal's fundamental frequency. Also, if the oscillator is clipped, then higher order harmonics will be present as well. In order to minimize the amount of emissions generated from these currents, the oscillator circuit should be kept as compact as possible (see **Figure 10**). Also, V_{SSSYN} should be connected directly to the ground plane so that return currents can flow easily between V_{SSSYN} and the two capacitors (C_X and C_Y).

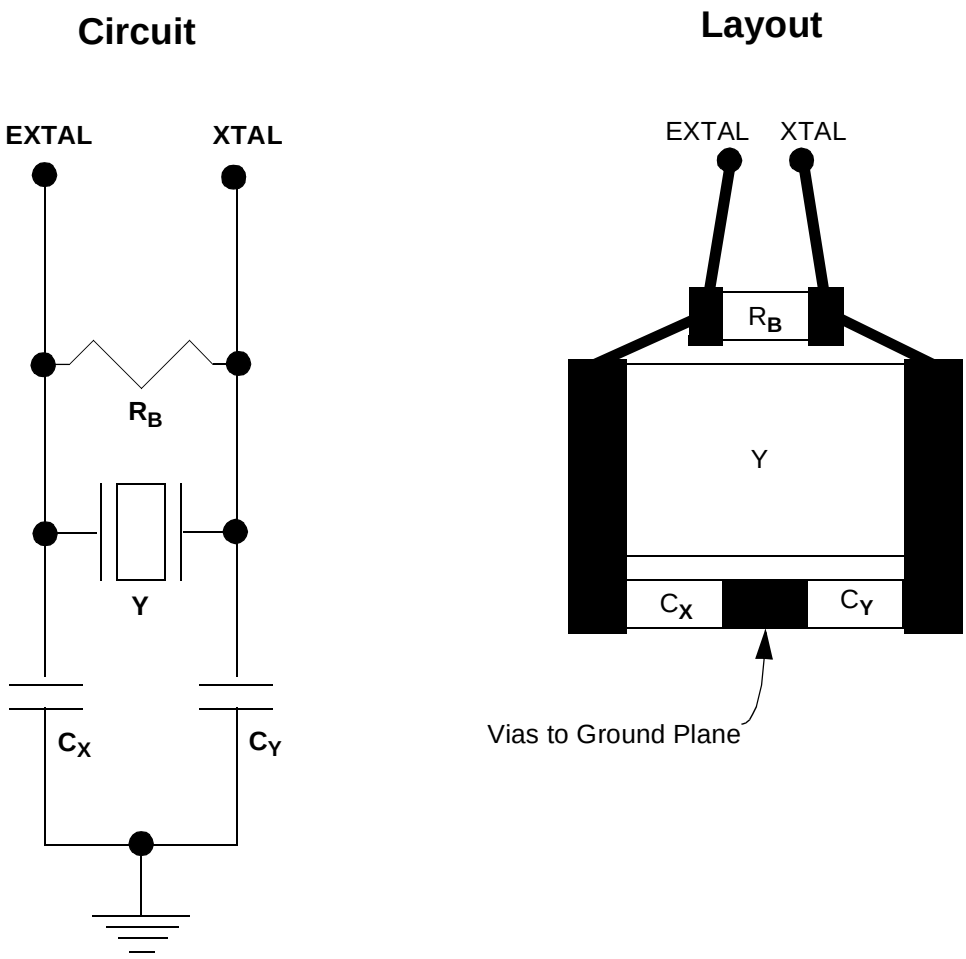

Figure 10 Oscillator CIrcuit and Layout

4 References

4.1 MPC500 Family Reference Documentation

1. ***MPC555 / MPC556 User's Manual***
2. ***MPC565 / MPC566 Reference Manual***
3. ***MPC561/MPC563 Reference Manual***

4.2 Motorola Semiconductor EMC Application Notes

1. Campbell, Dugald. ***Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers.*** Motorola Semiconductor Application Note **AN1263/D**. 1995.
2. Catherwood, Mike. ***Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers.*** Motorola Semiconductor Application Note **AN1050/D**. 1989.
3. Glenewinkel, Mark. ***System Design and Layout Techniques for Noise Reduction in MCU based Systems.*** Motorola Semiconductor Application Note **AN1259/D**. 1995.
4. Kobeissi, Imad. ***Noise Reduction Techniques for Microcontroller-Based Systems.*** Motorola Semiconductor Application Note **AN1705/D**. 1999.

4.3 General EMC References

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2. Johnson, Howard. ***High-Speed Digital Design: A Handbook of Black Magic***. Prentice Hall, 1993.
3. Ott, Henry. ***Noise Reduction Techniques in Electronic Systems***. Wiley and Sons, 1976.
4. Kimmel Gerke Associates website, http://www.emiguru.com/

4.4 Component Manufacturer Websites

1. AVX Corporation, *http://www.avxcorp.com/*
2. Murata, *http://www.murata.com/*
3. KEMET, http://www.kemet.com/
4. Vishay, *http://www.vishay.com/*

5 Revision History

Table 2 Revision History

Date	Revision	Description
July, 2001	Rev 0	Initial release
March, 2002	Rev 1	Changed all 1uF capacitors to 0.1uF.

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