

## TD351 Advanced IGBT Driver Principles of operation and application

### 1 Introduction

The TD351 is an advanced IGBT driver with integrated control and protection functions. It is a simplified version of the TD350, available in an SO8 or DIP8 package. The TD35x family (including the TD350, TD351 and TD352) provides a wide range of drivers specially adapted to drive 1200 V IGBTs with current ratings of 15 to 75 A in Econopak-like modules (see [Figure 2](#)).

The main features of the TD351 are:

- 1 A sink/0.75 A source peak output current minimum over the full temperature range (-20°C to 125°C),
- active Miller clamp function to reduce the risk of induced turn-on in high dV/dt conditions, and in most cases, without requiring a negative gate drive,
- optional 2-step turn-off sequence to reduce over-voltage in case of an over-current or a short-circuit situation; a feature that protects the IGBT and avoids RBSOA problems,
- input stage compatible with both an optocoupler and a pulse transformer.

Applications include three-phase full-bridge inverters such as in motor speed control and UPS systems (see [Figure 1](#)).

**Figure 1. TD351 in 3-phase inverter application (1200 V IGBTs)**

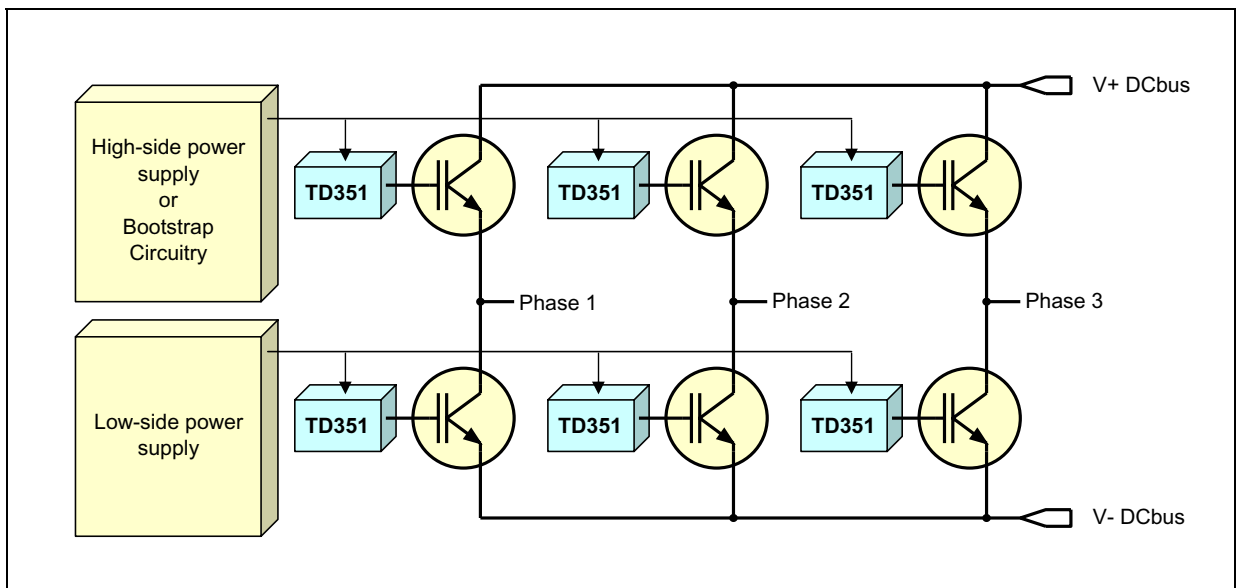
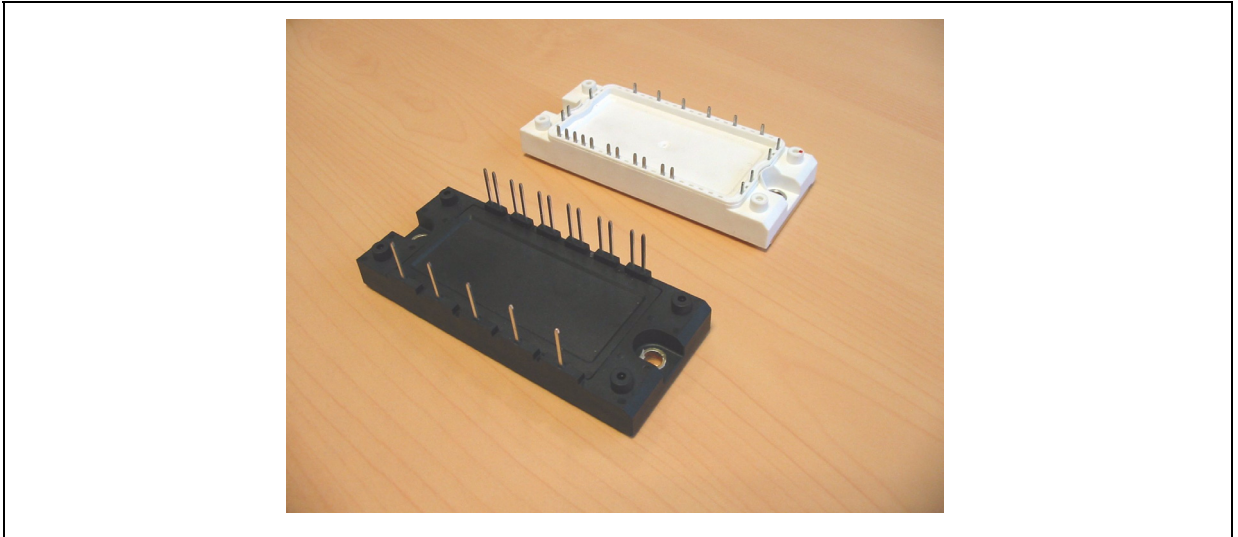


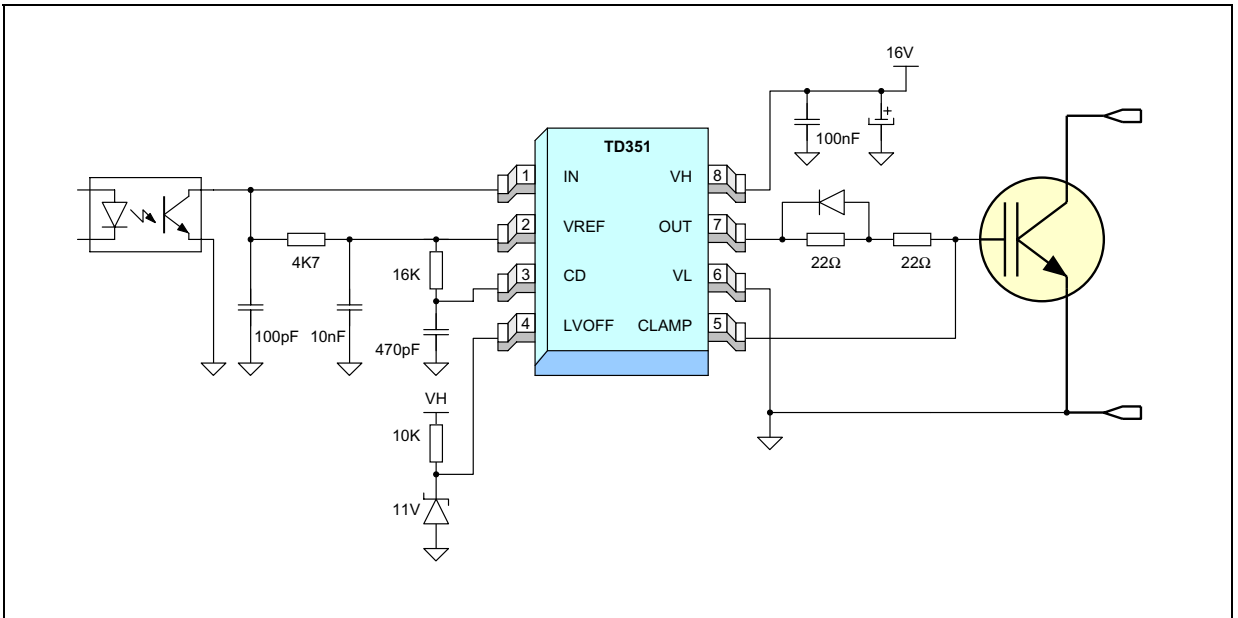
Figure 2. IGBT modules



## 2 TD351 application example

A TD351 application example is shown in *Figure 3*. In this example the device is supplied by a +16V isolated voltage source. An optocoupler is used for input signal galvanic isolation. The IGBT is driven by 44Ω for turn-on and 22Ω for turn-off thanks to the use of two gate resistors and one diode: sink and source currents can therefore be tuned independently to help and solve EMI issues. Power switch drivers are used in very noisy environment and decoupling of the supplies should be cared. In the application example the decoupling is made by a 100nF ceramic capacitor located as close as possible to the TD351 in parallel with a bigger electrolytic capacitor.

Figure 3. TD351 application example



### 3 Input stage

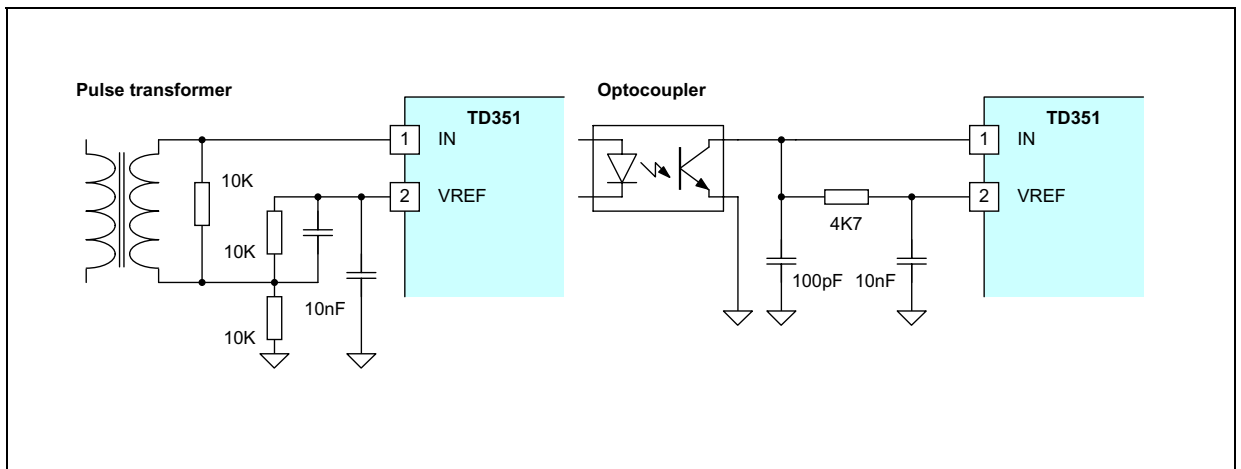
The TD351 is compatible with the use of both pulse transformers or optocouplers. The schematics shown in [Figure 4](#) can be considered as example of use with both solutions.

When using a pulse transformer, a 2.5 V reference point can be built from the 5 V VREF pin with a resistor bridge. The capacitor between the Vref and the bridge middle point provides decoupling of the 2.5 V reference, and also insures a high level on IN input at power-up, in order to start the TD351 in the OFF state.

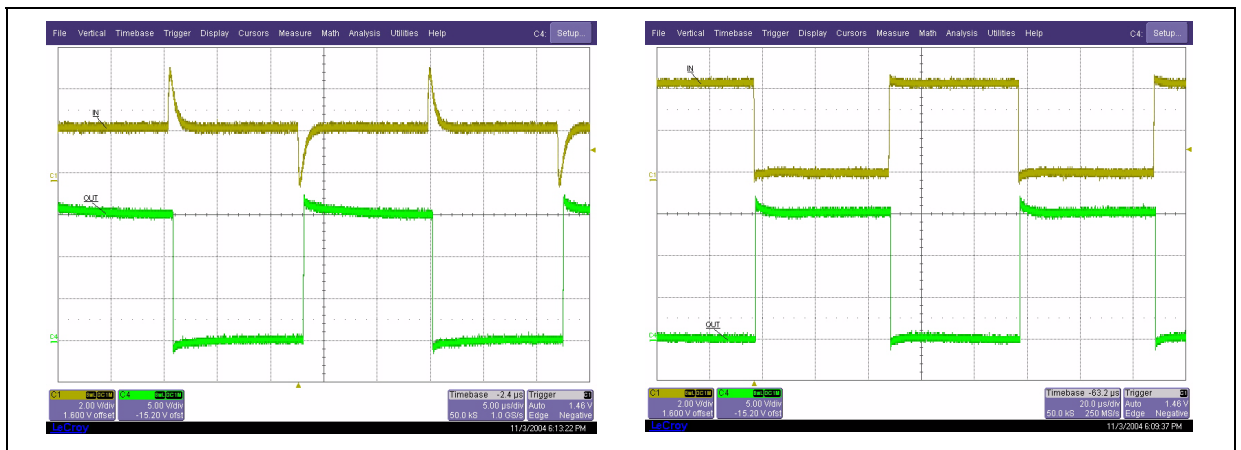
When using an optocoupler, the IN pin can be pulled-up to Vref. The pull up resistor is to be chosen between 5 k $\Omega$  to 20 k $\Omega$  depending on the characteristics of the optocoupler. An optional filtering capacitor can be added in case of a highly noisy environment, although the TD351 already includes filtering on input signals and rejects signals smaller than 135 ns ( $t_{onmin}$  specification).

Waveforms from the pulse transformer must comply with the  $t_{onmin}$  and  $V_{ton}/V_{toff}$  specifications (see [Figure 5](#)). To turn TD351 output on, the input signal must be lower than 0.8 V for 220 ns minimum. Conversely, the input signal must be higher than 4.2 V for 220 ns minimum in order to turn off TD351 output. A pulse width of about 500 ns at the threshold levels is recommended. In all cases, input signal at the IN pin must be between 0 and 5 V.

**Figure 4. Application schematic (pulse transformer at left; optocoupler at right)**



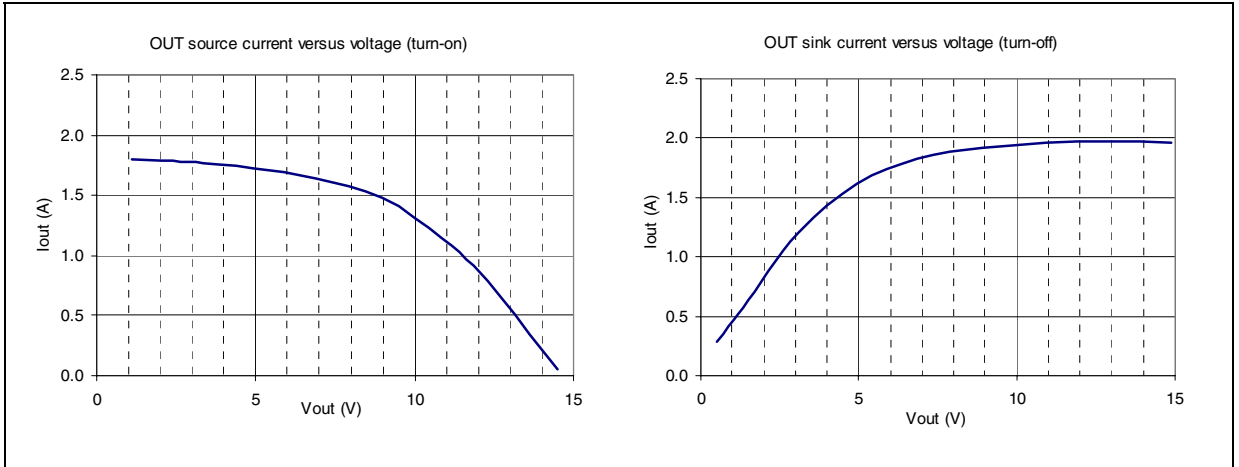
**Figure 5. Typical input signal waveforms with pulse transformer (left) or optocoupler (right)**



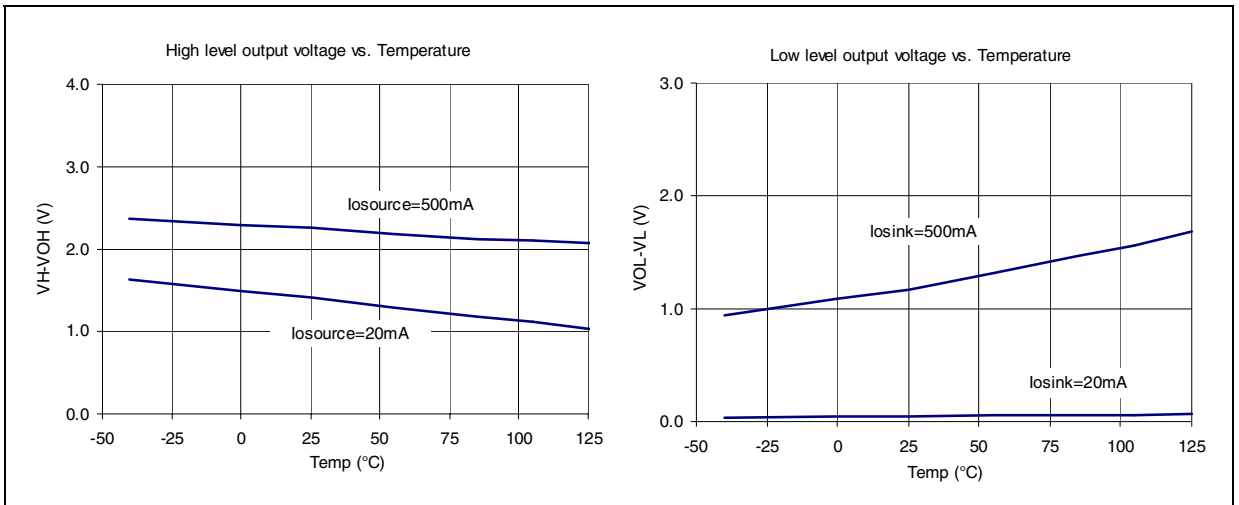
## 4 Output stage

The output stage is able to sink/source about 1.7 A / 1.3 A typical at 25°C with a voltage drop VOL/VOH of 6 V (see [Figure 6](#)). The minimum sink/source currents over the full temperature range (-20°C/+125°C) are 1 A sink and 0.75 A source. VOL and VOH voltage drops at 0.5 A are guaranteed to 2.5 V and 4 V maximum respectively, over the temperature range (see [Figure 7](#)). This current capability sets the limit of IGBT driving, and the IGBT gate resistor should not be lower than about 15Ω.

**Figure 6. Typical Output stage current capability at 25°C (VH=16V)**



**Figure 7. Typical VOL and VOH voltage variation with temperature**



## 5 Active Miller clamp

The TD351 offers an alternative solution to the problem of Miller current in IGBT switching applications.

Traditional solutions to the Miller current problem are:

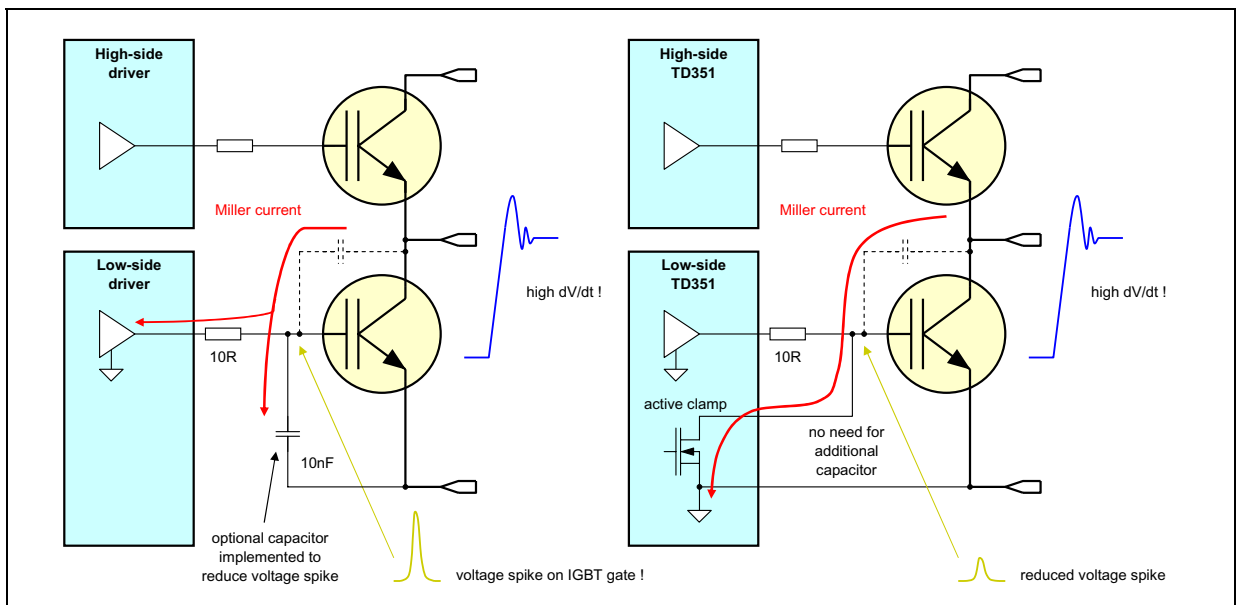
- to drive the IGBT gate to a negative voltage in OFF-state in order to increase the safety margin
- or, to implement an additional capacitor between the IGBT gate and collector as described in the left-hand schematic in [Figure 8](#))

The solution proposed by the TD351 uses a dedicated CLAMP pin to control the Miller current. When the IGBT is off, a low impedance path is established between IGBT gate and emitter to carry the Miller current, and the voltage spike on the IGBT gate is greatly reduced (see the right-hand schematic in [Figure 8](#)). The CLAMP switch is open when the input is activated and is closed when the actual gate voltage goes close to the ground level. In this way, the CLAMP function doesn't affect the turn-off characteristics, but simply keeps the gate at a low level during the entire off-time.

The main benefit is that negative supply voltage can be avoided in most cases, allowing for the use of a bootstrap technique for the high-side driver supply, and a consistent cost reduction for the application.

In addition, the use of the active Miller clamp feature avoids the need to implement any additional capacitors between the IGBT gate and the collector. Such capacitors would negatively affect the ability of the driver to control turn-on and turn-off.

**Figure 8. Active Miller Clamp: principles of operation**

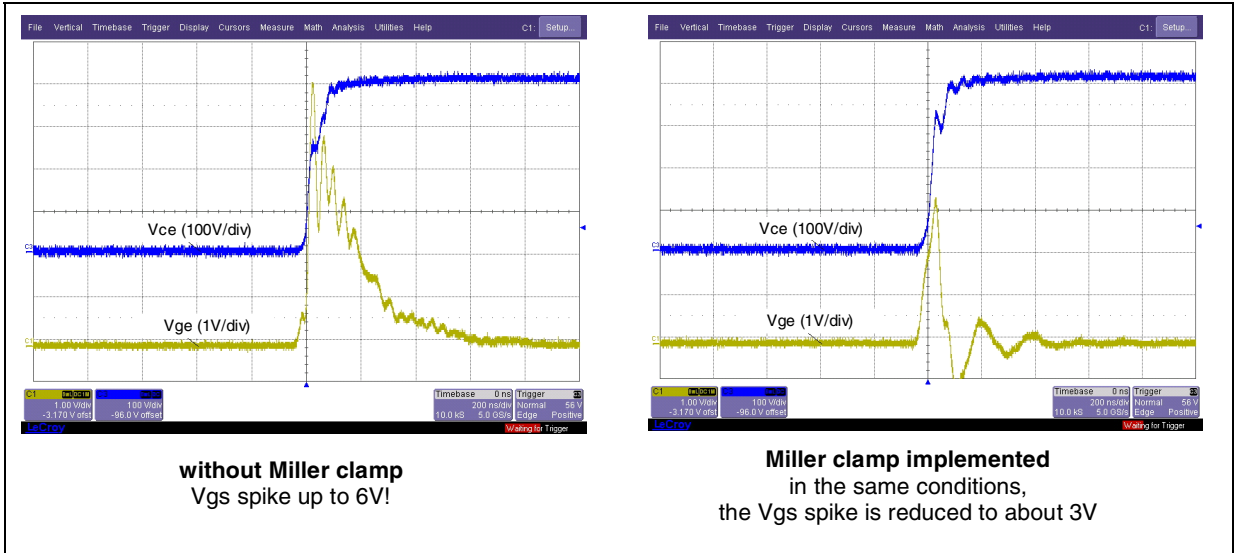


The test results shown in [Figure 9](#) prove how the active Miller clamp results in a consistent reduction of the voltage spike on IGBT gate.

The left-hand waveform shows the result of a 400 V switching with a 10 nF additional Gate to Emitter capacitor to control the voltage spike on gate.

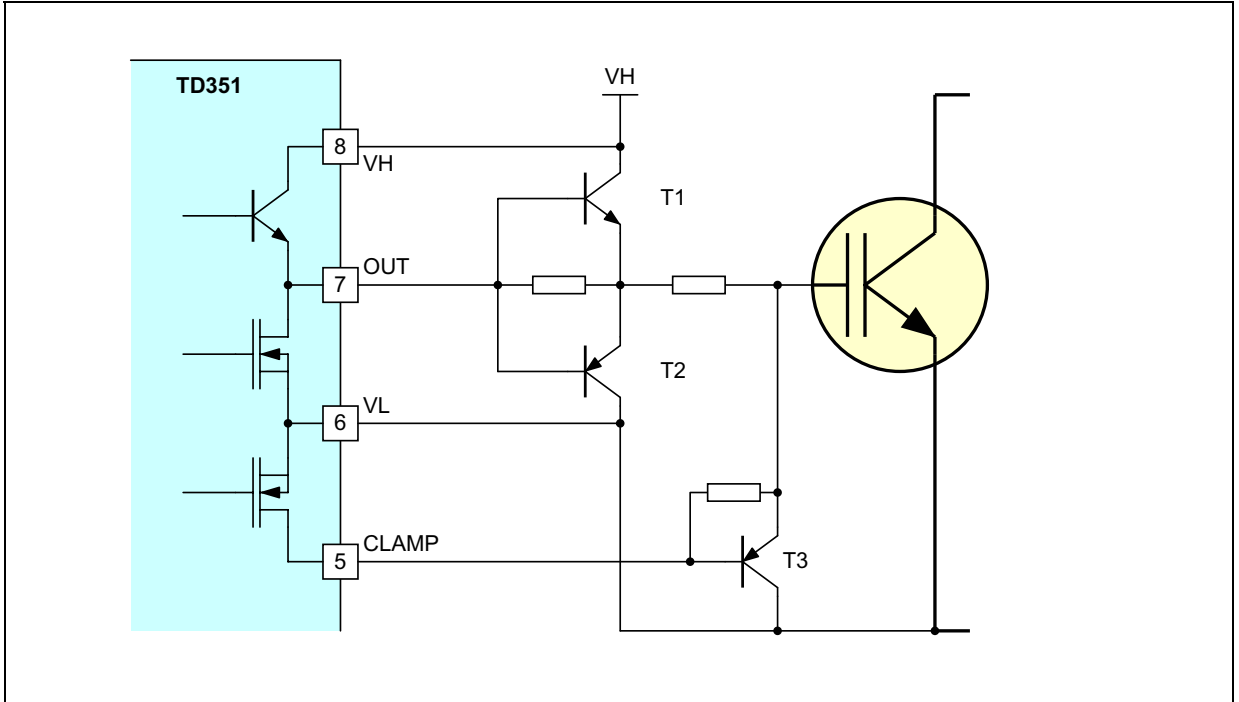
The right-hand waveform shows the results of the test in the same conditions but without any additional capacitors and with the active Miller clamp.

Figure 9. Active Miller clamp: test waveforms related to above schematic



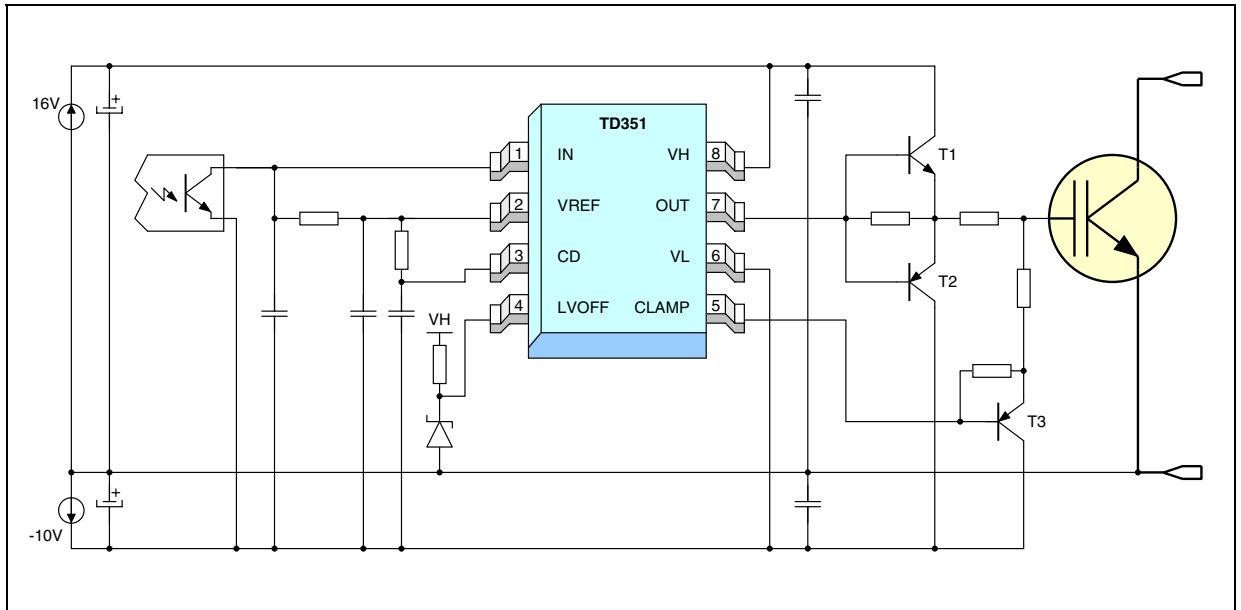
For high-power applications, buffers can be used to increase the output current capability. Figure 10 shows a schematic principle with external buffers for both the driver output and the clamp function.

Figure 10. Using external buffer to increase the current capability of the driver and clamp outputs



For very high-power applications, the active clamp function cannot replace the negative gate drive, due to the effect of the parasitic inductance of the active clamp path. In these cases, the application can benefit from the CLAMP output as a secondary gate discharge path (see [Figure 11](#) below).

**Figure 11. High power application: negative gate drive and secondary gate discharge path**



With the above schematic, when the gate voltage goes close to  $V_L+2\text{ V}$  (i.e. the IGBT is already driven off), the CLAMP pin is activated. Again, the benefit is to lower the resistance between gate and emitter when the IGBT is in the OFF state without affecting the IGBT turn-off characteristics.



**Tip:** *What should one do with the CLAMP pin when not used in application?  
Connect CLAMP to  $V_L$ .*

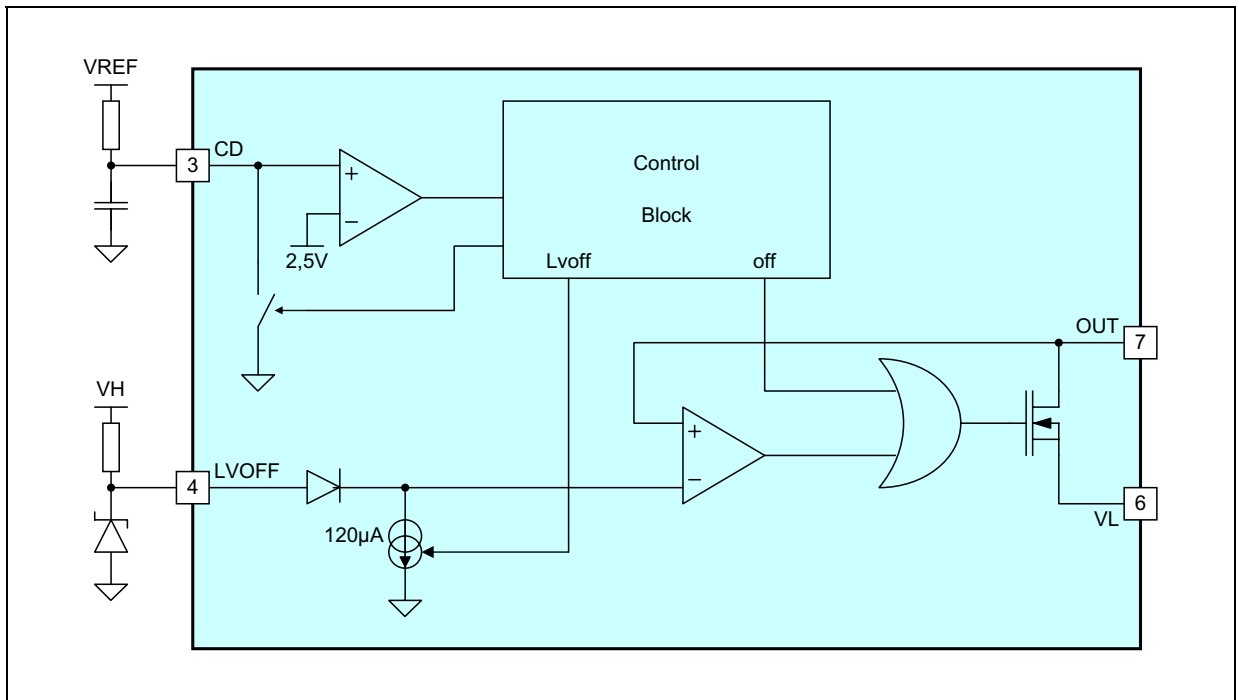
## 6 2-Level turn-off

In the event of a short-circuit or overcurrent in the load, a large voltage overshoot can occur across the IGBT at turn-off and can exceed the IGBT breakdown voltage. By reducing the gate voltage before turn-off, the IGBT current is limited and the potential over-voltage is reduced. This technique is called *2-level turn-off*. Both the level and duration of the intermediate off level are adjustable. The duration is set by an external resistor/capacitor in conjunction with the integrated voltage reference for accurate timing. The level can be easily set by an external Zener diode, and its value is chosen depending upon the IGBT's characteristics. This 2-level turn-off sequence takes place at each cycle; it has no effect if the current doesn't exceed the normal maximum rated value, but protects the IGBT in case of overcurrent (with a slight increase to conduction losses).

The principle is shown on [Figure 12](#). During the 2-level turn-off time, the OUT pin is controlled by a comparator between the actual OUT pin and an external reference voltage. When the voltage on OUT goes down as a result of the turn-off and reaches the reference threshold, then the OUT output is disabled and the IGBT gate is discharged no further. After the 2-level turn-off delay, the OUT output is enabled again to end the turn-off sequence.

To keep the output signal width unchanged relative to the input signal, the turn-on is delayed by the same value than the 2-level turn-off delay (see [Figure 13](#)).

**Figure 12. Principle schematic for 2-level turn-off feature**



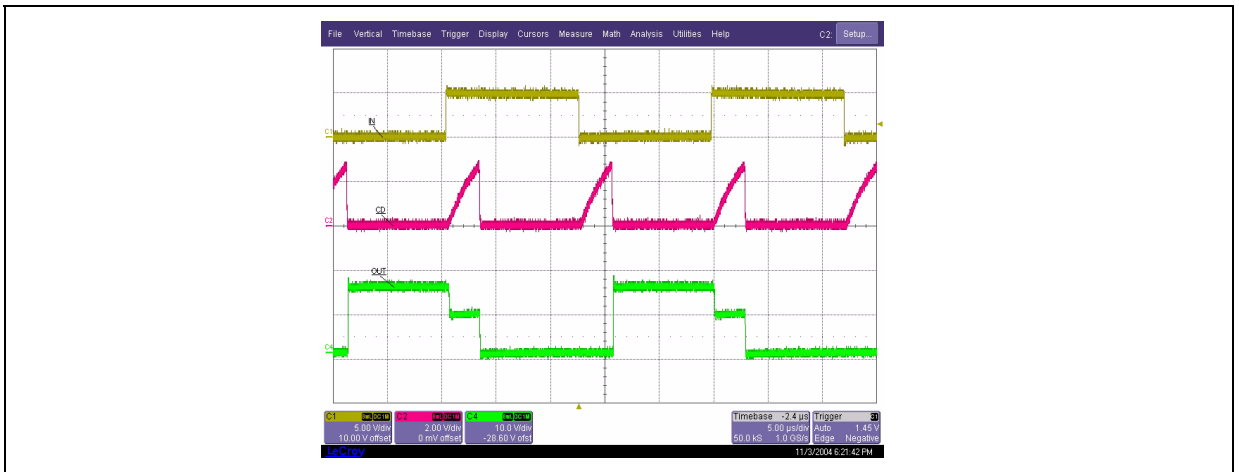
The duration of the 2-level turn-off is set by the external Rd-Cd components, and is approximately given by the formula:

$$T_a \text{ (in } \mu\text{s)} = 0.7 * R_d \text{ (in k}\Omega\text{)} * C_d \text{ (in nF)}$$

Recommended values are  $R_d$  from 10k $\Omega$  to 20k $\Omega$ , and  $C_d$  from 100 pF to 470 pF, providing a range of delay from about 0.7 to 6.6 microseconds.



Figure 13. Waveforms of the 2-level turn-off function (COFF timing exaggerated for illustration)



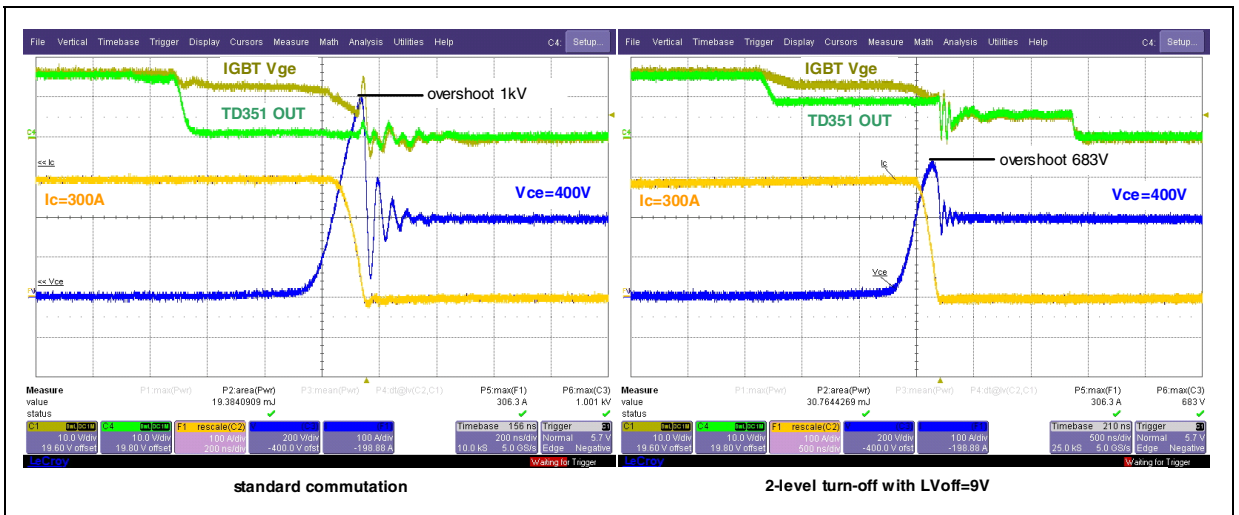
Practical tests were made with 1200 V - 50 A IGBT modules Fuji 6MBI50S120L. The results shown in [Figure 14](#) point out how the 2-level turn-off feature can consistently reduce voltage stress on the IGBT in the event of over-current.

During this test, the 50 A-rated IGBT module has to turn-off a 300 A current simulating an application faulty condition.

The left-hand graph in [Figure 14](#) shows a standard commutation. The driver OUT pin voltage is abruptly pulled from 16 V to 0 V and the IGBT gate is discharged through the gate resistor. The fast turn-off of the IGBT generates a voltage spike on Vce reaching **1 kV**, which is dangerously close to the IGBT absolute maximum rating (1200 V). The calculated turn-off energy reaches **19 mJ**.

The right-hand graph in [Figure 14](#) shows how the TD351 and its 2-level turn-off feature can help deal with this situation. During the first phase, the TD351 OUT pin is pulled from 16 V to 9 V during 2.5  $\mu$ s. In the second phase the OUT pin is pulled to 0 V. As a consequence, the IGBT turn-off is slightly longer and the Vce voltage spike is advantageously reduced to **683 V**. The calculated turn-off energy reaches **31 mJ**, but the resulting overheating can be more easily managed than the destruction of the IGBT by over-voltage stress.

Figure 14. Reduction of IGBT over-voltage stress using 2-level turn-off feature



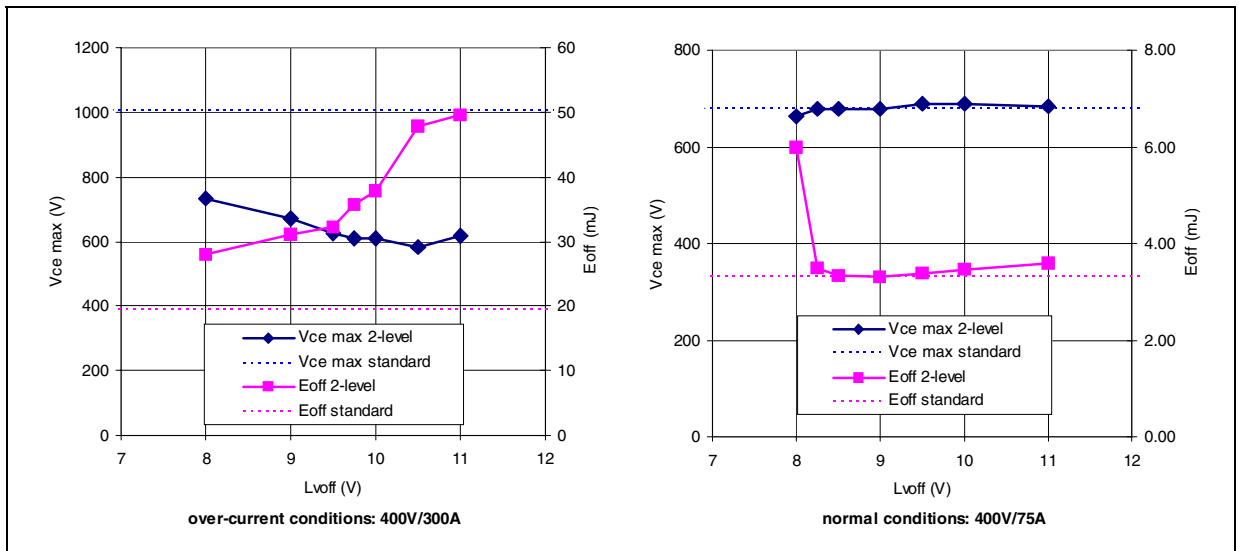
Maximum voltage reached on the IGBT collector and commutation losses are shown in the charts of [Figure 15](#). The influence of the LVoff value is studied both for nominal rated current at 25°C (75 A) and over current (300 A) conditions.

It can be noted that in over-current conditions (see [Figure 15](#), left graph) the 2-level turn-off can bring a significant reduction of Vcemax during turn-off. With LVoff values from 8 to 11 V, Vcemax is reduced from 1000 V to less than 750 V. The price to pay is an increase of the switching losses Eoff that are shifted from 20 mJ to 30~40 mJ.

In normal conditions (see [Figure 15](#), right graph) there is no noticeable difference to be seen regardless whether the 2-level turn-off feature is used or not, as long as LVoff is greater than 8.5 V.

These results suggest that it is useful to set the LVoff value from 9 to 10 V.

**Figure 15. Influence of LVoff value on Vcemax and turn-off energy (IGBT Fuji 6MBI50S120L)**



**Tip:**

**How does one disable the 2-level turn-off feature?**

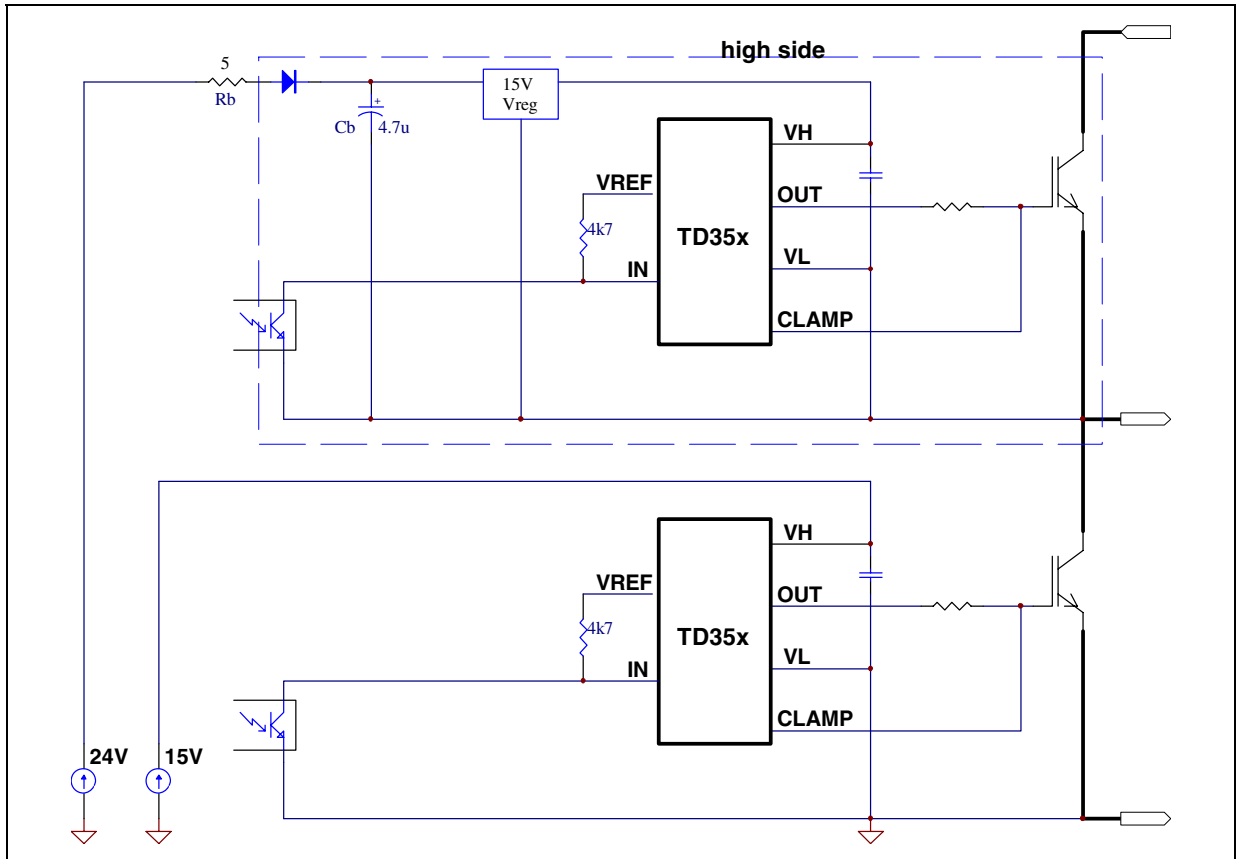
Connect LVOFF to VH, remove  $C_d$  capacitor and keep the CD pin connected to Vref by a 4.7 k $\Omega$  to 10 k $\Omega$  resistor.

## 7 Application schematic

The TD351 application design presented hereafter is based on the active Miller clamp concept. With this function, the high-side driver can be supplied with a bootstrap system instead of using a floating positive/negative supply. This concept is applicable to low- and medium-power systems, up to about 10 kW. Main benefit of this is to reduce the global application cost by making the supply system simpler. *Figures 16* shows the half bridge design concept using the TD35x.

It should be highlighted that the active Miller clamp is fully managed by the TD35x and doesn't require any special action from the system controller.

**Figure 16. TD35x application concept**



The TD351 is able to drive 1200 V IGBT modules up to 50 A or 75 A (depending on IGBT technology and manufacturer). Key parameters to consider are the TD351 peak output current (0.75 A source / 1.0 A sink) and the IGBT gate resistor.

The values of gate resistors should be chosen starting with the recommended values from the IGBT manufacturer. Thanks to the active Miller clamp function, the gate resistor can be tuned independently from the Miller effect, which normally puts some constraints on the gate resistor. The benefit is to optimize the turn-on and turn-off behavior, especially regarding switching losses and EMI issues.

*Table 1* shows the recommended gate resistors values from two major IGBT module manufacturers, and the peak gate current (with a 15 V supply) required for 10 A to 100 A IGBT modules. Approximate application power is indicated.

Table 1. Recommended gate resistors

<b>Eupec: FPxxR12KE3</b>		<b>15</b>	<b>25</b>		<b>40</b>	<b>50</b>	75		A
Rgate		<b>75</b>	<b>36</b>		<b>27</b>	<b>18</b>	5		$\Omega$
Ipeak		<b>0.2</b>	<b>0.4</b>		<b>0.55</b>	<b>0.8</b>	3		A
<b>Fuji: 6MBIxxS-120</b>	<b>10</b>	<b>15</b>	<b>25</b>	<b>35</b>		<b>50</b>	<b>75</b>	100	A
Rgate	<b>120</b>	<b>82</b>	<b>51</b>	<b>33</b>		<b>24</b>	<b>16</b>	12	$\Omega$
Ipeak	<b>0.12</b>	<b>0.2</b>	<b>0.3</b>	<b>0.45</b>		<b>0.6</b>	<b>0.9</b>	1.3	A
<b>App. Power</b>	<b>1.5</b>	<b>2</b>	<b>3</b>	<b>4</b>	<b>5</b>	<b>7</b>	<b>11</b>	15	kW

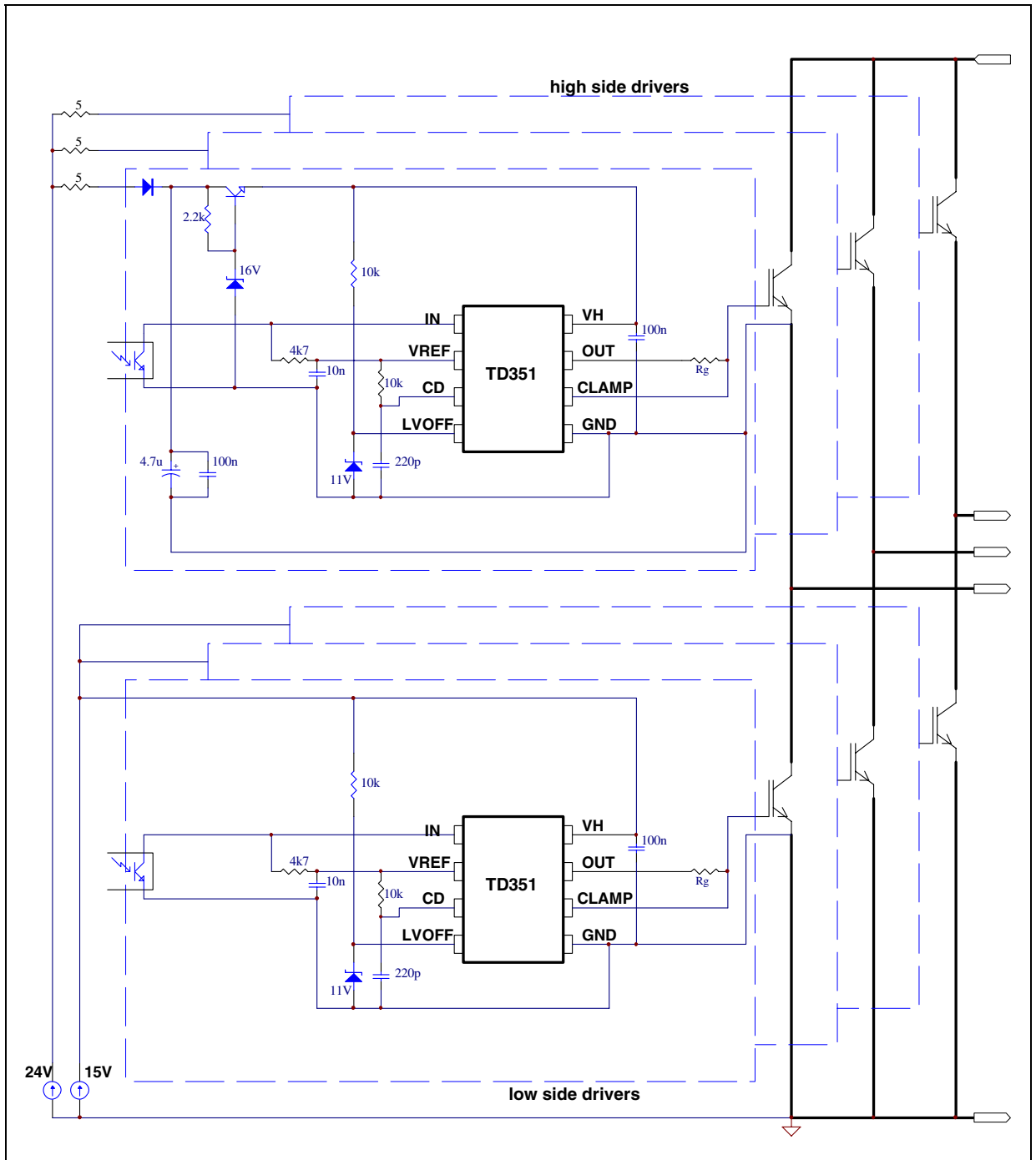
IGBT modules suitable for TD351 are indicated in bold. For the FP50R12KE3 and 6MBI75S-120 modules, the source (charging) peak current will be limited to 0.75 A in worst-case conditions instead of the theoretical 0.8 A or 0.9 A peak values; this usually doesn't affect the application performance.

An external buffer will be required for higher power applications.

A reference schematic is shown in [Figure 17](#). It uses a bootstrap principle for the high-side driver supply. A very simple voltage regulator is used in front of the TD351 high-side driver. In this way, the bootstrap supply voltage can be made significantly higher than the target driver supply, and the voltage across the Cb bulk capacitor can exhibit large voltage variations during each cycle with no impact on the driver operation.

Gate resistor Rg depends on the IGBT. It should be noted that the applications only use two supplies referenced to the ground level.

Figure 17. TD351 Application Schematic with 2-Level Turn-off



## 8 Conclusion

The TD351 is part of the new TD35x IGBT driver family, and is designed for 1200 V, 3-phase inverter applications, especially for motor control and UPS systems. It covers a large range of power applications, from 0.5 kW to more than 100 kW. Thanks to its Active Miller Clamp feature and low quiescent current, it can help avoid using negative gate driving for application up to 10 kW and simplifies the global power supply system for cost-sensitive applications.

## 9 Revision history

Date	Revision	Description of changes
01 Feb. 2005	1	First release.

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics  
All other names are the property of their respective owners

© 2005 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)