

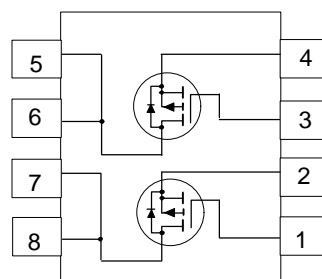
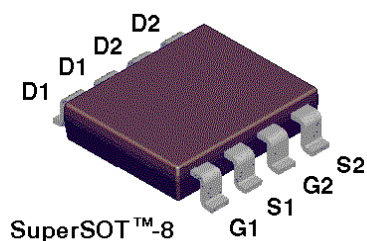
## NDH8304P Dual P-Channel Enhancement Mode Field Effect Transistor

### General Description

SuperSOT™-8 P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

### Features

- 2.7 A, -20 V.  $R_{DS(ON)} = 0.07 \Omega @ V_{GS} = -4.5 \text{ V}$   
 $R_{DS(ON)} = 0.095 \Omega @ V_{GS} = -2.7 \text{ V}$ .
- Proprietary SuperSOT™-8 package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low  $R_{DS(ON)}$ .
- Exceptional on-resistance and maximum DC current capability.



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	NDH8304P	Units
$V_{DSS}$	Drain-Source Voltage	-20	V
$V_{GSS}$	Gate-Source Voltage	$\pm 8$	V
$I_D$	Drain Current - Continuous (Note 1)	-2.7	A
	- Pulsed	-10	
$P_D$	Maximum Power Dissipation (Note 1)	0.8	W
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	156	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ\text{C/W}$

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-20			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$ $T_J = 55^\circ\text{C}$			-1	$\mu\text{A}$
					-10	$\mu\text{A}$
$I_{GSSF}$	Gate - Body Leakage, Forward	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate - Body Leakage, Reverse	$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
<b>ON CHARACTERISTICS</b> (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$ $T_J = 125^\circ\text{C}$	-0.4	-0.7	-1	V
			-0.3	-0.5	-0.8	
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -4.5\text{ V}, I_D = -2.7\text{ A}$ $T_J = 125^\circ\text{C}$		0.061	0.07	$\Omega$
				0.087	0.125	
			$V_{GS} = -2.7\text{ V}, I_D = -2.3\text{ A}$		0.082	0.095
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$ $V_{GS} = -2.7\text{ V}, V_{DS} = -5\text{ V}$	-10			A
			-3			
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -2.7\text{ A}$		8		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		865		pF
$C_{oss}$	Output Capacitance			415		pF
$C_{rss}$	Reverse Transfer Capacitance			150		pF
<b>SWITCHING CHARACTERISTICS</b> (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = -5\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$		11	22	ns
$t_r$	Turn - On Rise Time			25	50	ns
$t_{D(off)}$	Turn - Off Delay Time			78	150	ns
$t_f$	Turn - Off Fall Time			55	100	ns
$Q_g$	Total Gate Charge	$V_{DS} = -10\text{ V},$ $I_D = -2.7\text{ A}, V_{GS} = -4.5\text{ V}$		16	23	nC
$Q_{gs}$	Gate-Source Charge			2.4		nC
$Q_{gd}$	Gate-Drain Charge			5.1		nC

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current				-0.67	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = -0.67\text{ A}$ (Note 2)		-0.7	-1.2	V

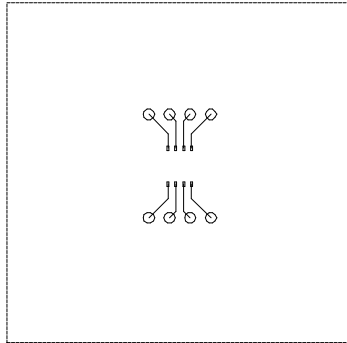
Notes:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)} \theta_{TJ}$$

Typical  $R_{\theta JA}$  using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

156°C/W when mounted on a 0.0025 in<sup>2</sup> pad of 2oz copper.



Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

## Typical Electrical Characteristics

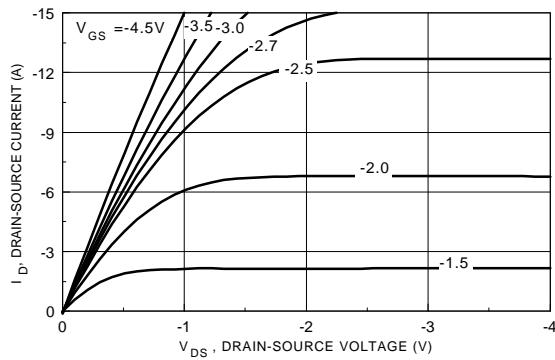


Figure 1. On-Region Characteristics.

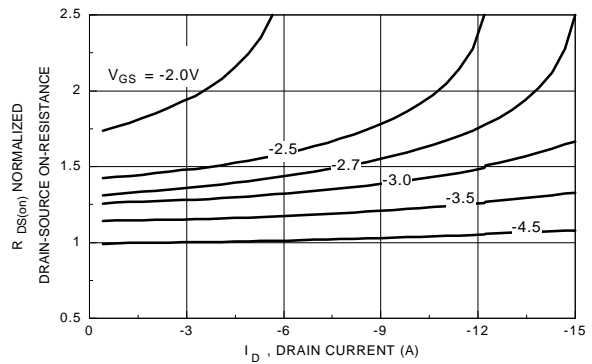


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

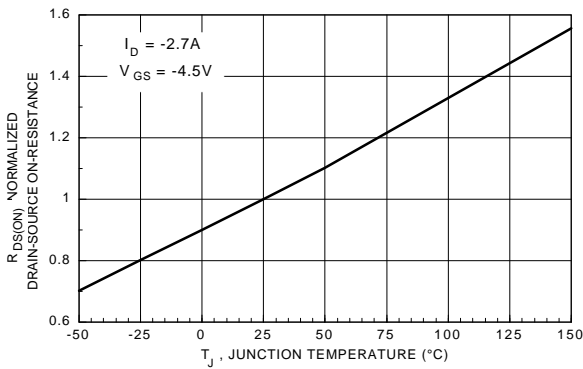


Figure 3. On-Resistance Variation with Temperature.

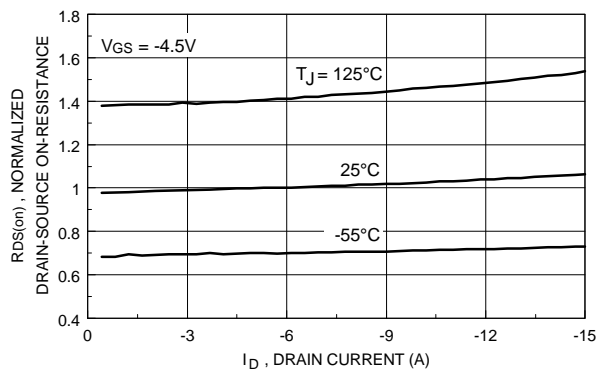


Figure 4. On-Resistance Variation with Drain Current and Temperature.

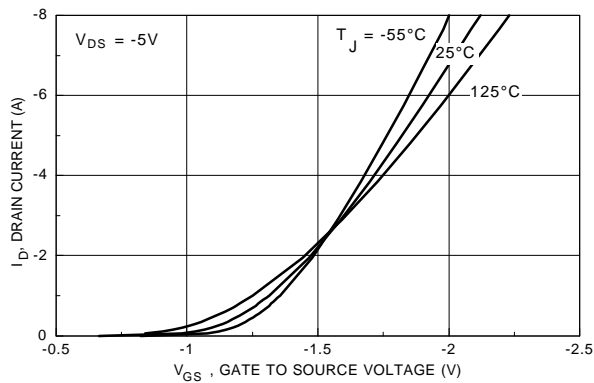


Figure 5. Transfer Characteristics.

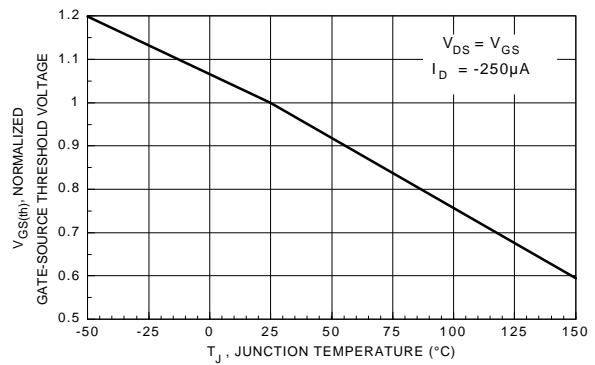
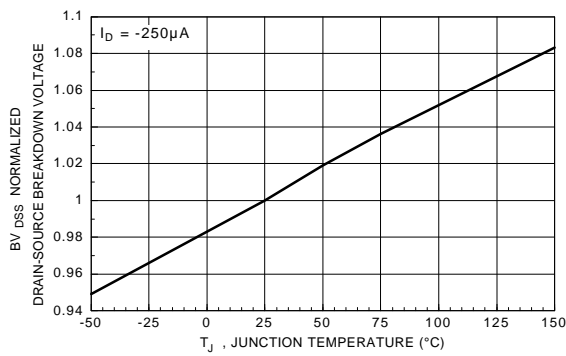
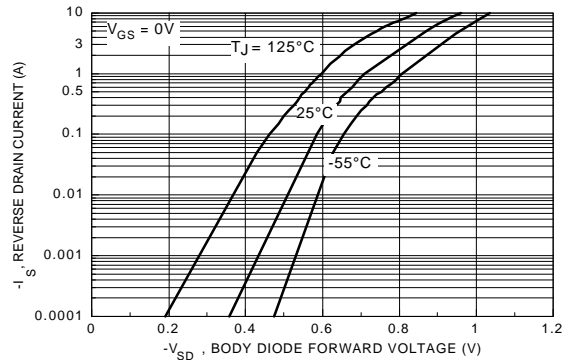


Figure 6. Gate Threshold Variation with Temperature.

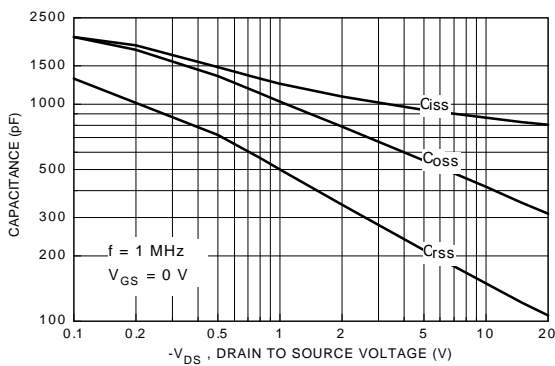
## Typical Electrical Characteristics



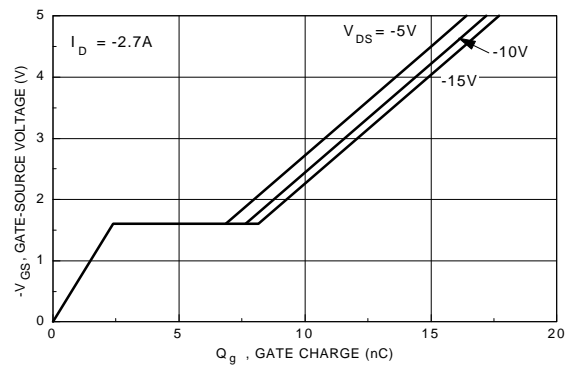
**Figure 7. Breakdown Voltage Variation with Temperature.**



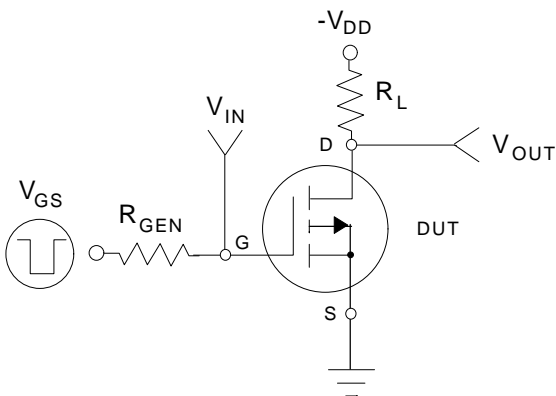
**Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.**



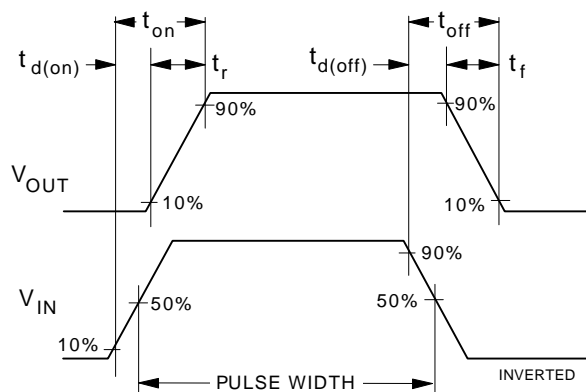
**Figure 9. Capacitance Characteristics.**



**Figure 10. Gate Charge Characteristics.**



**Figure 11. Switching Test Circuit.**



**Figure 12. Switching Waveforms.**

## Typical Electrical and Thermal Characteristics

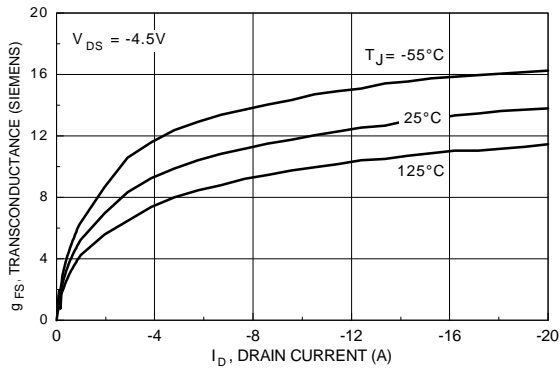


Figure 13. Transconductance Variation with Drain Current and Temperature.

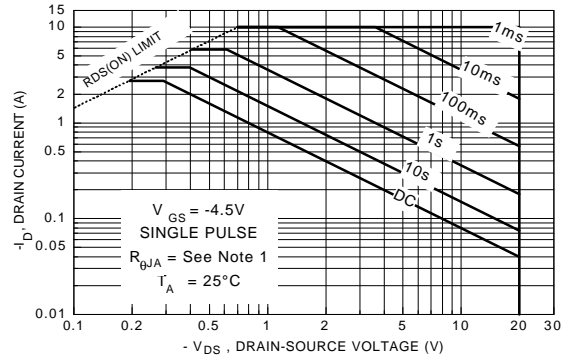


Figure 14. Maximum Safe Operating Area.

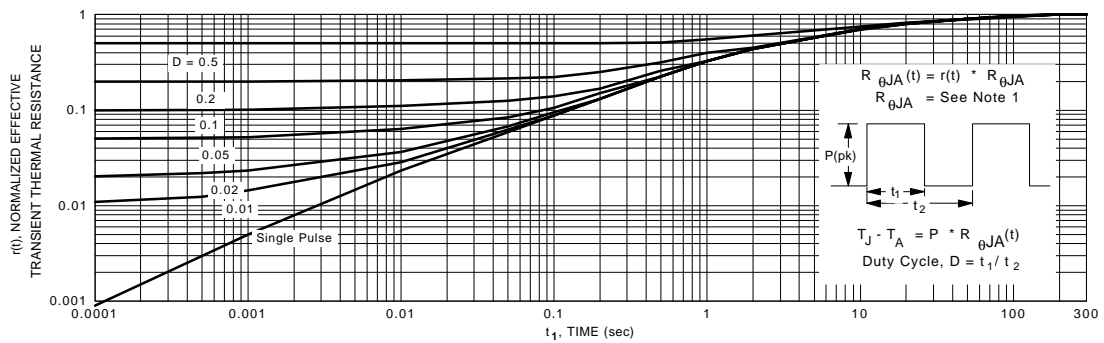


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1. Transient thermal response will change depending on the circuit board design.