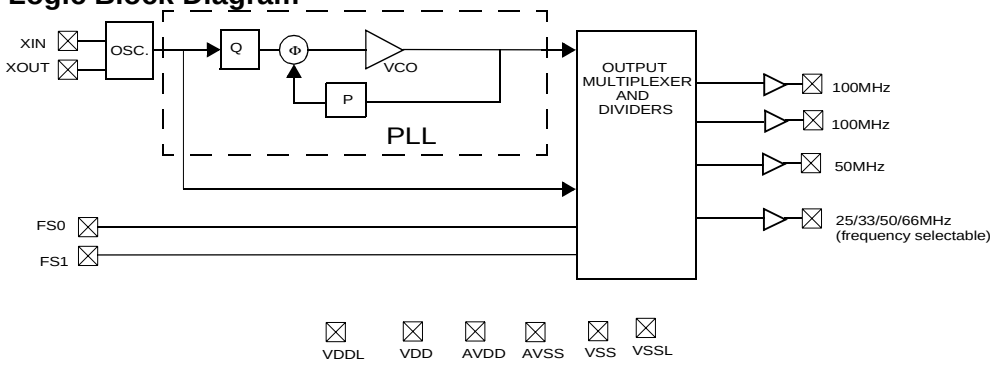
CY26114

One-PLL Clock Generator

Features	Benefits
• **Integrated phase-locked loop**	Internal PLL with up to 333 MHz internal operation
• **Low skew, low jitter, high accuracy outputs**	Meets critical timing requirements in complex system designs
• **3.3V Operation with 2.5 V Output Option**	Enables application compatibility

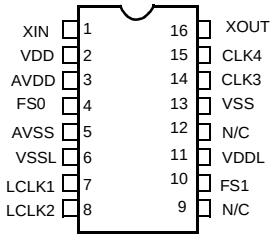
Part Number	Outputs	Input Frequency	Output Frequency Range
CY26114	4	25MHz Crystal Input	2 copies of 100MHz, 1 copy of 50MHz, 1 copy 25/33/50/66MHz (frequency selectable)

Logic Block Diagram



Pin Configurations

16-pin TSSOP



CLK4 Frequency Select Options

FS1	FS0	CLK 4	Units
0	0	25	MHz
0	1	33	MHz
1	0	50	MHz
1	1	66	MHz

Pin Definitions

Name	Pin Number	Description
XIN	1	Reference Crystal Input
V_{DD}	2	Voltage Supply
AV_{DD}	3	Analog Voltage Supply
FS0	4	Frequency Select 0
AV_{SS}	5	Analog Ground
V_{SSL}	6	LCLK Ground
LCLK1	7	100-MHz output clock at V_{DDL} Level
LCLK2	8	100-MHz output clock at V_{DDL} Level
N/C	9	No Connect
FS1	10	Frequency Select 1
V_{DDL}	11	LCLK Voltage Supply (2.5V or 3.3V)
N/C	12	No Connect
VSS	13	Ground
CLK3	14	50-MHz output clock
CLK4	15	25/33/50/66-MHz clock output (frequency selectable)
XOUT	16	Reference Crystal Output

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	–0.5	7.0	V
V_{DDL}	I/O Supply Voltage		7.0	V
T_J	Junction Temperature		125	°C
	Digital Inputs	AV_{SS} – 0.3	AV_{DD} + 0.3	V
	Digital Outputs referred to V_{DD}	V_{SS} – 0.3	V_{DD} + 0.3	V
	Digital Outputs referred to V_{DDL}	V_{SS} – 0.3	V_{DDL} +0.3	V
	Electro-Static Discharge	2		kV

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	3.0	3.3	3.6	V
V_{DDL}	Operating Voltage	2.375	2.5	2.625	V
T_A	Ambient Temperature	0		70	°C
C_{LOAD}	Max. Load Capacitance			15	pF
f_{REF}	Reference Frequency		25		MHz
t_{PU}	Power-up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic)	0.05		500	ms

Note:
1. Float XOUT if XIN is externally driven.

DC Electrical Characteristics

Parameter[2]	Name	Description	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} – 0.5$, $V_{DD}/V_{DDL} = 3.3V$	12	24		mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD}/V_{DDL} = 3.3V$	12	24		mA
I_{OH}	Output High Current	$V_{OH} = V_{DDL} – 0.5$, V_{DDL}=2.5V	8	16		mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DDL} = 2.5V$	8	16		mA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	0.7			VDD
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}			0.3	VDD
I_{VDD}	Supply Current	AV_{DD}/V_{DD} Current			25	mA
I_{VDDL}	Supply Current	V_{DDL} Current ($V_{DDL} = 3.6V$)			20	mA
I_{VDDL}	Supply Current	V_{DDL} Current ($V_{DDL} = 2.625V$)			15	mA

AC Electrical Characteristics

Parameter[2]	Name	Description	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in Figure 1; t1/t2, 50% of V_{DD}	45	50	55	%
t_3	Rising Edge Rate	Output Clock Rise Time, 20% – 80% of $V_{DD}/V_{DDL} = 3.3V$	0.8	1.4		V/ns
t_3	Rising Edge Rate	Output Clock Rise Time, 20% – 80% of $V_{DDL} = 2.5V$	0.6	1.2		V/ns
t_4	Falling Edge Rate	Output Clock Fall Time, 80% – 20% of $V_{DD}/V_{DDL} = 3.3V$	0.8	1.4		V/ns
t_4	Falling Edge Rate	Output Clock Fall Time, 80% – 20% of $V_{DDL} = 2.5V$	0.6	1.2		V/ns
t5	Skew	Delay between related outputs at rising edge			250	ps
t9	Clock Jitter	Peak to Peak period jitter			200	ps
t10	PLL Lock Time				3	ms

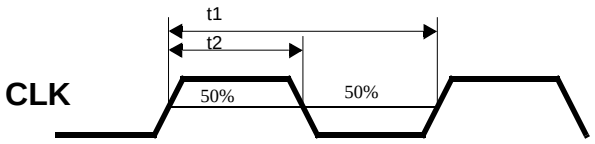


Figure 1. Duty Cycle Definitions: DC = t2/t1.

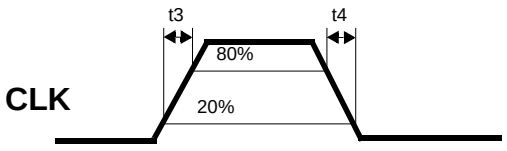
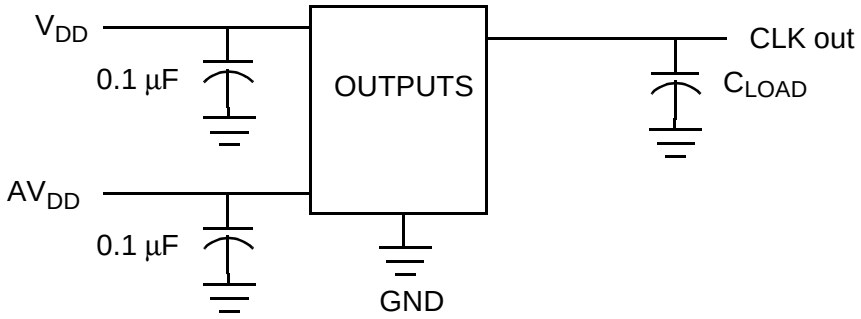


Figure 2. Rise Time and Fall Time Definitions.

Note:
2. Not 100% tested.

Test Circuit



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY26114ZC	Z16	16-Pin TSSOP	Commercial	3.3V

Document Title: CY26114 One-PLL Clock Generator Document Number: 38-07098				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107333	08/28/01	CKN	New Data Sheet
*A	121867	12/14/02	RBI	Power up requirements added to Operating Conditions Information