FailSafe™ PacketClock™ Global Communications Clock Generator

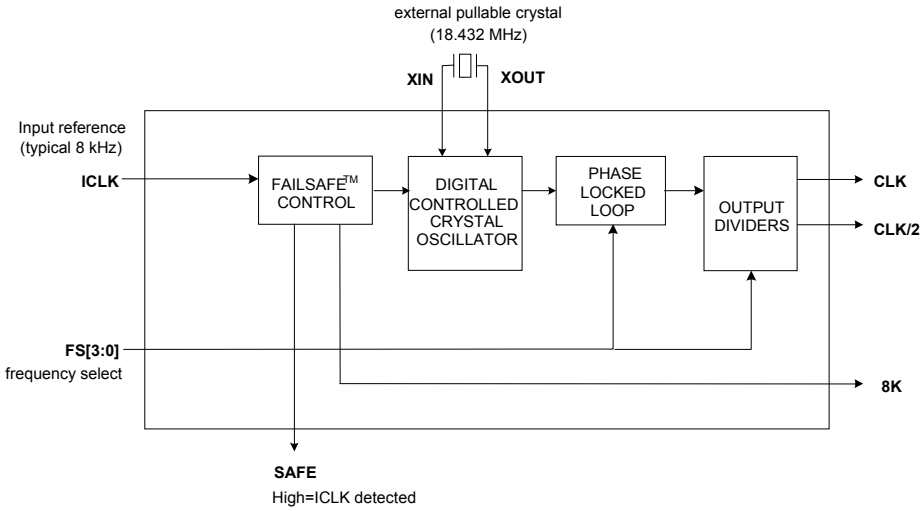
Features

- Fully integrated phase-locked loop (PLL)
- FailSafe™ output
- PLL driven by a crystal oscillator that is phase aligned with external reference
- Output frequencies selectable and/or programmed to standard communication frequencies
- Low-jitter, high-accuracy outputs
- Commercial and Industrial operation
- 3.3V ± 5% operation
- 16-lead TSSOP

Benefits

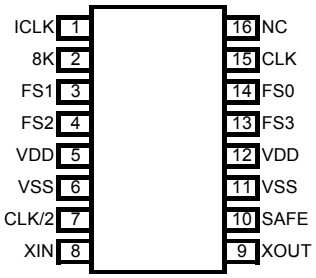
- Integrated high-performance PLL tailored for telecommunications frequency synthesis eliminates the need for external loop filter components
- When reference is in range, SAFE pin is driven high.
- When reference is off, DCXO maintains clock outputs. SAFE pin is low.
- DCXO maintains continuous operation should the input reference clock fail
- Glitch-free transition simplifies system design
- Selectable output clock rates include T1/DS1, E1, T3/DS3, E3, and OC-3.
- Works with commonly available, low-cost 18.432-MHz crystal
- Zero-ppm error for all output frequencies
- Performance guaranteed for applications that require an extended temperature range
- Compatible across industry standard design platforms
- Industry standard package with 6.4 x 5.0 mm^2 footprint and a height profile of just 1.1 mm.

Logic Block Diagram



Pin Configuration

CY26049-36
16-pin TSSOP
Top View



Pin Definitions

Pin Name	Pin Number	Pin Description
ICLK	1	**Reference Input Clock**; 8 kHz or 10 to 60 MHz.
8K	2	**Clock Output**; 8 kHz or high impedance in buffer mode.
FS1	3	**Frequency Select 1**; Determines CLK outputs per *Table 1*.
FS2	4	**Frequency Select 2**; Determines CLK outputs per *Table 1*.
VDD	5	**Voltage Supply;** 3.3V.
VSS	6	**Ground**
CLK/2	7	**Clock Output**; Frequency per *Table 1*.
XIN	8	**Pullable Crystal Input;** 18.432 MHz.
XOUT	9	**Pullable Crystal Output**; 18.432 MHz.
SAFE	10	**High = reference ICLK within range, Low = reference ICLK out of range**.
VSS	11	**Ground**
VDD	12	**Voltage Supply;** 3.3V.
FS3	13	**Frequency Select 3**; Determines CLK outputs per *Table 1*.
FS0	14	**Frequency Select 0**; Determines CLK outputs per *Table 1*.
CLK	15	**Clock Output**; Frequency per *Table 1*.
NC	16	**No Connect**

Selector Guide

Part Number	Input Frequency Range	Outputs	Output Frequencies
CY26049-36	8 kHz or 10 to 60 MHz Reference Input Crystal: 18.432-MHz pullable Crystal per Cypress Specification	3	8 kHz to 155.52 MHz Selectable (see *Table 1*)

Functional Description

CY26049 is a FailSafe frequency synthesizer with a reference clock input and three clock outputs. The device provides an optimum solution for applications where continuous operation is required in the event of a primary clock failure. The continuous, glitch-free operation is achieved by using a DCXO which serves as a primary clock source. The FailSafe control circuit synchronizes the DCXO with the reference as long as the reference is within the pull range of the crystal.

In the event of a reference clock failure the DCXO maintains the last frequency and phase information of the reference clock. The unique feature of the CY26049-36 is that the DCXO is in fact the primary clocking source. When the reference clock is restored, the DCXO automatically re-synchronizes to the reference. The status of the reference clock input, as detected by the CY26049-36, is reported by the SAFE pin.

In the buffer mode (FS3:FS0 = 1110 or 1111), the CY26049-36 can be used as a jitter attenuator. In this mode, extensive jitter on the input clock will be “filtered”, resulting in a low-jitter output clock.

Frequency Select Tables

Table 1. CY26049-36 Frequency Select–Output Decoding Table–External Mode (MHz except as noted)

ICLK	FS3	FS2	FS1	FS0	CLK/2	CLK	8K	Crystal
8 kHz	0	0	0	0	1.544	3.088	8 kHz	18.432
8 kHz	0	0	0	1	2.048	4.096	8 kHz	18.432
8 kHz	0	0	1	0	22.368	44.736	8 kHz	18.432
8 kHz	0	0	1	1	17.184	34.368	8 kHz	18.432
8 kHz	0	1	0	0	77.76	155.52	8 kHz	18.432
8 kHz	0	1	0	1	16.384	32.768	8 kHz	18.432
8 kHz	0	1	1	0	14.352	28.704	8 kHz	18.432
8 kHz	0	1	1	1	High Z[1]	High Z[1]	High Z[1]	18.432
8 kHz	1	0	0	0	18.528	37.056	8 kHz	18.432
8 kHz	1	0	0	1	12.352	24.704	8 kHz	18.432
8 kHz	1	0	1	0	7.68	15.36	8 kHz	18.432
8 kHz	1	0	1	1	High Z[1]	High Z[1]	High Z[1]	18.432
8 kHz	1	1	0	0	12.288	24.576	8 kHz	18.432
8 kHz	1	1	0	1	16.384	32.768	8 kHz	18.432

Table 2. CY26049-36 Frequency Select–Output Decoding Table–Buffer Mode

ICLK	FS3	FS2	FS1	FS0	CLK/2	CLK	8K	Crystal
20 to 60	1	1	1	0	ICLK/2	ICLK	High Z[1]	ICLK/2
10 to 30	1	1	1	1	2*ICLK	4*ICLK	High Z[1]	ICLK

Note:
1. High Z = high impedance.

Absolute Maximum Conditions

Supply Voltage (V_{DD}) .....–0.5 to +7.0V
DC Input Voltage .....–0.5V to V_{DD}+0.5
Storage Temperature (Non-Condensing) ....–55°C to +125°C
Junction Temperature ..... –40°C to +125°C
Data Retention @ Tj=125°C.....>10 years
Package Power Dissipation..... 350 mW
ESD (Human Body Model) MIL-STD-883..... 2000V
(Above which the useful life may be impaired. For user guidelines, not tested.

Recommended Pullable Crystal Specifications[2]

Parameter	Description	Comments	Min.	Typ.	Max.	Units
F_{NOM}	Nominal crystal frequency	Parallel resonance, fundamental mode, AT cut	–	18.432	–	MHz
C_{LNOM}	Nominal load capacitance		–	14	–	pF
R_1	Equivalent series resistance (ESR)	Fundamental mode	–	–	25	Ω
R_3/R_1	Ratio of third overtone mode ESR to fundamental mode ESR	Ratio used because typical R_1 values are much less than the maximum spec	3	–	–	
DL	Crystal drive level	No external series resistor assumed	–	0.5	2	mW
F_{3SEPHI}	Third overtone separation from 3*F_{NOM}	High side	400	–	–	ppm
F_{3SEPLO}	Third overtone separation from 3*F_{NOM}	Low side	–	–	–200	ppm
C_0	Crystal shunt capacitance		–	–	7	pF
C_0/C_1	Ratio of shunt to motional capacitance		180	–	250	
C_1	Crystal motional capacitance		14.4	18	21.6	fF

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	3.15	3.3	3.45	V
T_{AC}	Ambient Temperature (Commercial Temperature)	0	–	70	° C
T_{AI}	Ambient Temperature (Industrial Temperature)	–40	–	85	° C
C_{LOAD}	Max Output Load Capacitance	–	–	15	pF
t_{pu}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms
$t_{ER(I)}$	8 kHz Input Edge Rate, 20% to 80% of V_{DD} = 3.3V	0.07	–	–	V/ns

DC Electrical Specifications (Commercial Temp: 0° to 70°C)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current	V_{OH} = V_{DD} – 0.5, V_{DD} = 3.3V (source)	12	24	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.5, V_{DD} = 3.3V (sink)	12	24	–	mA
V_{IH}	Input High Voltage	CMOS Levels	0.7	–	–	V_{DD}
V_{IL}	Input High Voltage	CMOS Levels	–	–	0.3	V_{DD}
I_{IH}	Input High Current	V_{IH}=V_{DD}	–	5	10	µA
I_{IL}	Input Low Current	V_{IL}=0V	–	5	10	µA
C_{IN}	Input Capacitance		–	–	7	pF
I_{OZ}	Output Leakage Current	High Z[1] output	–	± 5	–	µA
I_{DD}	Supply Current	C_{LOAD} = 15 pF, V_{DD} = 3.45V, FS [3:0] = 0100	–	–	45	mA
		C_{LOAD} = 15 pF, V_{DD} = 3.45V, FS [3:0] = 1101	–	–	30	mA

Note:
2. Ecliptek ECX-5761-18.432 M and ECX-5762-18.432 M meets these specifications.

DC Electrical Specifications (Industrial Temp: –40° to 85°C)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} – 0.5$, $V_{DD} = 3.3V$ (source)	10	20	–	mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD} = 3.3V$ (sink)	10	20	–	mA
V_{IH}	Input High Voltage	CMOS Levels	0.7	–	–	V_{DD}
V_{IL}	Input High Voltage	CMOS Levels	–	–	0.3	V_{DD}
I_{IH}	Input High Current	$V_{IH} = V_{DD}$	–	5	10	µA
I_{IL}	Input Low Current	$V_{IL} = 0V$	–	5	10	µA
C_{IN}	Input Capacitance		–	–	7	pF
I_{OZ}	Output Leakage Current	High Z[1] output	–	± 5	–	µA
I_{DD}	Supply Current	$C_{LOAD} = 15$ pF, $V_{DD} = 3.45V$, FS [3:0] = 0100	–	–	50	mA
		$C_{LOAD} = 15$ pF, $V_{DD} = 3.45V$, FS [3:0] = 1101	–	–	35	mA

AC Electrical Specifications (Commercial Temp: 0° to 70° C and Industrial Temp: –40° to 85°C)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
f_{ICLK-E}	Frequency, Input Clock	Input Clock Frequency, External Mode	–	8.00	–	kHz
f_{ICLK-B}	Frequency, Input Clock	Input Clock Frequency, Buffer Mode	10	–	60	MHz
LR	FailSafe Lock Range[3]	Range of reference ICLK for Safe = High	–250	–	+250	ppm
DC = t_2/t_1	Output Duty Cycle	Duty Cycle defined in *Figure 1*, measured at 50% of V_{DD}	45	50	55	%
T_{PJIT1}	Clock Jitter; output > 5 MHz	Period Jitter, Peak to Peak, 10,000 periods	–	–	250	ps
		RMS Period Jitter, RMS	–	–	50	ps
T_{PJIT2}	Clock Jitter; output <5 MHz	Period Jitter, Peak to Peak, 10,000 periods	–	–	500	ps
		RMS Period Jitter, RMS	–	–	100	ps
t_6	PLL Lock Time	Time for PLL to lock within ± 150 ppm of target frequency	–	–	3	ms
t_{fs_lock}	Failsafe Lock Time	Time for PLL to lock to ICKL (outputs phase aligned with ICKL and Safe = High)	–	–	7	s
f_{error}	Frequency Synthesis Error	Actual mean frequency error vs. target	–	0	–	ppm
ER	Rising Edge Rate	Output Clock Edge Rate, Measured from 20% to 80% of V_{DD}, $C_{LOAD} = 15$ pF See *Figure 2*.	0.8	1.4	2	V/ns
EF	Falling Edge Rate	Output Clock Edge Rate, Measured from 20% to 80% of V_{DD}, $C_{LOAD} = 15$ pF See *Figure 2*.	0.8	1.4	2	V/ns

Voltage and Timing Definitions

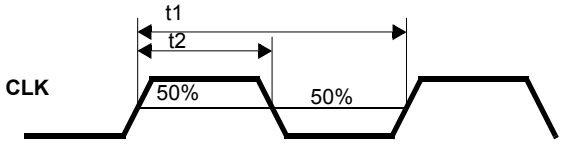


Figure 1. Duty Cycle Definition; DC = t2/t1

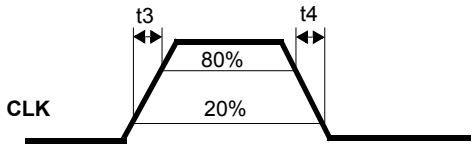
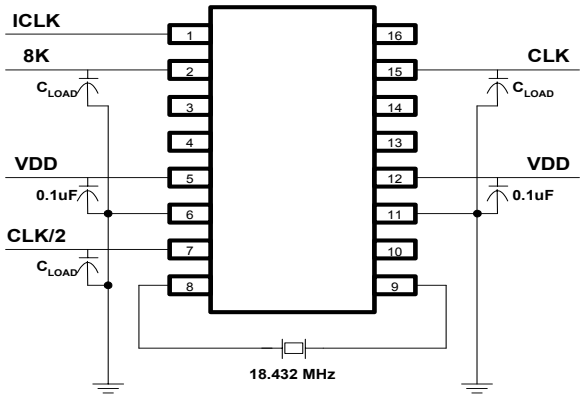


Figure 2. Rise and Fall Time Definitions: ER = 0.6 x VDD / t3, EF = 0.6 x VDD / t4

Note:
3. Dependent on crystals chosen and crystal specs.

Test Circuit

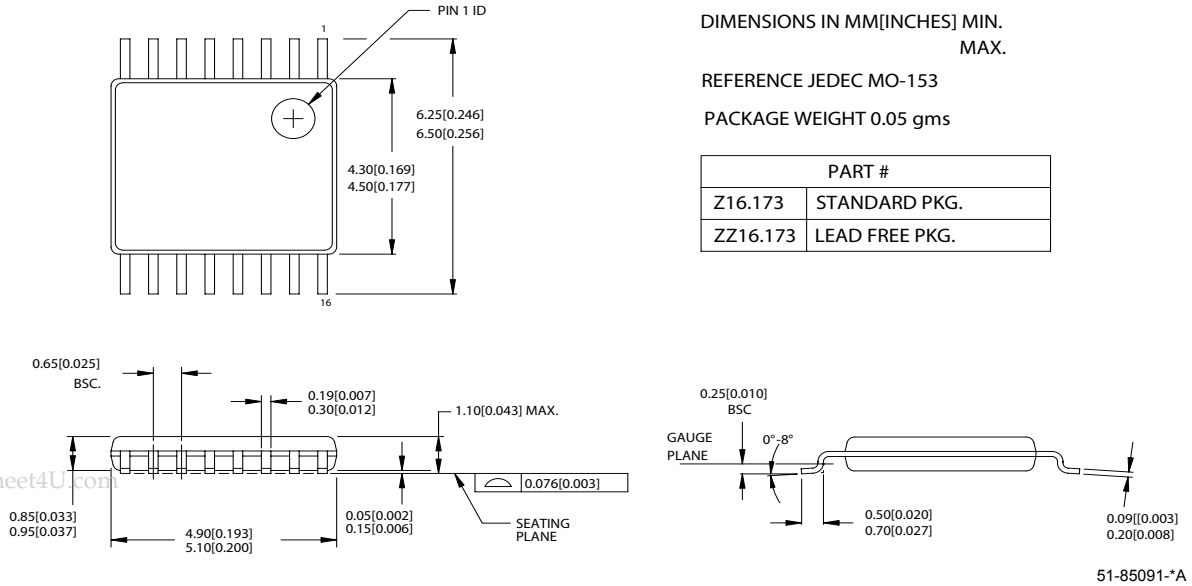


Ordering Information

Ordering Code	Package Type	Operating Temperature Range
CY26049ZC-36	16-lead TSSOP	Commercial 0 to 70°C
CY26049ZC-36T	16-lead TSSOP–Tape and Reel	Commercial 0 to 70°C
CY26049ZI-36	16-lead TSSOP	Industrial –40 to 85°C
CY26049ZI-36T	16-lead TSSOP–Tape and Reel	Industrial –40 to 85°C
Lead Free		
CY26049ZXC-36	16-lead TSSOP	Commercial 0 to 70°C
CY26049ZXC-36T	16-lead TSSOP–Tape and Reel	Commercial 0 to 70°C
CY26049ZXI-36	16-lead TSSOP	Industrial –40 to 85°C
CY26049ZXI-36T	16-lead TSSOP–Tape and Reel	Industrial –40 to 85°C

Package Diagram

16-lead TSSOP 4.40 MM Body Z16.173



FailSafe and PacketClock are trademarks of Cypress Semiconductor. All product and company names mentioned in this document are the trademarks of their respective holders.

Document History Page

Document Title: CY26049-36 FailSafe™ PacketClock™ Global Communications Clock Generator Document Number: 38-07415				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	114749	08/08/02	CKN	New Data Sheet
*A	120067	01/06/03	CKN	Changed “FailSafe is a trademark of Silicon Graphics, Inc.” to read “FailSafe is a trademark of Cypress Semiconductor”
*B	128000	07/15/03	IJA	Changed Benefits to read “When reference is in range, SAFE pin is driven high” Changed first sentence to “CY26049 is a FailSafe frequency synthesizer with a reference clock input and three clock outputs” Changed title from “Failsafe™ PacketClock™ Global Communications Clocks” to “FailSafe™ PacketClock™ Global Communications Clock Generator” Changed definitions in Pin Description Table Replaced format for Absolute Maximum Conditions Replaced Recommended Pullable Crystal Specifications table Added t_{pu} to Recommended Operating Conditions Added I_{IH} and I_{IL} to DC Electrical Specifications Replaced AC Electrical Specifications from Cy26049-16 data sheet Changed Voltage and Timing Definitions to match CY2410 data sheet Moved Package Diagram to end of data sheet
*C	244412	See ECN	RGL	Spec. ($t_{ER(I)}$) Input Edge Rate in the Recommended Operating Conditions Table Added Lead Free Devices