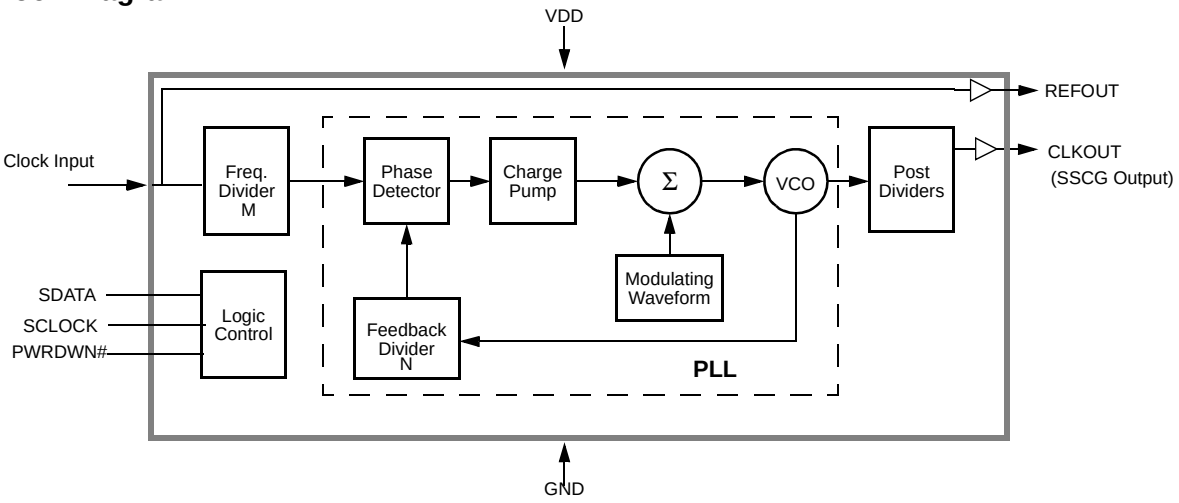
CK-SSC Spread Spectrum Clock Generator

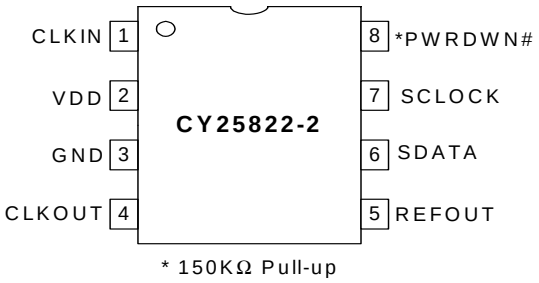
Features

- **3.3V operation**
- **48- and 66-MHz frequency support**
- **Selectable slew rate control**
- **350-pS jitter**
- **I^2C programmability**
- **500-μA power-down current**
- **Spread Spectrum for best electromagnetic interference (EMI) reduction**
- **8-pin SOIC package**

Block Diagram



Pin Configuration



Pin Description

Pin No.	Pin Name	Pin Type	Pin Description
1	CLKIN	Input	**48-MHz or 66-MHz Clock Input**.
2	VDD	Power	**Power Supply for PLL and Outputs**.
3	GND	Ground	**Ground for Outputs**.
4	CLKOUT	Output	**48-MHz or 66-MHz Spread Spectrum Clock Output**.
5	REFOUT	Output	**Non-spread Spectrum Reference Clock Output**.
6	SDATA	I/O	**I^2C-compatible SDATA**.
7	SCLOCK	Input	**I^2C-compatible SCLOCK**.
8	PWRDWN#	Output	**LVTTL Input for PowerDown# Active Low**.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions such as individual clock output buffers, etc., can be individually enabled or disabled.

The registers associated with the Serial Data Interface initializes to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operation from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individual indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 1*.

The block write and block read protocol is outlined in *Table 2* while *Table 3* outlines the corresponding byte write and byte read protocol.The slave receiver address is 11010100 (D4h).

Table 1. Command Code Definition

Bit	Description
7	0 = Block read or block write operation 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be ’0000000’

Table 2. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits '00000000' stands for block operation	11:18	Command Code – 8 bits '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29:36	Data byte 1 – 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 2 – 8 bits	30:37	Byte count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge
....	.....	39:46	Data byte from slave – 8 bits
....	Data Byte (N–1) –8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte from slave – 8 bits

Table 2. Block Read and Block Write Protocol (continued)

....	Data Byte N –8 bits	56	Acknowledge
....	Acknowledge from slave	....	Data bytes from slave/Acknowledge
....	Stop	....	Data byte N from slave – 8 bits
		....	Not Acknowledge
		....	Stop

Table 3. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits '1xxxxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code – 8 bits '1xxxxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte from master – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29	Stop	28	Read = 1
		29	Acknowledge from slave
		30:37	Data byte from slave – 8 bits
		38	Not Acknowledge
		39	Stop

Byte 0: Control Register

Bit	@Pup	Pin#	Name	Pin Description
7	1	4	SS0	–
6	0	4	SS1	–
5	0	4	SS2	–
4	0	4	SS3	–
3	1		Not Applicable	Reserved, must be written as 1
2	1	4, 5	CLKOUT, REFOUT	Power-down three-state enable 0 = three-state outputs, 1 = drive outputs low (Applies only in Power Down State)
1	1	4	CLKOUT	Spread Spectrum enable 0 = spread off, 1 = spread on
0	0		Not Applicable	No Pins

Table 4. Spread Spectrum Select

SS3	SS2	SS1	SS0	Spread Mode	Spread Amount%
0	0	0	0	Down	0.8
0	0	0	1	Down	1.0
0	0	1	0	Down	1.25
0	0	1	1	Down	1.5
0	1	0	0	Down	1.75

Table 4. Spread Spectrum Select (continued)

SS3	SS2	SS1	SS0	Spread Mode	Spread Amount%
0	1	0	1	Down	2.0
0	1	1	0	Down	2.5
0	1	1	1	Down	3.0
1	0	0	0	Center	±0.3
1	0	0	1	Center	±0.4
1	0	1	0	Center	±0.5
1	0	1	1	Center	±0.6
1	1	0	0	Center	±0.8
1	1	0	1	Center	±1.0
1	1	1	0	Center	±1.25
1	1	1	1	Center	±1.5

Byte 1: Control Register

Bit	@Pup	Pin#	Name	Pin Description
7	1	5	REFEN	REFOUT enable 0 = disabled, 1 = enabled
6	1	5	REFSLEW	REFOUT edge rate control 0 = slow, 1 = nominal
5	0		Not Applicable	Reserved.
4	0		Not Applicable	Reserved
3	1	4	CLKSLEW	CLKOUT edge rate control 0 = slow, 1 = nominal
2	1	4	CLKEN	CLKOUT enable 0 =disabled, 1 = enabled
1	0		Not Applicable	Reserved
0	0		Not Applicable	Reserved

Bytes 2 through 5: Reserved Registers

Byte 6: Vendor/Revision ID Register

Bit	@Pup	Pin#	Name	Pin Description
7	0	–	–	Revision ID Bit 3
6	0	–	–	Revision ID Bit 2
5	0	–	–	Revision ID Bit 1
4	0	–	–	Revision ID Bit 0
3	1	–	–	Vendor ID Bit 3
2	0	–	–	Vendor ID Bit 2
1	0	–	–	Vendor ID Bit 1
0	0	–	–	Vendor ID Bit 0

PWRDWN# (Power-down) Clarification

The PWRDWN# (Power-down) pin is used to shut off ALL clocks prior to shutting off power to the device. PWRDWN# is an asynchronous active LOW input. This signal is synchronized internally to the device powering down the clock synthesizer. PWRDWN# is an asynchronous function for powering up the system. When PWRDWN# is low, all clocks are driven to a LOW value and held there and the VCO and PLLs are also powered down. All clocks are shut down in a synchronous manner so has not to cause glitches while transitioning to the low 'stopped' state. When PWRDWN# is deasserted the clocks should remain stopped until the VCO is stable and within specification (t_{STABLE}). A stopped clock is either tri-stated or driven low depending on the state of the tri-state enable I^2C register bit. CY25822 clocks that are stopped in the driven state are driven low.

The CLKIN input must be on and within specified operating parameters before PWRDWN# is asserted and it must remain in this state while PWRDWN# is asserted.

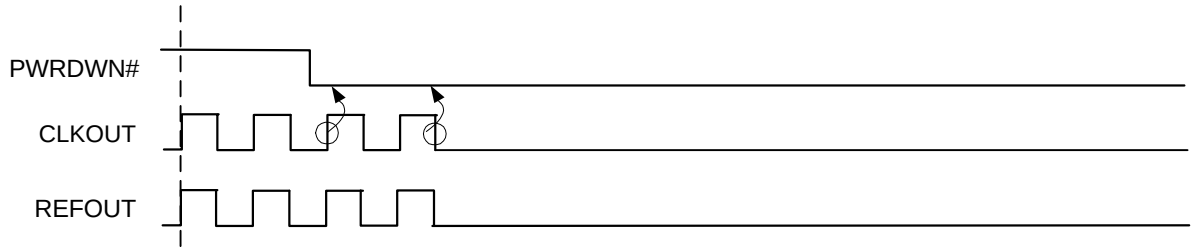


Figure 1. Power-down Assertion

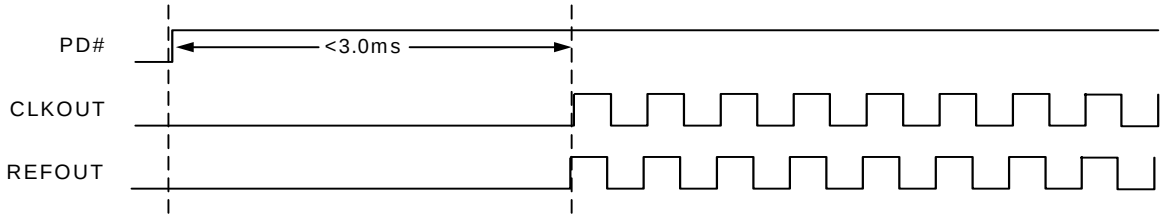


Figure 2. Power-down Deassertion

CLKOUT and REFOUT Enable Clarification

The CLKOUT enable and REFOUT enable I^2C register bits are used to shot-off the CLKOUT and REFOUT clocks individually. The VCO and crystal oscillator must remain on. A shutdown clock is driven low. ALL clocks need to be stopped in a predictable manner. All clocks need to be shutdown without any glitches or other abnormal behavior while transitioning to a stopped state. Similarly when CLKOUT or REFOUT is enabled the clock must start in a predictable manner without any glitches or abnormal behavior.

Table 5. Absolute Maximum Ratings

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}	Core Supply Voltage		–0.5	4.6	V
V_{DD_A}	Analog Supply Voltage		–0.5	4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, Storage	Non Functional	–65	+150	°C
T_A	Temperature, Operating Ambient	Functional	0	70	°C
T_J	Temperature, Junction	Functional	–	150	°C
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	Volts
UL–94	Flammability Rating	@1/8 in.	V–0		
MSL	Moisture Sensitivity Level		1		

Table 6. DC Parameters (T_A = 0°C to +70°C, V_{DD} = 3.3V ± 5%)

Parameter	Description	Condition	Min.	Max	Unit	Notes
V_{DD}	Supply Voltage	–	3.135	3.465	V	V_{DD} = 3.3 ± 5%
V_{IH}	Input High Voltage	–	2.0	V_{DD} + 0.3	V	
V_{IL}	Input Low Voltage	–	V_{SS} – 0.3	0.8	V	
I_{IL1}	Input Leakage Current	SCLOCK or SDATA	–25	+25	µA	
I_{IL2}	Input Leakage Current	PWRDWN#	–75	–15	µA	
V_{OH}	Output High Voltage	I_{OH} = –4 mA	2.4	–	V	Single edge is required to be monotonic when transitioning through this region.
V_{OL}	Output Low Voltage	I_{OL} = 4 mA	–	0.4	V	Single edge is required to be monotonic when transitioning through this region.
C_{IN}	Input Pin Capacitance	–	–	5	pF	
C_{OUT}	Output Pin Capacitance	–	–	6	pF	
L_{IN}	Pin Inductance	–	–	7	nH	
T_A	Ambient Temperature	–	0	70	°C	No air flow
I_{DD1}	Supply Current	@ 66 MHz	–	50	mA	
I_{DD2}	Supply Current	@ 48 MHz	–	40	mA	
I_{PD}	Power Down Supply Current	–	–	500	µA	

Table 7. AC Parameters (T_A = 0°C to +70°C, V_{DD} = 3.3V ± 5%)

Parameter	Description	Conditions	Min.	Max.	Unit	Notes
t_{HIGH}	CLK High Time, 48MHz	Measured @2.4V	9.45	10.95	ns	Specification applies to 48MHz output mode.
t_{LOW}	CLK, Low Time, 48MHz	Measured @0.4V	8.50	10.10	ns	Specification applies to 48MHz output mode.
t_{HIGH}	CLK High Time, 66MHz	Measured @2.4V	6.85	7.90	ns	Specification applies to 66.7MHz output mode.
t_{LOW}	CLK Low Time, 66MHz	Measured @0.4V	5.95	6.95	ns	Specification applies to 66.7MHz output mode.
t_{RISEH1}	Rising Edge Rate	Measured from 0.4V to 2.4V REFOUT and CLOCKOUT	2.0	5.0	V/ns	High Buffer Strength Refer to I^2C Control
t_{FALLH1}	Falling Edge Rate	Measured from 2.4V to 0.4V REFOUT and CLOCKOUT	2.0	5.0	V/ns	High Buffer Strength Refer to I^2C Control
t_{RISEL1}	Rising Edge Rate	Measured from 0.4V to 2.4V REFOUT and CLOCKOUT	1.33	4.0	V/ns	Low Buffer Strength Refer to I^2C Control

Table 7. AC Parameters (T_A = 0°C to +70°C, V_{DD} = 3.3V ± 5%) (continued)

Parameter	Description	Conditions	Min.	Max.	Unit	Notes
t_{FALLL1}	Falling Edge Rate	Measured from 2.4V to 0.4V REFOUT and CLOCKOUT	1.33	4.0	V/ns	Low Buffer Strength Refer to I^2C Control
t_{RISEH2}	Rise Time	Measured from 0.4V to 2.4V REFOUT and CLOCKOUT	0.4	1.0	ns	High Buffer Strength Refer to I^2C Control
t_{FALLH2}	Fall Time	Measured from 2.4V to 0.4V REFOUT and CLOCKOUT	0.4	1.0	ns	High Buffer Strength Refer to I^2C Control
t_{RISEL2}	Rise Time	Measured from 0.4V to 2.4V REFOUT and CLOCKOUT	0.5	1.5	ns	Low Buffer Strength Refer to I^2C Control
t_{FALLL2}	Fall Time	Measured from 2.4V to 0.4V REFOUT and CLOCKOUT	0.5	1.5	ns	Low Buffer Strength Refer to I^2C Control
T_{CYC1}	Cycle to Cycle Jitter	REFOUT	–	500	ps	SSCG is ON
T_{CYC2}	Cycle to Cycle Jitter	CLOCKOUT	–	250	ps	SSCG is ON
LTJ	10µS Period Jitter (100KHz, Frequency Modulation Amplitude)	Applies to REFOUT at all times and CLOCKOUT when SSCG is Off	–	2.0	ns	–
t_{START}	Start up time	From VDD = 2.0 V	–	3.0	ms	All outputs disabled

Table 8. Signal Loading Table

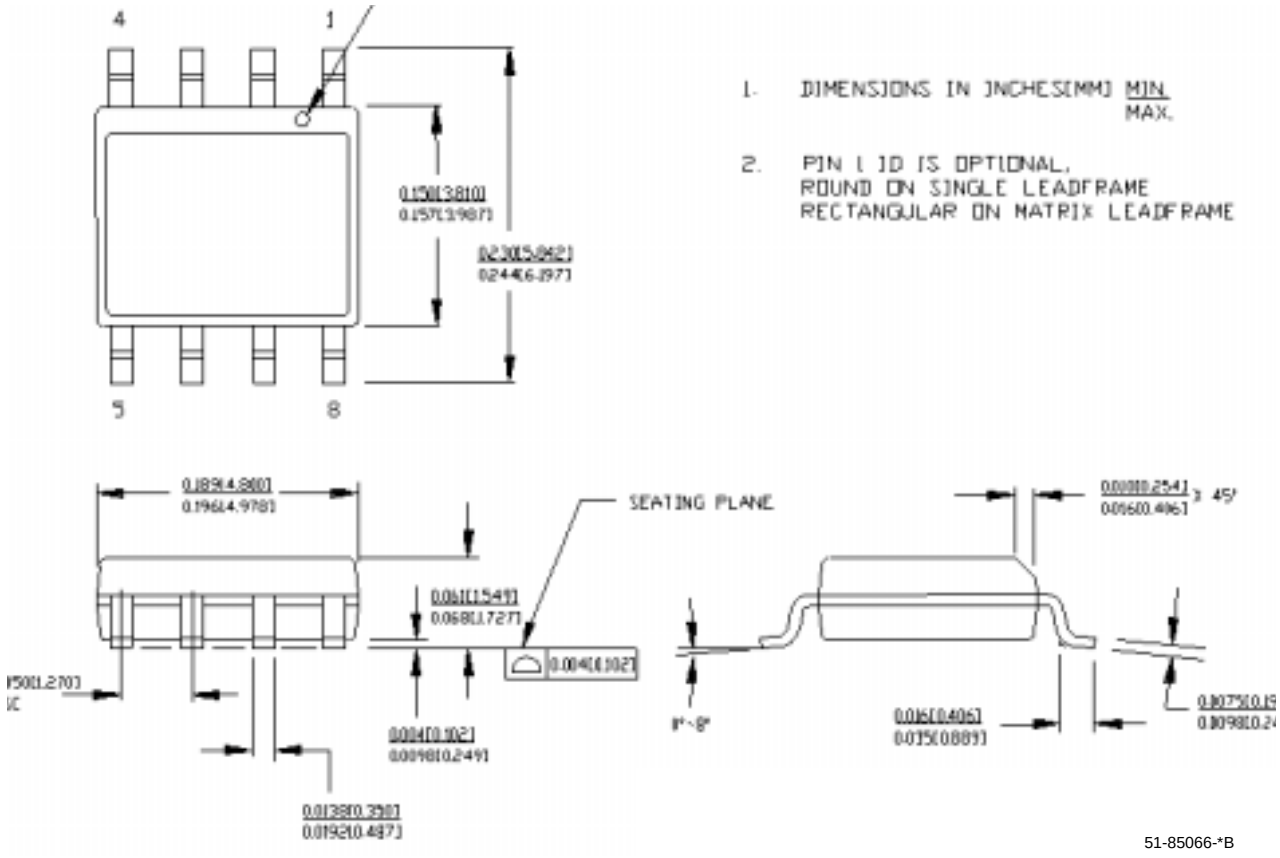
Clock Name	Max Load (pF)
CLKOUT, REFOUT	15

Ordering Information

Part Number	Package Type	Product Flow
CY25822SC–2	8-pin SOIC	Commercial, 0°C to 70°C
CY25822SC–2T	8-pin SOIC – Tape and Reel	Commercial, 0°C to 70°C

Package Diagram

8-lead (150-Mil) SOIC – S8



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Document History Page

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**	124462	03/19/03	RGL	New Data Sheet