

## 3.3V Zero Delay Buffer

### Features

- Zero input-output propagation delay, adjustable by capacitive load on FBK input
- Multiple configurations – see “Available Configurations” table
- Multiple low-skew outputs
  - Output-output skew less than 200 ps
  - Device-device skew less than 500 ps
- 10-MHz to 133-MHz operating range
- Low jitter, less than 200 ps cycle-cycle
- Space-saving 8-pin 150-mil SOIC package
- 3.3V operation
- Industrial temperature available

### Functional Description

The CY2304 is a 3.3V zero delay buffer designed to distribute high-speed clocks in PC, workstation, datacom, telecom, and other high-performance applications.

The part has an on-chip phase-locked loop (PLL) that locks to an input clock presented on the REF pin. The PLL feedback is required to be driven into the FBK pin, and can be obtained from one of the outputs. The input-to-output skew is guaranteed to be less than 250 ps, and output-to-output skew is guaranteed to be less than 200 ps.

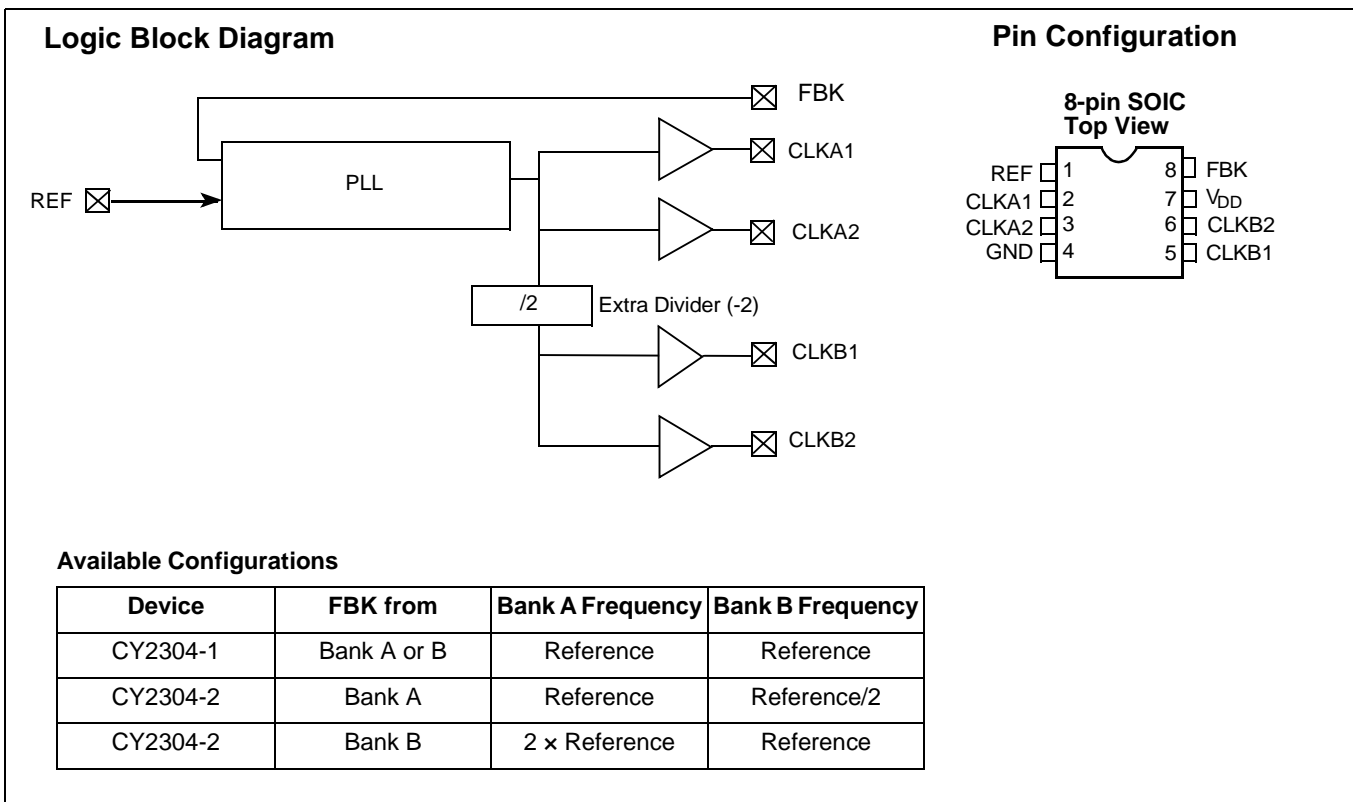
The CY2304 has two banks of two outputs each.

The CY2304 PLL enters a power-down state when there are no rising edges on the REF input. In this mode, all outputs are three-stated and the PLL is turned off, resulting in less than 25  $\mu$ A of current draw.

Multiple CY2304 devices can accept the same input clock and distribute it in a system. In this case, the skew between the outputs of two devices is guaranteed to be less than 500 ps.

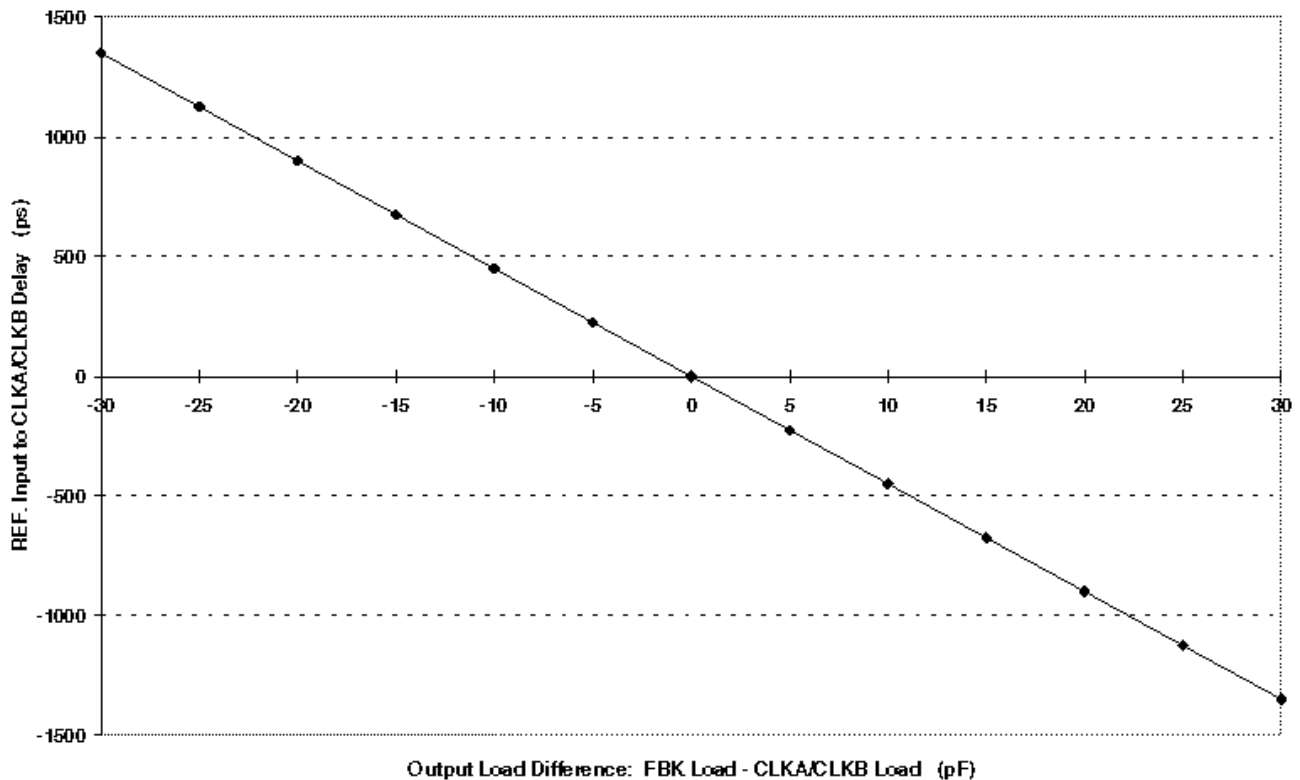
The CY2304 is available in two different configurations, as shown in the “Available Configurations” table. The CY2304–1 is the base part, where the output frequencies equal the reference if there is no counter in the feedback path.

The CY2304–2 allows the user to obtain Ref and 1/2x or 2x frequencies on each output bank. The exact configuration and output frequencies depends on which output drives the feedback pin.



**Pin Description**

Pin	Signal	Description
1	REF <sup>[1]</sup>	Input reference frequency, 5V-tolerant input
2	CLKA1 <sup>[2]</sup>	Clock output, Bank A
3	CLKA2 <sup>[2]</sup>	Clock output, Bank A
4	GND	Ground
5	CLKB1 <sup>[2]</sup>	Clock output, Bank B
6	CLKB2 <sup>[2]</sup>	Clock output, Bank B
7	V <sub>DD</sub>	3.3V supply
8	FBK	PLL feedback input

**Zero Delay and Skew Control**
**REF. Input to CLKA/CLKB Delay vs. Difference in Loading Between FBK Pin and CLKA/CLKB Pins**


To close the feedback loop of the CY2304, the FBK pin can be driven from any of the four available output pins. The output driving the FBK pin will be driving a total load of 7 pF plus any additional load that it drives. The relative loading of this output (with respect to the remaining outputs) can adjust the input-output delay. This is shown in the graph above.

For applications requiring zero input-output delay, all outputs including the one providing feedback should be equally

loaded. If input-output delay adjustments are required, use the above graph to calculate loading differences between the feedback output and remaining outputs.

For zero output-output skew, be sure to load outputs equally. For further information on using CY2304, refer to the application note "CY2308: Zero Delay Buffer."

**Notes:**

1. Weak pull-down.
2. Weak pull-down on all outputs.

**Maximum Ratings**

Supply Voltage to Ground Potential.....	-0.5V to +7.0V	Storage Temperature .....	-65°C to +150°C
DC Input Voltage (Except Ref) .....	-0.5V to $V_{DD} + 0.5V$	Junction Temperature .....	150°C
DC Input Voltage REF.....	-0.5 to 7V	Static Discharge Voltage (per MIL-STD-883, Method 3015).....	> 2000V

**Operating Conditions for CY2304SC-X Commercial Temperature Devices**

Parameter	Description	Min.	Max.	Unit
$V_{DD}$	Supply Voltage	3.0	3.6	V
$T_A$	Operating Temperature (Ambient Temperature)	0	70	°C
$C_L$	Load Capacitance (below 100 MHz)		30	pF
	Load Capacitance (from 100 MHz to 133 MHz)		15	pF
$C_{IN}$	Input Capacitance <sup>[3]</sup>		7	pF
$t_{PU}$	Power-up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

**Electrical Characteristics for CY2304SC-X Commercial Temperature Devices**

Parameter	Description	Test Conditions	Min.	Max.	Unit
$V_{IL}$	Input LOW Voltage			0.8	V
$V_{IH}$	Input HIGH Voltage		2.0		V
$I_{IL}$	Input LOW Current	$V_{IN} = 0V$		50.0	μA
$I_{IH}$	Input HIGH Current	$V_{IN} = V_{DD}$		100.0	μA
$V_{OL}$	Output LOW Voltage <sup>[4]</sup>	$I_{OL} = 8\text{ mA} (-1, -2)$		0.4	V
$V_{OH}$	Output HIGH Voltage <sup>[4]</sup>	$I_{OH} = -8\text{ mA} (-1, -2)$	2.4		V
$I_{DD}$ (PD mode)	Power-down Supply Current	REF = 0 MHz		12.0	μA
$I_{DD}$	Supply Current	Unloaded outputs, 100-MHz REF, Select inputs at $V_{DD}$ or GND		45.0	mA
		Unloaded outputs, 66-MHz REF (-1,-2)		32.0	mA
		Unloaded outputs, 33-MHz REF (-1,-2)		18.0	mA

**Switching Characteristics for CY2304SC-X Commercial Temperature Devices<sup>[5]</sup>**

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
$t_1$	Output Frequency	30-pF load, all devices	10		100	MHz
$t_1$	Output Frequency	15-pF load, -1, -2 devices	10		133.3	MHz
	Duty Cycle <sup>[4]</sup> = $t_2 \div t_1$ (-1,-2)	Measured at 1.4V, $F_{OUT} = 66.66\text{ MHz}$ 30-pF load	40.0	50.0	60.0	%
	Duty Cycle <sup>[4]</sup> = $t_2 \div t_1$ (-1,-2)	Measured at 1.4V, $F_{OUT} < 50.0\text{ MHz}$ 15-pF load	45.0	50.0	55.0	%
$t_3$	Rise Time <sup>[4]</sup> (-1, -2)	Measured between 0.8V and 2.0V, 30-pF load			2.20	ns
$t_3$	Rise Time <sup>[4]</sup> (-1, -2)	Measured between 0.8V and 2.0V, 15-pF load			1.50	ns

**Notes:**

3. Applies to both REF clock and FBK.
4. Parameter is guaranteed by design and characterization. Not 100% tested in production.
5. All parameters are specified with loaded output.

**Switching Characteristics for CY2304SC-X Commercial Temperature Devices (continued)<sup>[5]</sup>**

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
t <sub>4</sub>	Fall Time <sup>[4]</sup> (-1, -2)	Measured between 0.8V and 2.0V, 30-pF load			2.20	ns
t <sub>4</sub>	Fall Time <sup>[4]</sup> (-1, -2)	Measured between 0.8V and 2.0V, 15-pF load			1.50	ns
t <sub>5</sub>	Output-to-Output Skew on same Bank (-1,-2) <sup>[4]</sup>	All outputs equally loaded			200	ps
	Output Bank A to Output Bank B Skew (-1)	All outputs equally loaded			200	ps
	Output Bank A to Output Bank B Skew (-2)	All outputs equally loaded			400	ps
t <sub>6</sub>	Skew, REF Rising Edge to FBK Rising Edge <sup>[4]</sup>	Measured at V <sub>DD</sub> /2		0	±250	ps
t <sub>7</sub>	Device-to-Device Skew <sup>[4]</sup>	Measured at V <sub>DD</sub> /2 on the FBK pins of devices		0	500	ps
t <sub>J</sub>	Cycle-to-Cycle Jitter <sup>[4]</sup> (-1)	Measured at 66.67 MHz, loaded outputs, 15-pF load			175	ps
		Measured at 66.67 MHz, loaded outputs, 30-pF load			200	ps
		Measured at 133.3 MHz, loaded outputs, 15 pF load			100	ps
t <sub>J</sub>	Cycle-to-Cycle Jitter <sup>[4]</sup> (-2)	Measured at 66.67 MHz, loaded outputs 30-pF load			400	ps
		Measured at 66.67 MHz, loaded outputs 15-pF load			375	ps
t <sub>LOCK</sub>	PLL Lock Time <sup>[4]</sup>	Stable power supply, valid clocks presented on REF and FBK pins			1.0	ms

**Operating Conditions for CY2304SI-X Industrial Temperature Devices**

Parameter	Description	Min.	Max.	Unit
V <sub>DD</sub>	Supply Voltage	3.0	3.6	V
T <sub>A</sub>	Operating Temperature (Ambient Temperature)	-40	85	°C
C <sub>L</sub>	Load Capacitance (below 100 MHz)		30	pF
	Load Capacitance (from 100 MHz to 133 MHz)		15	pF
C <sub>IN</sub>	Input Capacitance		7	pF

**Switching Characteristics for CY2304SI-X Industrial Temperature Devices <sup>[5]</sup>**

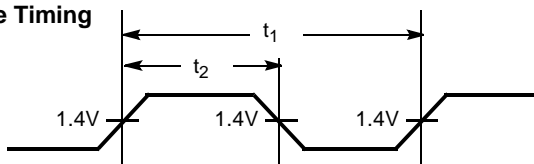
Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
t <sub>1</sub>	Output Frequency	30-pF load, All devices	10		100	MHz
t <sub>1</sub>	Output Frequency	15-pF load, All devices	10		133.3	MHz
	Duty Cycle <sup>[4]</sup> = t <sub>2</sub> ÷ t <sub>1</sub> (-1,-2)	Measured at 1.4V, F <sub>OUT</sub> = 66.66 MHz 30-pF load	40.0	50.0	60.0	%
	Duty Cycle <sup>[4]</sup> = t <sub>2</sub> ÷ t <sub>1</sub> (-1,-2)	Measured at 1.4V, F <sub>OUT</sub> < 50.0 MHz 15-pF load	45.0	50.0	55.0	%
t <sub>3</sub>	Rise Time <sup>[4]</sup> (-1, -2)	Measured between 0.8V and 2.0V, 30-pF load			2.50	ns
t <sub>3</sub>	Rise Time <sup>[4]</sup> (-1, -2)	Measured between 0.8V and 2.0V, 15-pF load			1.50	ns
t <sub>4</sub>	Fall Time <sup>[4]</sup> (-1, -2)	Measured between 0.8V and 2.0V, 30-pF load			2.50	ns
t <sub>4</sub>	Fall Time <sup>[4]</sup> (-1, -2)	Measured between 0.8V and 2.0V, 15-pF load			1.50	ns

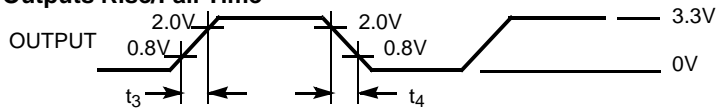
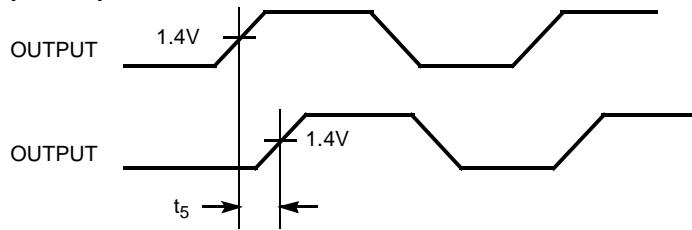
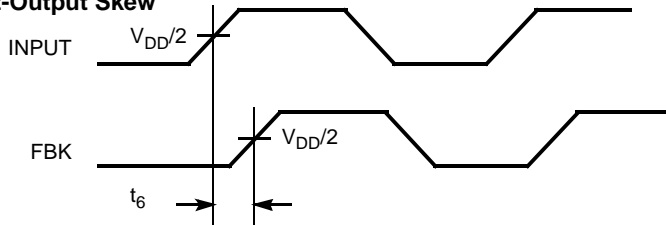
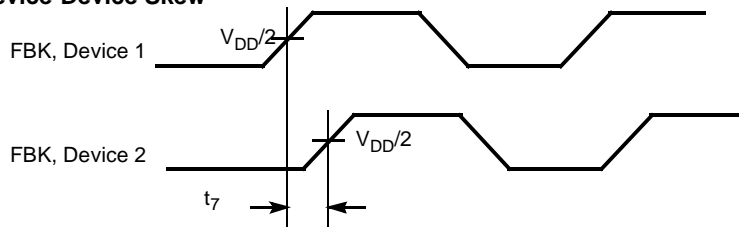
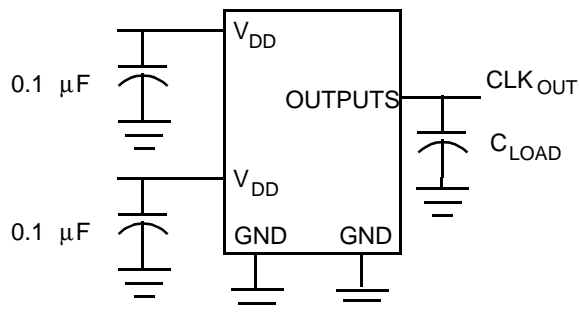
**Switching Characteristics for CY2304SI-X Industrial Temperature Devices** (continued)<sup>[5]</sup>

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
t <sub>5</sub>	Output-to-Output Skew on same Bank (-1,-2) <sup>[4]</sup>	All outputs equally loaded			200	ps
	Output Bank A to Output Bank B Skew (-1)	All outputs equally loaded			200	ps
	Output Bank A to Output Bank B Skew (-2)	All outputs equally loaded			400	ps
t <sub>6</sub>	Skew, REF Rising Edge to FBK Rising Edge <sup>[4]</sup>	Measured at V <sub>DD</sub> /2		0	±250	ps
t <sub>7</sub>	Device-to-Device Skew <sup>[4]</sup>	Measured at V <sub>DD</sub> /2 on the FBK pins of devices		0	500	ps
t <sub>J</sub>	Cycle-to-Cycle Jitter <sup>[4]</sup> (-1)	Measured at 66.67 MHz, loaded outputs, 15-pF load			180	ps
		Measured at 66.67 MHz, loaded outputs, 30-pF load			200	ps
		Measured at 133.3 MHz, loaded outputs, 15 pF load			100	ps
t <sub>J</sub>	Cycle-to-Cycle Jitter <sup>[4]</sup> (-2)	Measured at 66.67 MHz, loaded outputs, 30-pF load			400	ps
		Measured at 66.67 MHz, loaded outputs, 15-pF load			380	ps
t <sub>LOCK</sub>	PLL Lock Time <sup>[4]</sup>	Stable power supply, valid clocks presented on REF and FBK pins			1.0	ms

**Electrical Characteristics for CY2304SI-X Industrial Temperature Devices**

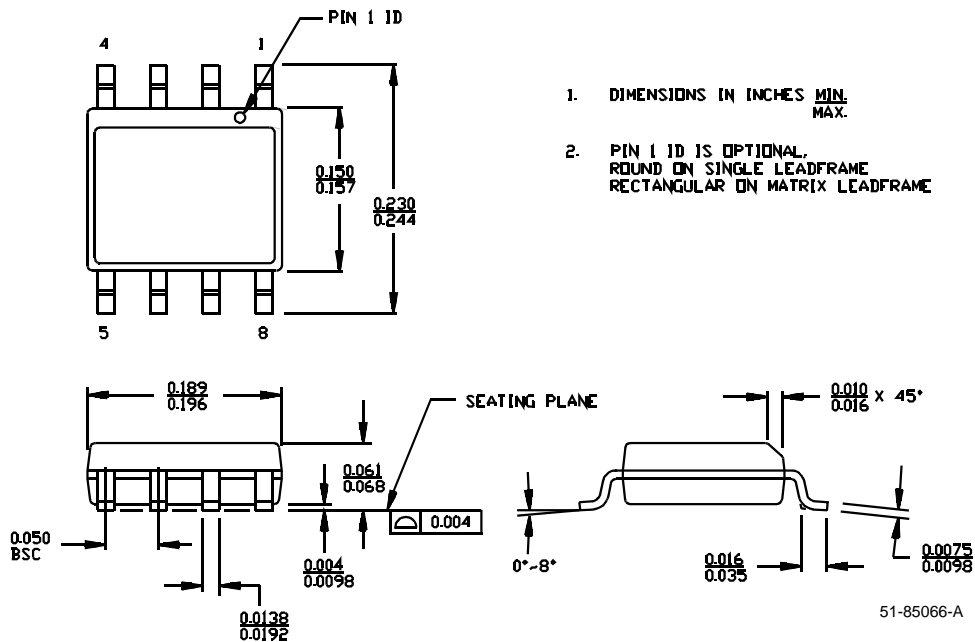
Parameter	Description	Test Conditions	Min.	Max.	Unit
V <sub>IL</sub>	Input LOW Voltage			0.8	V
V <sub>IH</sub>	Input HIGH Voltage		2.0		V
I <sub>IL</sub>	Input LOW Current	V <sub>IN</sub> = 0V		50.0	μA
I <sub>IH</sub>	Input HIGH Current	V <sub>IN</sub> = V <sub>DD</sub>		100.0	μA
V <sub>OL</sub>	Output LOW Voltage <sup>[4]</sup>	I <sub>OL</sub> = 8 mA (-1, -2)		0.4	V
V <sub>OH</sub>	Output HIGH Voltage <sup>[4]</sup>	I <sub>OH</sub> = -8 mA (-1, -2)	2.4		V
I <sub>DD</sub> (PD mode)	Power-down Supply Current	REF = 0 MHz		25.0	μA
I <sub>DD</sub>	Supply Current	Unloaded outputs, 100 MHz, Select inputs at V <sub>DD</sub> or GND		45.0	mA
		Unloaded outputs, 66-MHz REF (-1, -2)		35.0	mA
		Unloaded outputs, 33-MHz REF (-1, -2)		20.0	mA

**Switching Waveforms**
**Duty Cycle Timing**


**Switching Waveforms**
**All Outputs Rise/Fall Time**

**Output-Output Skew**

**Input-Output Skew**

**Device-Device Skew**

**Test Circuits**
**Test Circuit # 1**

 Test circuit for all parameters except  $t_8$

**Ordering Information**

Ordering Code	Package Name	Package Type	Operating Range
CY2304SC-1	S8	8-pin 150-mil SOIC	Commercial
CY2304SI-1	S8	8-pin 150-mil SOIC	Industrial
CY2304SC-2	S8	8-pin 150-mil SOIC	Commercial
CY2304SI-2	S8	8-pin 150-mil SOIC	Industrial

**Package Diagram**
**8-lead (150-Mil) SOIC S8**


Document Title: CY2304 3.3V Zero Delay Buffer  
Document Number: 38-07247

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	110512	12/11/01	SZV	Change from Spec number: 38-01010 to 38-07247
*A	112294	03/04/02	CKN	On Pin Configuration Diagram (p.1), swapped CLKA2 and CLKA1
*B	113934	05/01/02	CKN	Added Operating Conditions for CY2304SI-X Industrial Temperature Devices, p. 4
*C	121851	12/14/02	RBI	Power up requirements added to Operating Conditions Information