

MOS FIELD EFFECT TRANSISTOR **μ PA1730**

SWITCHING P-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The μ PA1730 is P-Channel MOS Field Effect Transistor designed for power management applications of notebook computers and Li-ion battery protection circuit.

FEATURES

Low on-resistance

 $R_{DS(on)1} = 9.5 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = -10 \text{ V, ID} = -6.5 \text{ A)}$

 $R_{DS(on)2} = 13.5 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = -4.5 \text{ V, Ip} = -6.5 \text{ A)}$

- RDS(on)3 = 15.0 m Ω MAX. (VGS = -4.0 V, ID = -6.5 A)
 - Low Ciss: Ciss = 3800 pF TYP.
 - · Built-in G-S protection diode
 - Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit: mm) ; Source 1,2,3 Gate 5,6,7,8 ; Drain 日月日日 6.0 ±0.3 4.4 5.37 MAX 0.8 Z □ 0.10 1.27 0.78 MAX 0.05

0.40 ^{+0.10}/_{-0.05} \oplus 0.12 M

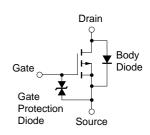
ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1730G	Power SOP8

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

VDSS	-30	V
Vgss	∓ 20	V
ID(DC)	∓ 13.0	Α
D(pulse)	∓ 52.0	Α
PT	2.2	W
Tch	150	°C
Tstg	-55 to +150	°C
	VGSS ID(DC) ID(pulse) PT Tch	VGSS \mp 20 ID(DC) \mp 13.0 ID(pulse) \mp 52.0 PT 2.2 Tch 150

EQUIVALENT CIRCUIT



Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1 %

2. Mounted on ceramic substrate of 1200 mm² x 2.2 mm

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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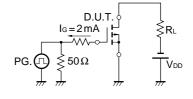


ELECTRICAL CHARACTERISTICS (T_A = 25 °C, All terminals are connected.)

	CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Drain to Source On-state Resistance	RDS(on)1	Vgs = -10 V, ID = -6.5 A		7.6	9.5	mΩ
		RDS(on)2	$V_{GS} = -4.5 \text{ V}, I_{D} = -6.5 \text{ A}$		10.3	13.5	mΩ
*		RDS(on)3	$V_{GS} = -4.0 \text{ V}, I_{D} = -6.5 \text{ A}$		11.3	15.0	mΩ
	Gate to Source Cut-off Voltage	V _{GS(off)}	$V_{DS} = -10 \text{ V}, I_{D} = -1 \text{ mA}$	-1.0	-1.6	-2.5	V
	Forward Transfer Admittance	y fs	$V_{DS} = -10 \text{ V}, I_{D} = -6.5 \text{ A}$	11.0	23.0		S
*	Drain Leakage Current	Ipss	V _{DS} = -30 V, V _{GS} = 0 V			-1	μΑ
	Gate to Source Leakage Current	Igss	$V_{GS} = \mp 20 \text{ V}, V_{DS} = 0 \text{ V}$			∓ 10	μΑ
	Input Capacitance	Ciss	V _{DS} = -10 V		3800		pF
	Output Capacitance	Coss	Vgs = 0 V		1200		pF
	Reverse Transfer Capacitance	Crss	f = 1 MHz		500		pF
	Turn-on Delay Time	td(on)	ID = -6.5 A		40		ns
	Rise Time	tr	VGS(on) = -10 V		240		ns
	Turn-off Delay Time	td(off)	V _{DD} = -15 V		230		ns
	Fall Time	t f	R _G = 10 Ω		160		ns
	Total Gate Charge	Q _G	I _D = -13.0 A		70		nC
	Gate to Source Charge	Qgs	V _{DD} = -24 V		9		nC
	Gate to Drain Charge	Q _{GD}	Vgs = -10 V		17		nC
	Body Diode Forward Voltage	VF(S-D)	IF = 13 A, VGS = 0 V		0.80		V
	Reverse Recovery Time	trr	IF = 13 A, VGS = 0 V		53		ns
	Reverse Recovery Charge	Qrr	$di/dt = 100 \text{ A}/\mu\text{s}$		57		nC

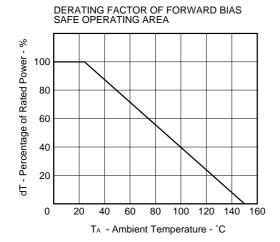
TEST CIRCUIT 1 SWITCHING TIME

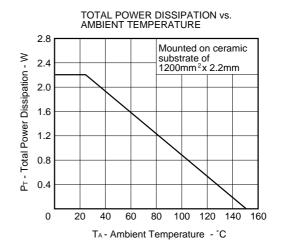
TEST CIRCUIT 2 GATE CHARGE





★ TYPICAL CHARACTERISTICS (TA = 25 °C)





FORWARD BIAS SAFE OPERATING AREA

-100

-100

-100

-100

-100

-100

-100

-100

-100

-100

-100

-100

-100

-100

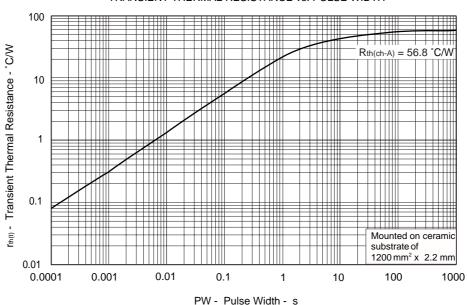
-100

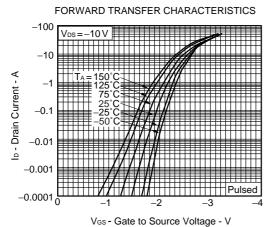
-100

V_{DS} - Drain to Source Voltage - V

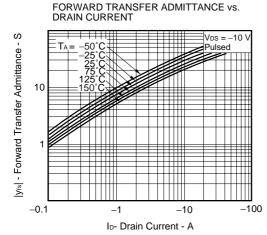
Remark Mounted on ceramic substrate of 1200 mm² x 2.2 mm

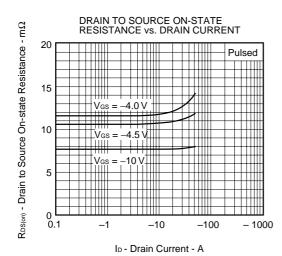
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



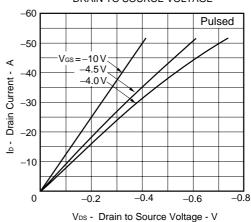


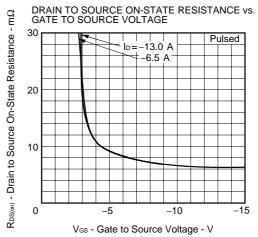




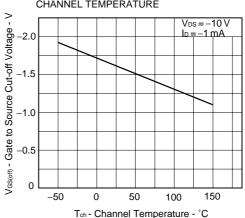


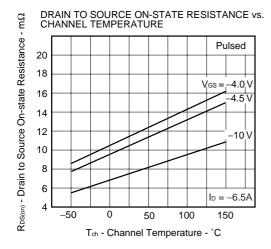
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

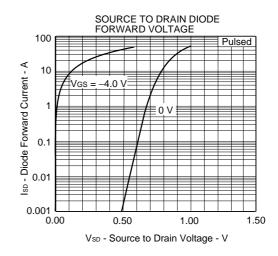


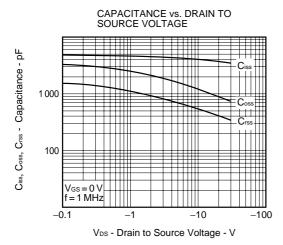


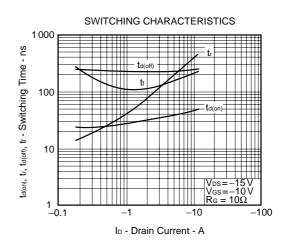
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE

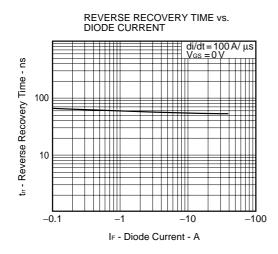


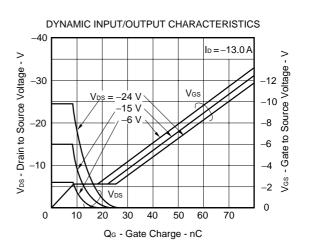












NEC μ PA1730

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