

SGM721 SGM722 SGM723 SGM724

970 μ A, 10MHz, Rail-to-Rail I/O CMOS Operational Amplifier

PRODUCT DESCRIPTION

The SGM721 (single), SGM722 (dual), SGM723 (single with shutdown) and SGM724 (quad) are low noise, low voltage, and low power operational amplifiers, that can be designed into a wide range of applications. The SGM721/2/3/4 have a high Gain-Bandwidth Product of 10MHz, a slew rate of 8.5V/ μ s, and a quiescent current of 0.97mA/amplifier at 5V. The SGM723 has a power-down disable feature that reduces the supply current to 160nA.

The SGM721/2/3/4 are designed to provide optimal performance in low voltage and low noise systems. They provide rail-to-rail output swing into heavy loads. The input common-mode voltage range includes ground, and the maximum input offset voltage is 4mV for SGM721/2/3/4. They are specified over the extended industrial temperature range (-40°C to +125°C). The operating range is from 2.5V to 5.5V.

The single version, SGM721 is available in SC70-5, SOT23-5 and SO-8 packages. SGM723 is available in SOT23-6 and SO-8 packages. The dual version SGM722 is available in SO-8 and MSOP-8 packages. The quad version SGM724 is available in TSSOP-16 and SO-16 packages.

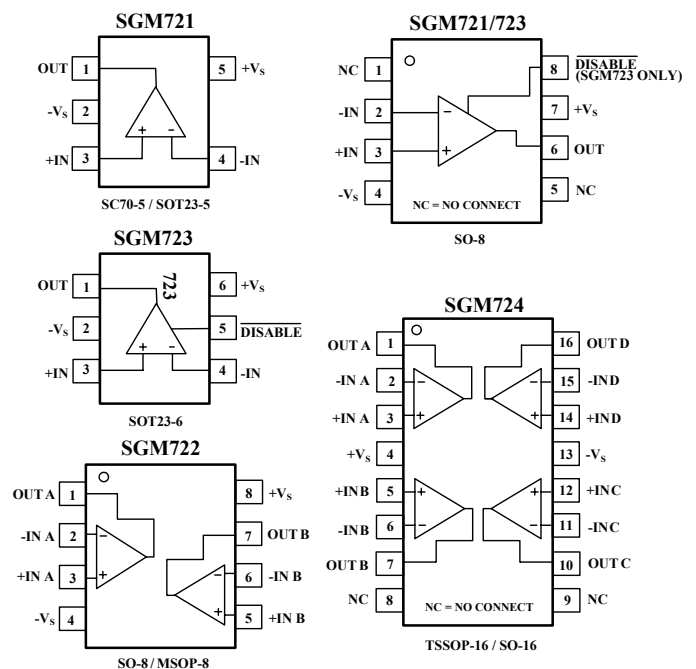
APPLICATIONS

Sensors
Audio
Active Filters
A/D Converters
Communications
Test Equipment
Cellular and Cordless Phones
Laptops and PDAs
Photodiode Amplification
Battery-Powered Instrumentation

FEATURES

- Low Cost
- Rail-to-Rail Input and Output
1mV Typical V_{os}
- High Gain-Bandwidth Product: 10MHz
- High Slew Rate: 8.5V/ μ s
- Settling Time to 0.1% with 2V Step: 0.36 μ s
- Overload Recovery Time: 0.4 μ s
- Low Noise : 8 nV/ \sqrt{Hz}
- Operates on 2.5 V to 5.5V Supplies
- Input Voltage Range = - 0.1 V to +5.6 V with $V_s = 5.5$ V
- Low Power
0.97 mA/Amplifier Typical Supply Current
SGM723 160nA when Disabled
- Small Packaging
SGM721 Available in SC70-5, SOT23-5 and SO-8
SGM722 Available in MSOP-8 and SO-8
SGM723 Available in SOT23-6 and SO-8
SGM724 Available in TSSOP-16 and SO-16

PIN CONFIGURATIONS (Top View)



ELECTRICAL CHARACTERISTICS : $V_S = +5V$

(At $T_A = +25^\circ C$, $V_{CM} = V_S/2$, $R_L = 600\Omega$, unless otherwise noted)

PARAMETER	CONDITION	SGM721/2/3/4							
		TYP	MIN/MAX OVER TEMPERATURE					UNITS	MIN/ MAX
		+25°C	+25°C	0°C to 70°C	-40°C to 85°C	-40°C to 125°C			
INPUT CHARACTERISTICS									
Input Offset Voltage (V_{OS})		1	4	4.5	4.75	5	mV	MAX	
Input Bias Current (I_b)		1					pA	TYP	
Input Offset Current (I_{OS})		1					pA	TYP	
Common-Mode Voltage Range (V_{CM})	$V_S = 5.5V$	-0.1 to +5.6					V	TYP	
Common-Mode Rejection Ratio (CMRR)	$V_S = 5.5V, V_{CM} = -0.1V$ to 4 V	91	75	74	73	72.5	dB	MIN	
	$V_S = 5.5V, V_{CM} = -0.1V$ to 5.6 V	86	64	64	63	62	dB	MIN	
Open-Loop Voltage Gain (A_{OL})	$R_L = 600\Omega, V_O = 0.15V$ to 4.85V	90	84	81	80	72	dB	MIN	
	$R_L = 10K\Omega, V_O = 0.05V$ to 4.95V	100	95	90	88	77	dB	MIN	
Input Offset Voltage Drift ($\Delta V_{OS}/\Delta T$)		2.1					$\mu V/^\circ C$	TYP	
OUTPUT CHARACTERISTICS									
Output Voltage Swing from Rail	$R_L = 600\Omega$	0.1					V	TYP	
	$R_L = 10K\Omega$	0.015					V	TYP	
Output Current (I_{OUT})		57	53	52	50	45	mA	MIN	
Closed-Loop Output Impedance	$F = 1MHz, G = +1$	5.7					Ω	TYP	
POWER-DOWN DISABLE									
Turn-On Time		2.2					μs	TYP	
Turn-Off Time		0.8					μs	TYP	
$\overline{DISABLE}$ Voltage-Off			0.8				V	MAX	
$\overline{DISABLE}$ Voltage-On			2				V	MIN	
POWER SUPPLY									
Operating Voltage Range			2.5	2.5	2.5	2.5	V	MIN	
			5.5	5.5	5.5	5.5	V	MAX	
Power Supply Rejection Ratio (PSRR)	$V_S = +2.5V$ to + 5.5 V								
	$V_{CM} = (-V_S) + 0.5V$	100	80	79	78	77	dB	MIN	
Quiescent Current/ Amplifier (I_Q)	$I_{OUT} = 0$	0.97	1.13	1.25	1.28	1.38	mA	MAX	
Supply Current when Disabled (SGM723 only)		0.16	1				μA	MAX	
DYNAMIC PERFORMANCE									
Gain-Bandwidth Product (GBP)	$R_L = 600\Omega$	10					MHz	TYP	
Phase Margin (ϕ_O)		63.5					degrees	TYP	
Full Power Bandwidth (BW_P)	< 1% distortion	400					KHz	TYP	
Slew Rate (SR)	$G = +1, 2V$ Output Step	8.5					V/ μs	TYP	
Settling Time to 0.1% (t_s)	$G = +1, 2V$ Output Step	0.36					μs	TYP	
Overload Recovery Time	$V_{IN} \cdot Gain = V_S$	0.4					μs	TYP	
NOISE PERFORMANCE									
Voltage Noise Density (e_n)	$f = 1kHz$	8					nV/\sqrt{Hz}	TYP	
	$f = 10kHz$	6.4					nV/\sqrt{Hz}	TYP	
Current Noise Density (i_n)	$f = 1kHz$	10					fA/\sqrt{Hz}	TYP	

Specifications subject to change without notice.

PACKAGE/ORDERING INFORMATION

MODEL	ORDER NUMBER	PACKAGE DESCRIPTION	PACKAGE OPTION	MARKING INFORMATION
SGM721	SGM721XC5/TR	SC70-5	Tape and Reel, 3000	721
	SGM721XN5/TR	SOT23-5	Tape and Reel, 3000	721
	SGM721XS/TR	SO-8	Tape and Reel, 2500	SGM721XS
SGM722	SGM722XMS/TR	MSOP-8	Tape and Reel, 3000	SGM722XMS
	SGM722XS/TR	SO-8	Tape and Reel, 2500	SGM722XS
SGM723	SGM723XN6/TR	SOT23-6	Tape and Reel, 3000	723
	SGM723XS/TR	SO-8	Tape and Reel, 2500	SGM723XS
SGM724	SGM724XS/TR	SO-16	Tape and Reel, 2500	SGM724XS
	SGM724XTS	TSSOP-16	Tape and Reel, 3000	SGM724XTS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+ to V-	7.5 V
Common-Mode Input Voltage	(-V _S) - 0.5 V to (+V _S) +0.5V
Storage Temperature Range	-65°C to +150°C
Junction Temperature	160°C
Operating Temperature Range	-55°C to +150°C
Package Thermal Resistance @ T _A = 25°C	
SC70-5, θ _{JA}	333°C/W
SOT23-5, θ _{JA}	190°C/W
SOT23-6, θ _{JA}	190°C/W
SO-8, θ _{JA}	125°C/W
MSOP-8, θ _{JA}	216°C/W
SO-16, θ _{JA}	82°C/W
TSSOP-16, θ _{JA}	105°C/W
Lead Temperature Range (Soldering 10 sec)	260°C
ESD Susceptibility	
HBM	1500V
MM	400V

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

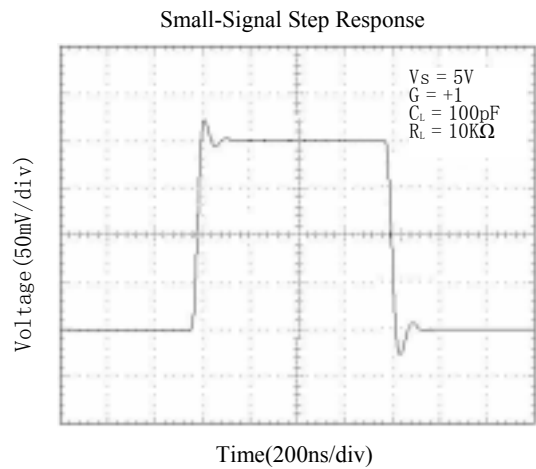
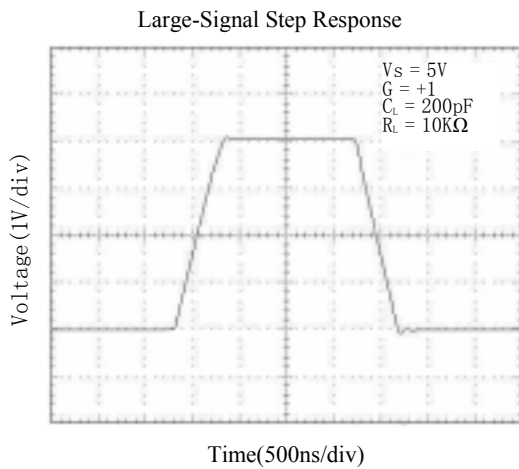
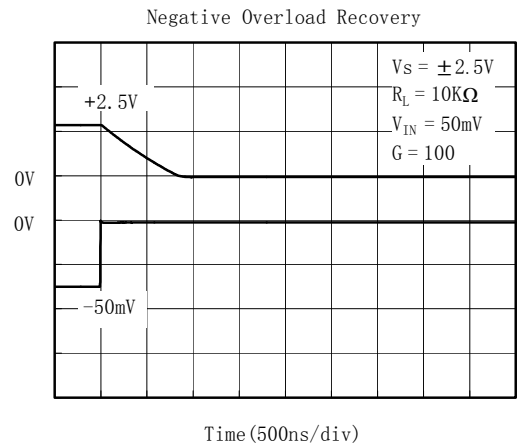
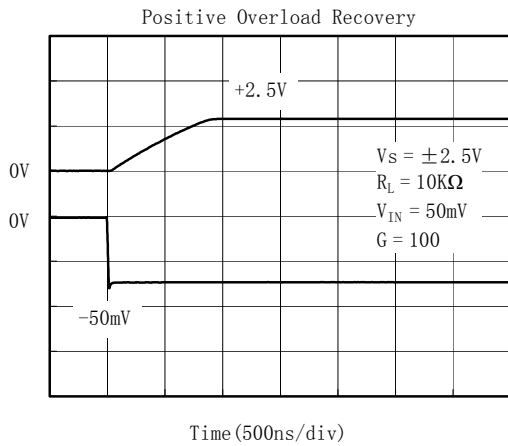
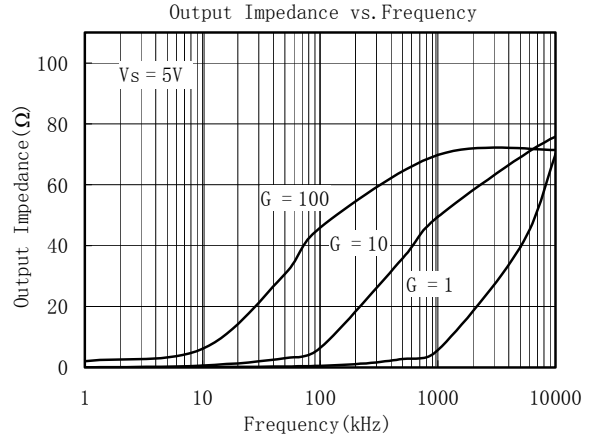
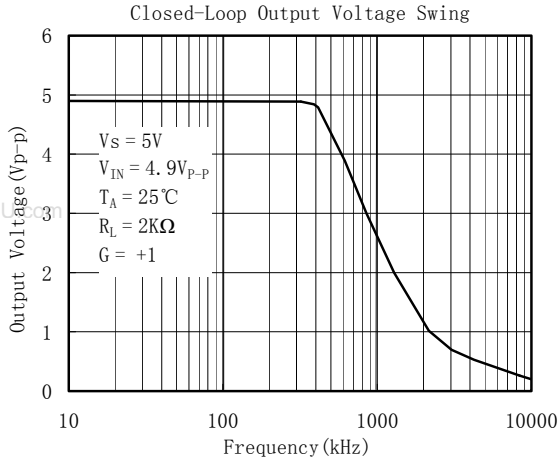
CAUTION

This integrated circuit can be damaged by ESD. Shengbang Micro-electronics recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

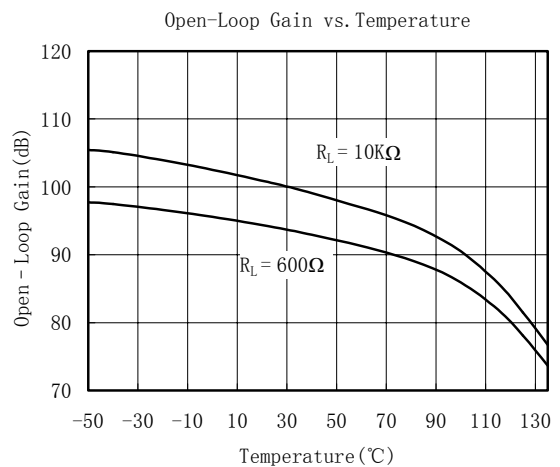
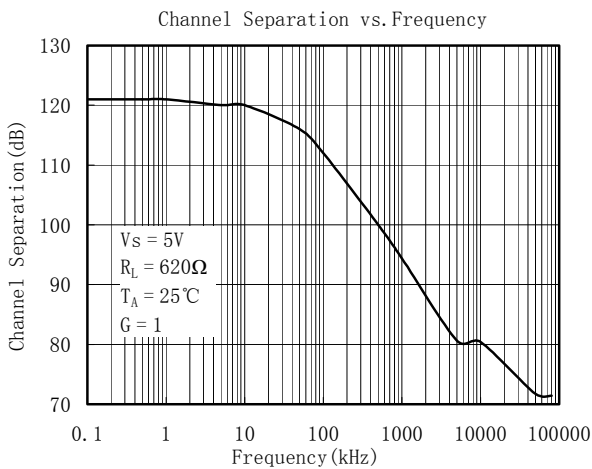
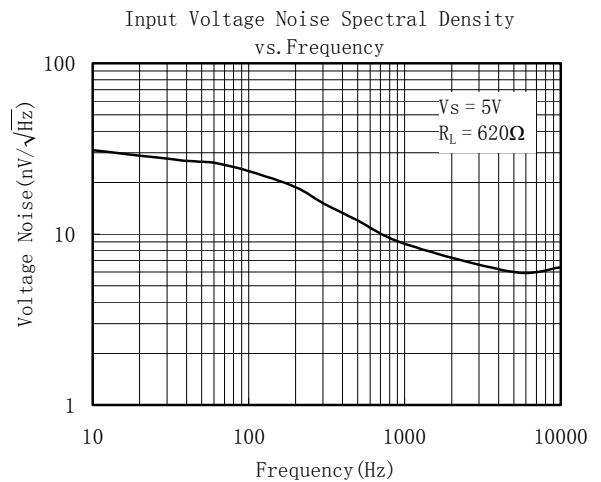
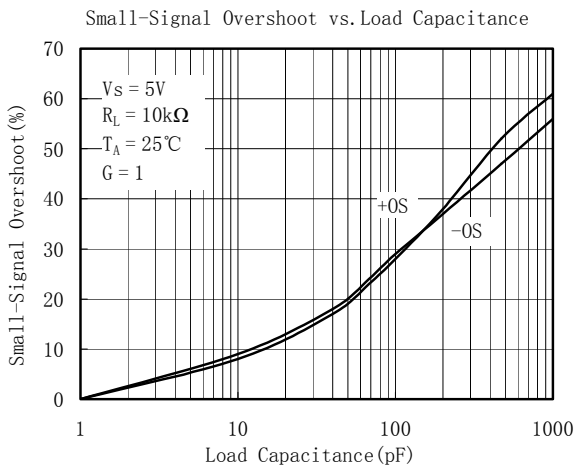
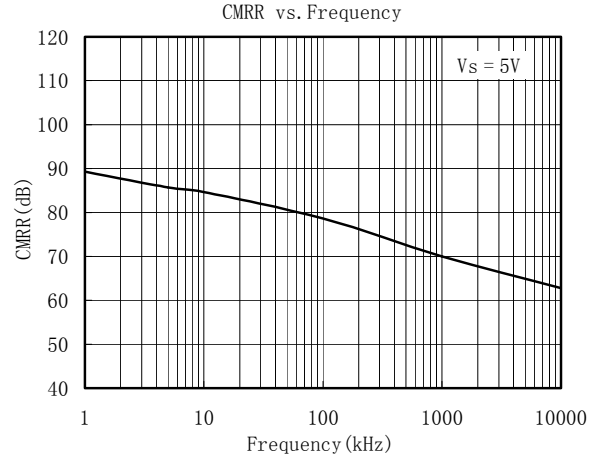
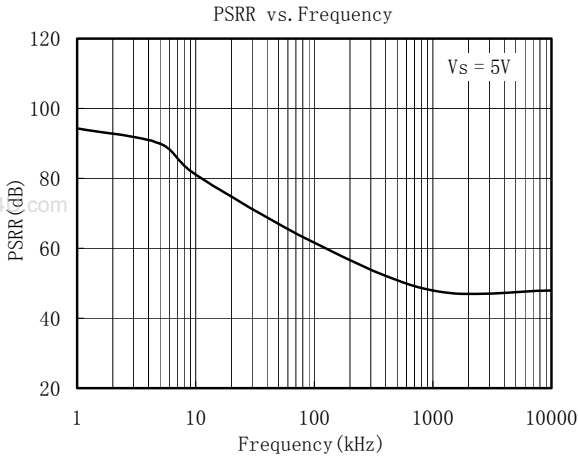
TYPICAL PERFORMANCE CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_{CM} = V_S/2$, $R_L = 600\Omega$, unless otherwise noted.



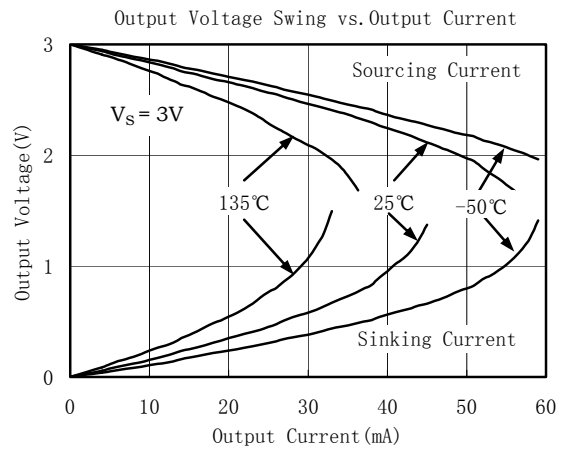
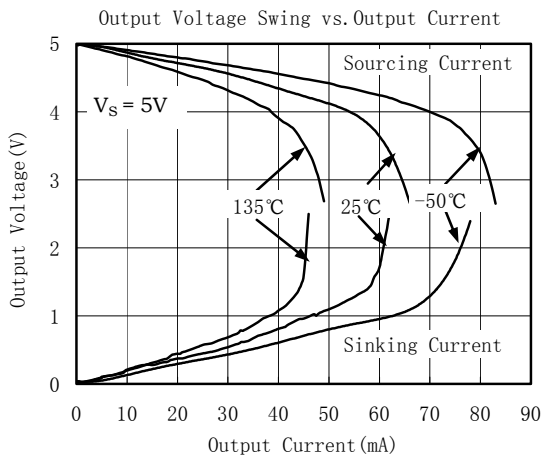
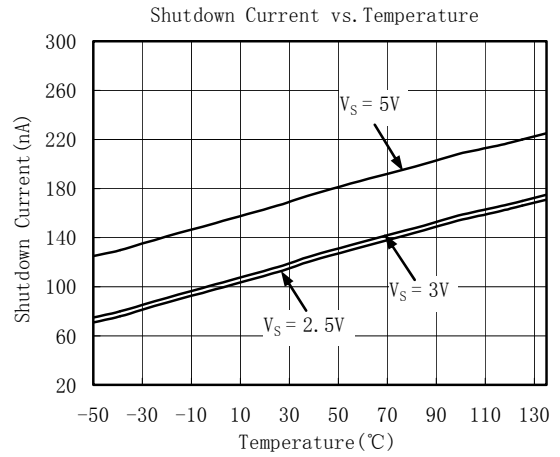
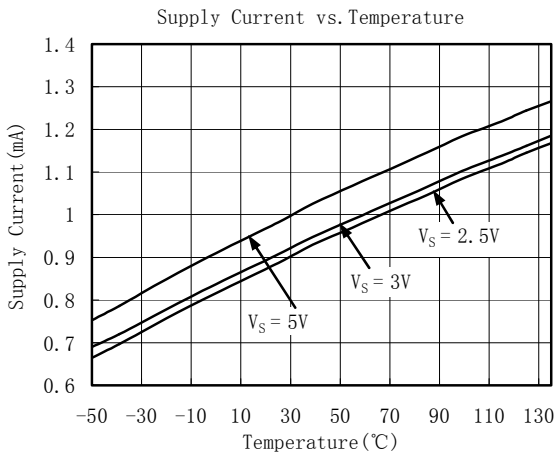
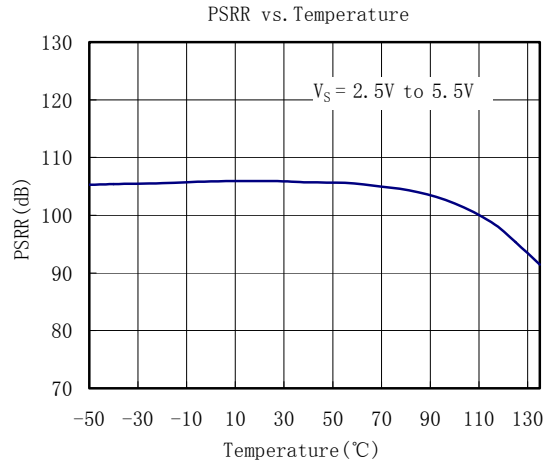
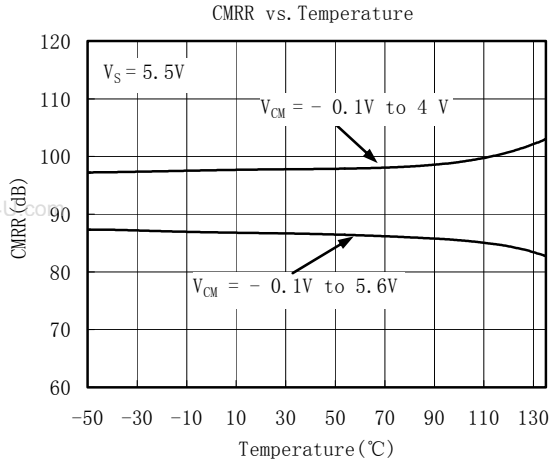
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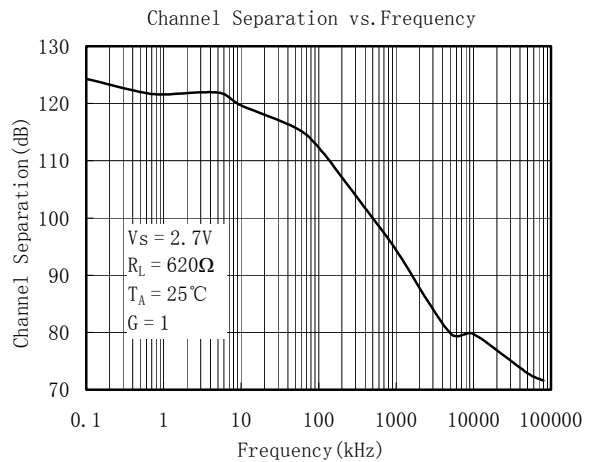
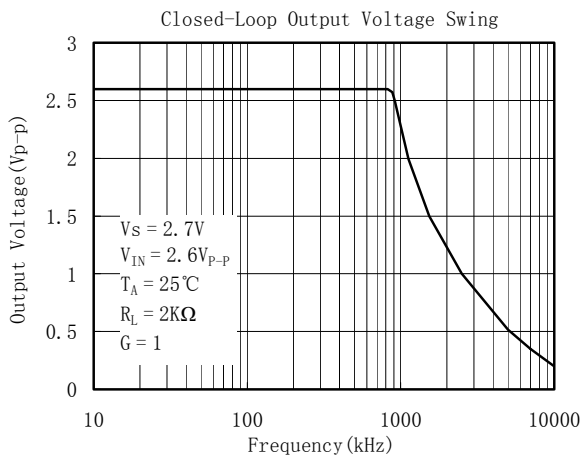
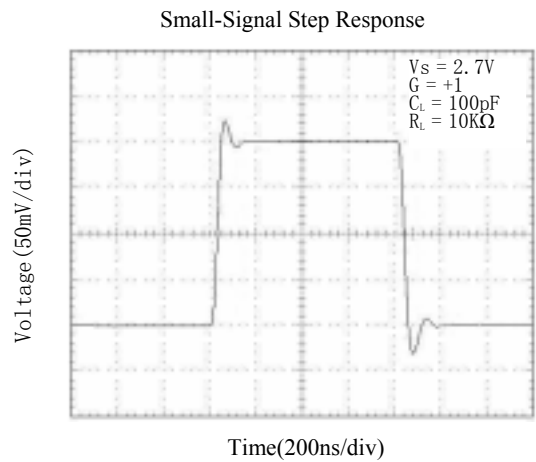
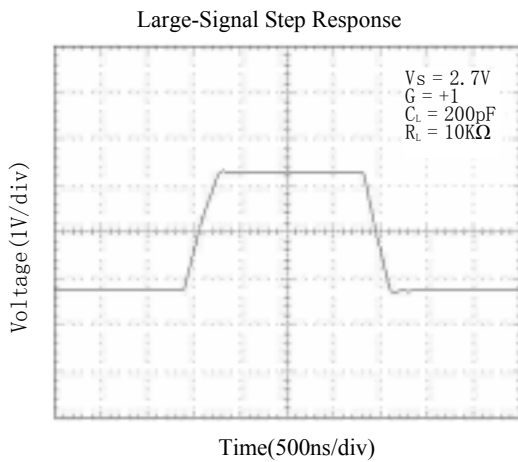
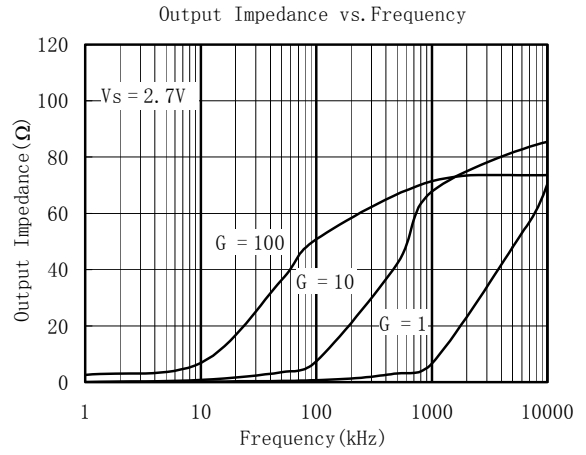
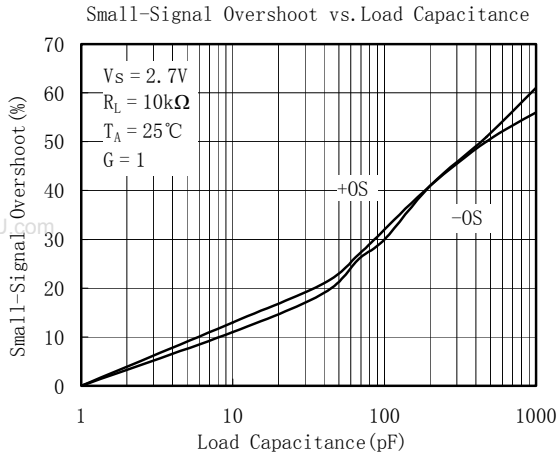
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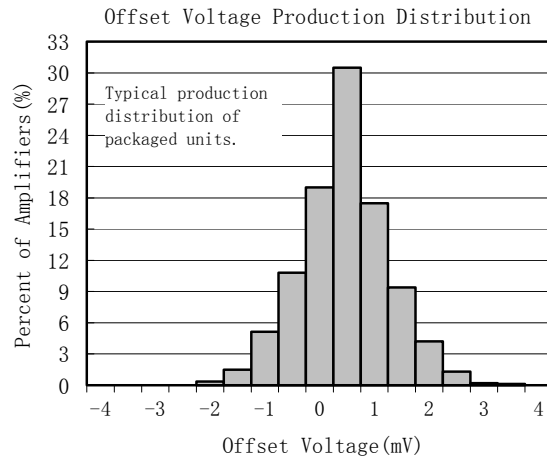
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At $T_A = +25^\circ\text{C}$, $V_{CM} = V_S/2$, $R_L = 600\Omega$, unless otherwise noted.



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APPLICATION NOTES

Driving Capacitive Loads

The SGM72x can directly drive 4700pF in unity-gain without oscillation. The unity-gain follower (buffer) is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers and this results in ringing or even oscillation. Applications that require greater capacitive drive capability should use an isolation resistor between the output and the capacitive load like the circuit in Figure 1. The isolation resistor R_{ISO} and the load capacitor C_L form a zero to increase stability. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Note that this method results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_{LOAD} .

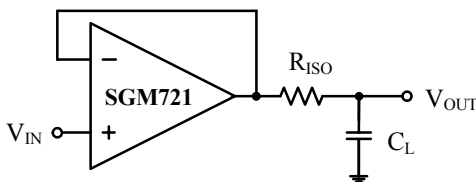


Figure 1. Indirectly Driving Heavy Capacitive Load

An improvement circuit is shown in Figure 2. It provides DC accuracy as well as AC stability. R_F provides the DC accuracy by connecting the inverting signal with the output. C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

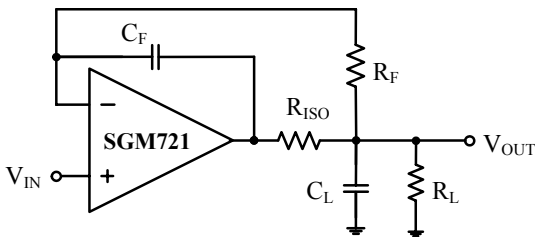


Figure 2. Indirectly Driving Heavy Capacitive Load with DC Accuracy

For no-buffer configuration, there are two other ways to increase the phase margin: (a) by increasing the amplifier's gain or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

Power-Supply Bypassing and Layout

The SGM72x family operates from either a single +2.5V to +5.5V supply or dual $\pm 1.25V$ to $\pm 2.75V$ supplies. For single-supply operation, bypass the power supply V_{DD} with a $0.1\mu F$ ceramic capacitor which should be placed close to the V_{DD} pin. For dual-supply operation, both the V_{DD} and the V_{SS} supplies should be bypassed to ground with separate $0.1\mu F$ ceramic capacitors. $2.2\mu F$ tantalum capacitor can be added for better performance.

Good PC board layout techniques optimize performance by decreasing the amount of stray capacitance at the op amp's inputs and output. To decrease stray capacitance, minimize trace lengths and widths by placing external components as close to the device as possible. Use surface-mount components whenever possible.

For the operational amplifier, soldering the part to the board directly is strongly recommended. Try to keep the high frequency big current loop area small to minimize the EMI (electromagnetic interfacing).

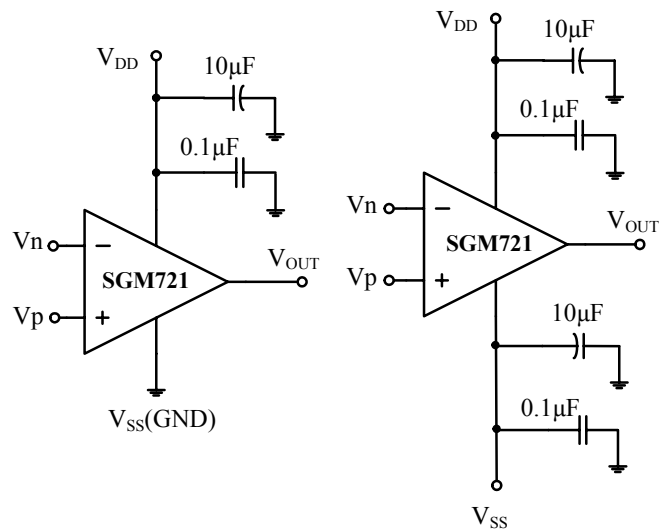


Figure 3. Amplifier with Bypass Capacitors

Grounding

A ground plane layer is important for SGM72x circuit design. The length of the current path speed currents in an inductive ground return will create an unwanted voltage noise. Broad ground plane areas will reduce the parasitic inductance.

Input-to-Output Coupling

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

Typical Application Circuits

Differential Amplifier

The circuit shown in Figure 4 performs the difference function. If the resistors ratios are equal ($R4 / R3 = R2 / R1$), then $V_{OUT} = (Vp - Vn) \times R2 / R1 + Vref$.

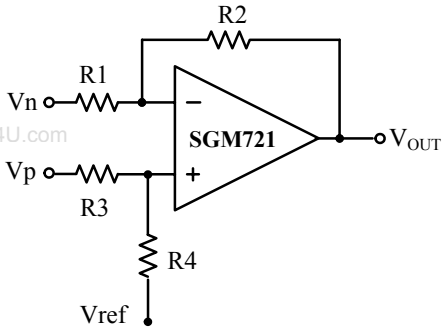


Figure 4. Differential Amplifier

Instrumentation Amplifier

The circuit in Figure 5 performs the same function as that in Figure 4 but with the high input impedance.

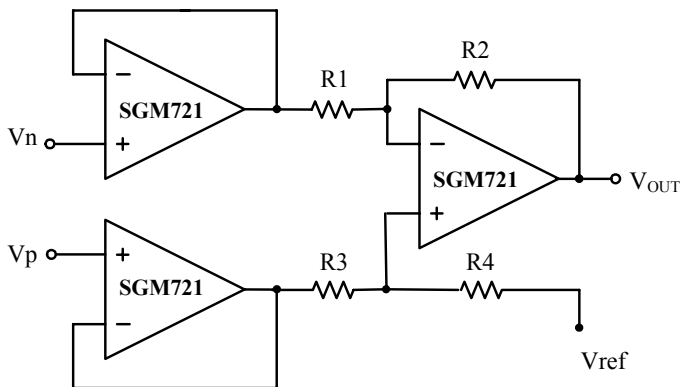


Figure 5. Instrumentation Amplifier

Low Pass Active Filter

The low pass filter shown in Figure 6 has a DC gain of $(-R2/R1)$ and the -3dB corner frequency is $1/2\pi R2C$. Make sure the filter is within the bandwidth of the amplifier. The Large values of feedback resistors can couple with parasitic capacitance and cause undesired effects such as ringing or oscillation in high-speed amplifiers. Keep resistors value as low as possible and consistent with output loading consideration.

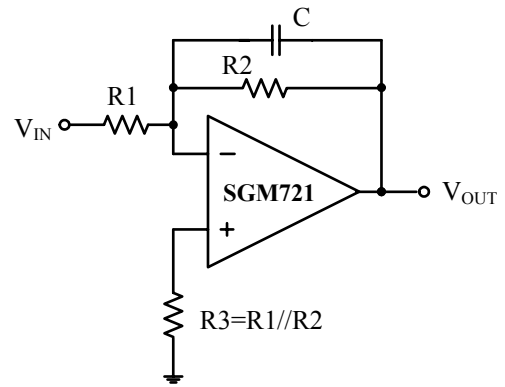
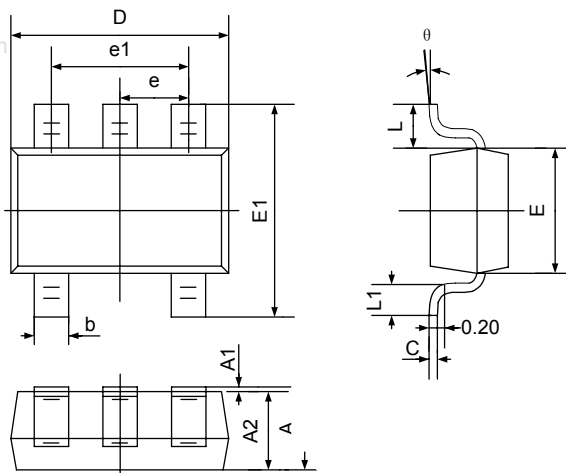


Figure 6. Low Pass Active Filter

PACKAGE OUTLINE DIMENSIONS

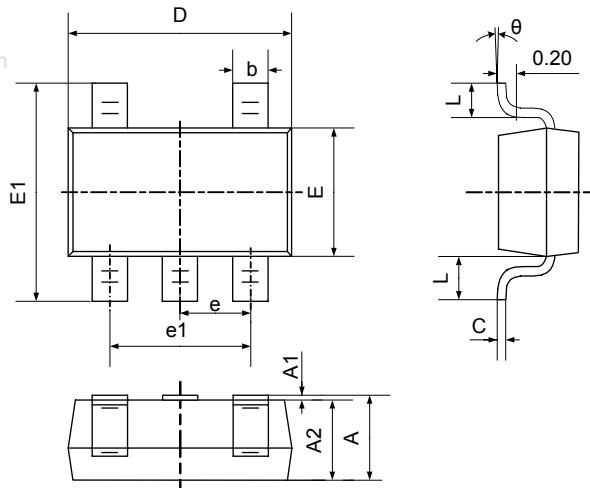
SC70-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650TYP		0.026TYP	
e1	1.200	1.400	0.047	0.055
L	0.525REF		0.021REF	
L1	0.260	0.460	0.010	0.018
theta	0°	8°	0°	8°

PACKAGE OUTLINE DIMENSIONS

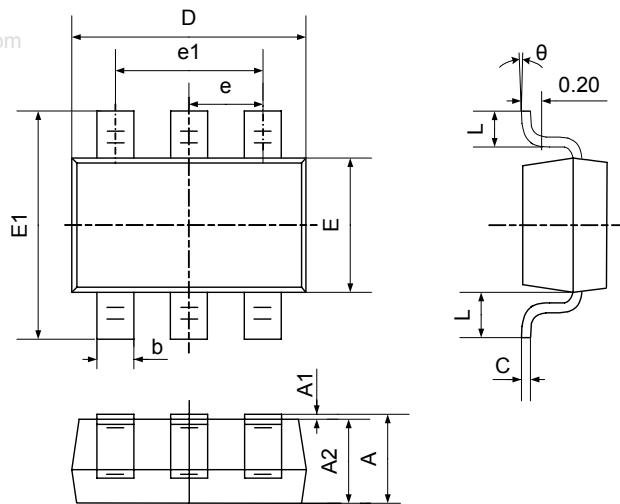
SOT23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

PACKAGE OUTLINE DIMENSIONS

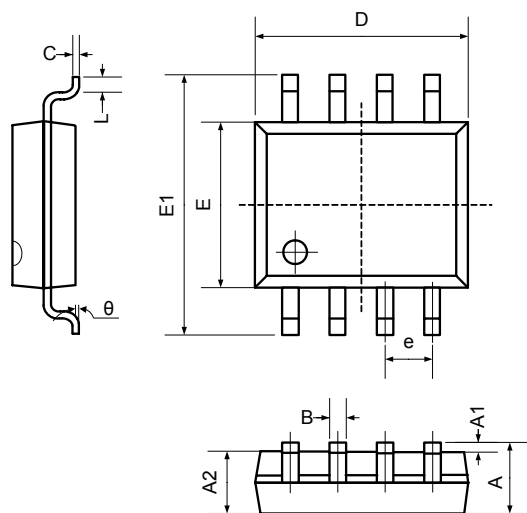
SOT23-6



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
theta	0°	8°	0°	8°

PACKAGE OUTLINE DIMENSIONS

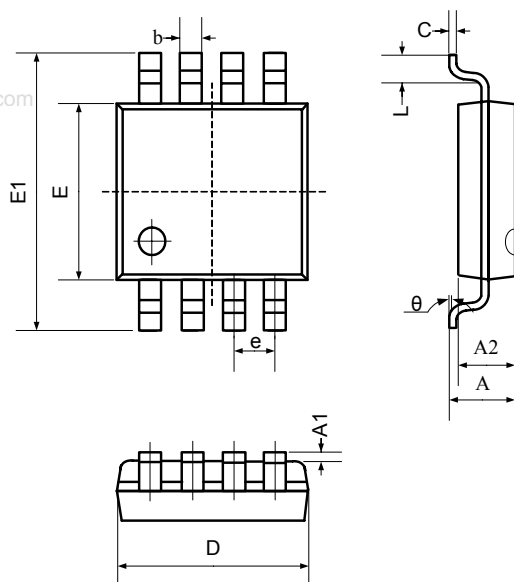
SO-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

PACKAGE OUTLINE DIMENSIONS

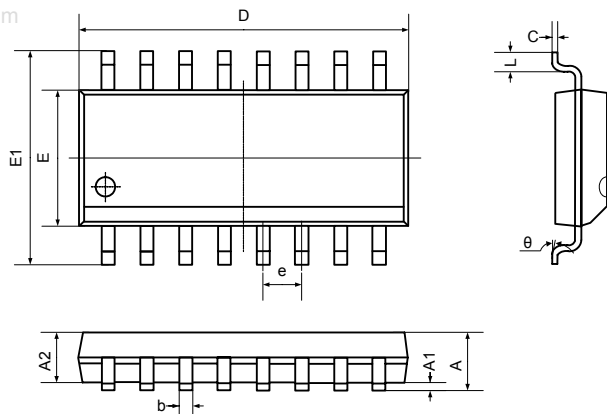
MSOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
c	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026 TYP	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L	0.410	0.650	0.016	0.026
θ	0°	6°	0°	6°

PACKAGE OUTLINE DIMENSIONS

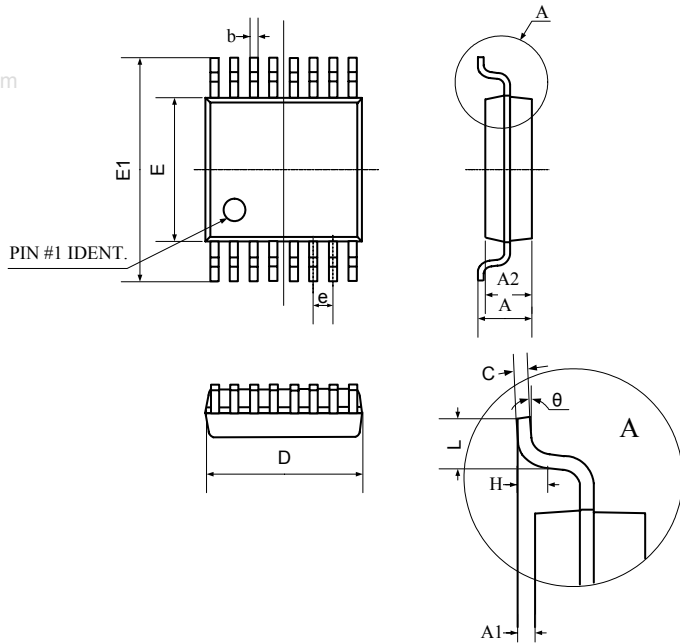
SO-16



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.20	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
theta	0°	8°	0°	8°

PACKAGE OUTLINE DIMENSIONS

TSSOP-16



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	4.900	5.100	0.193	0.201
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

REVISION HISTORY

Location	Page
11/06— Data Sheet changed from REV. A to REV. B	
Changes to ABSOLUTE MAXIMUM RATINGS	3

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