T-51-10-12

MP674

Complete 12-Bit, 12 µs Analog-to-Digital Converter with Microprocessor Interface

Micro Power Systems

FEATURES

- Complete 12-Bit A/D Converter with Reference Clock and Three-State Outputs
- Digital Error Correction
- Full 8, 12 or 16-Bit Microprocessor Bus Interface
- 100 ns Bus Access Time
- No Missing Codes over Temperature
- Minimal Setup Time for Control Signals
- 12µs typ. Conversion Time over Temperature
- Precision Reference for Long Term Stability and Low Gain Tempco
- Monolithic BiCMOS Construction
- Byte Enable/Short Cycle (A0 Input)
- ESD Protection: 1500 V Minimum
- Faster Version of the MP574A
- Low Power: 240 mW typ.
- Same Pin Out as MP574A
- Guaranteed Performance at ±12 V and ±15 V
- PDIP, SOIC & PLCC Packages Available

APPLICATIONS

- Industrial Data Acquisition Systems
- High-Speed Electronics Test and Scientific Instrumentation
- Process Control Systems
- Digital Signal Processing

3

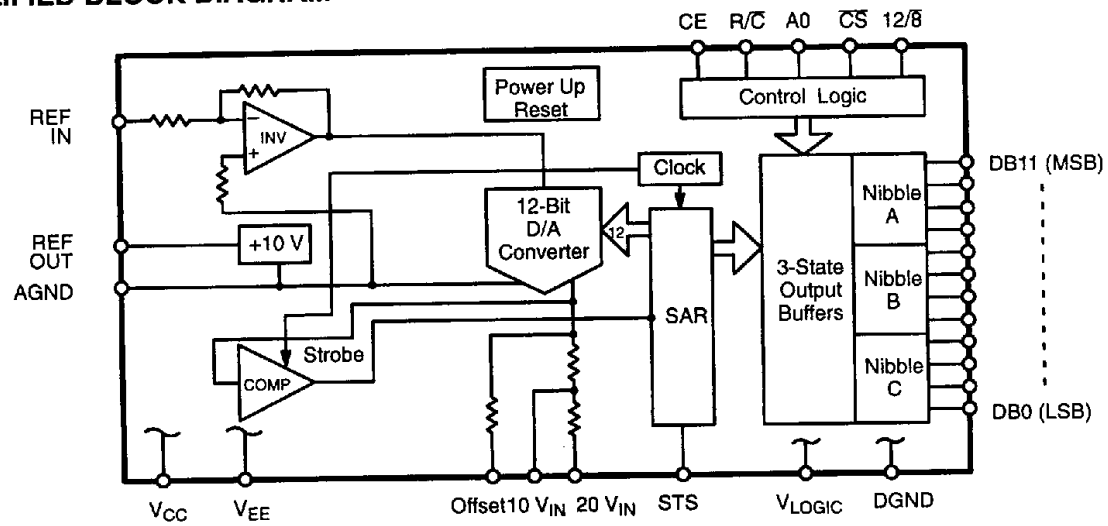
GENERAL DESCRIPTION

The MP674 is a complete 12-bit Successive Approximation Analog-to-Digital Converter with 3-state output buffers for direct interfacing to 8- and 16-bit microprocessor busses. The MP674 is implemented in advanced BiCMOS, the converter includes a digital error correction circuit. Micro Power Systems utilizes a proprietary decoding technique to improve drift performance and to guarantee no missing codes for all grades. Also, precision low temperature coefficient resistors are used to set critical performance parameters.

Designed for full scale range of ±20 V, ±5 V, +10 V, or +20 V, the MP674 will operate with any supply voltage between ±12 V and ±15 V without special selection. Offset, linearity, and full-scale errors are minimized by laser trimming. To improve digital noise immunity and ease the digital interface, all digital inputs and outputs have been designed for true TTL compatibility.

Specified for operation over the commercial (0 to +70°C) temperature range, the MP674 is available in Plastic dual-in-line (PDIP), Surface Mount (SOIC) and Plastic Leaded Chip Carrier (PLCC) packages.

SIMPLIFIED BLOCK DIAGRAM



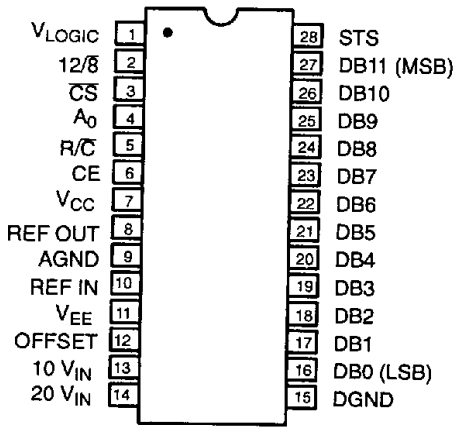
MP674

Micro Power Systems

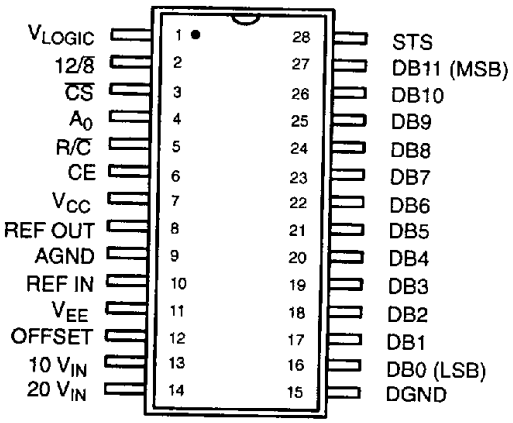
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	0 to 70°C	MP674JN	±1	±1	0.3
Plastic Dip	0 to 70°C	MP674KN	±1/2	±1	0.3
SOIC	0 to 70°C	MP674JS	±1	±1	0.3
SOIC	0 to 70°C	MP674KS	±1/2	±1	0.3
PLCC	0 to 70°C	MP674JP	±1	±1	0.3
PLCC	0 to 70°C	MP674KP	±1/2	±1	0.3

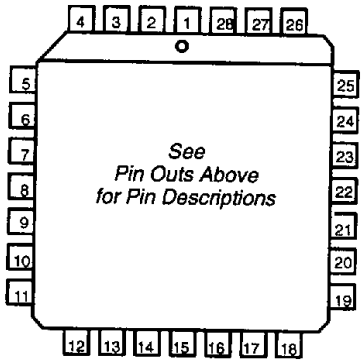
PIN CONFIGURATIONS



28 Pin PDIP, (0.600")
N28



28 Pin SOIC, (Jedec, 0.300")
S28



28 Pin PLCC
P28

Micro Power Systems

MP674

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	V_{LOGIC}	+5 V Logic Supply
2	12/$\overline{8}$	Select Format of Output Bits (8 or 12) (TTL Compatible)
3	$\overline{CS}$	Chip Select. Enables Conversions on Falling Clock Edge
4	A0	Access High 8 Bits or Low 4 Bits Plus 4 Zeroes (Read Mode)
5	R/$\overline{C}$	Read/Convert: Main Control for Stand-Alone Operation
6	CE	Chip Enable. Enables Conversion on Rising Clock Edge
7	V_{CC}	+12 V to +15 V
8	REF OUT	Output from Internal +10 V Reference

PIN NO.	NAME	DESCRIPTION
9	AGND	Analog Ground
10	REF IN	Input for Voltage Reference
11	V_{EE}	−12 V to −15 V
12	OFFSET	Voltage Input for Bipolar Operations, or Zero Adjust
13*	10 V_{IN}	Input for 0 to +10 V or −5 V to +5 V Operation
14	20 V_{IN}	Input for 0 to +20 V or −10 V to +10 V
15	DGND	Digital Ground
16-27	Output Data Bits	DB0 (LSB) to DB11 (MSB)
28	STS	Status Flag

* When not in use, NC to avoid noise pick-up.

3

DEFINING THE CONTROL FUNCTIONS

FUNCTION	DEFINITION	FUNCTION
CE	Chip Enable	1. Typically used as clock synchronization with µp. 2. Must be high (1) for a conversion to start. 3. Must be high (1) to read data on the output. 4. ↑ Transition may be used to initiate conversion.
$\overline{CS}$	Chip Select	1. Typically the address pin when used with a microprocessor. 2. Must be low (0) for a conversion to start. 3. ↓ Transition may be used to initiate conversion.
R/$\overline{C}$	Read/Convert	1. ↓ Initiate conversion. 2. ↑ Initiate read.
A0	Address	1. Selects conversion mode 12 Bits if low (0) 8 Bits if high (1). 2. In read mode A0 selects the output format. If low (0) then 8 MSB's (high and middle byte) are enabled. If high (1) then the 4 LSB's are enabled.
12/$\overline{8}$	Output Format	1. Usually hard-wired. 2. Normal 12-Bit format if high (1). 3. 8-Bit format as set by A0 if low (0).

* When not in use, NC to avoid noise pick-up.

MP674

Micro Power Systems

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: V_{CC} = +15 V, V_{LOGIC} = +5 V, V_{EE} = −15 V, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
KEY FEATURES								FSR = Full Scale Range
Resolution		12			12		Bits	
ACCURACY (K Grade)								
Differential Non-Linearity	DNL			±1		±1	LSB	
Integral Non-Linearity	INL			±1/2		±1/2	LSB	
Unipolar Offset	U_{OZT}			±2		±2	LSB	Adjustable to Zero
Bipolar Offset[1]	B_{OZT}			±4		±4	LSB	Adjustable to Zero
Full Scale Calibration Error (with fixed 50Ω resistor from REF OUT to REF IN)	FSE			±0.3		±0.3	% FSR	Adjustable to Zero
Tempco[2]								
Unipolar Offset	TC_{UOZT}					±1 (5)	LSB	(ppm/°C)
Bipolar Offset	TC_{BOZT}					±1 (5)	LSB	(ppm/°C)
Full Scale Calibration	TC_{FSE}					±5 (27)	LSB	(ppm/°C)
ACCURACY (J Grade)								
Differential Non-Linearity	DNL			±1		±1	LSB	
Integral Non-Linearity	INL			±1		±1	LSB	
Unipolar Offset	U_{OZT}			±2		±2	LSB	Adjustable to Zero
Bipolar Offset[1]	B_{OZT}			±4		±4	LSB	Adjustable to Zero
Full Scale Calibration Error (with fixed 50Ω resistor from REF OUT to REF IN)	FSE			±0.3		±0.3	% FSR	Adjustable to Zero
Tempco[2]								
Unipolar Offset	TC_{UOZT}					±2 (10)	LSB	(ppm/°C)
Bipolar Offset	TC_{BOZT}					±1 (10)	LSB	(ppm/°C)
Full Scale Calibration	TC_{FSE}					±5 (50)	LSB	(ppm/°C)
POWER SUPPLY REJECTION								
Max Change in FS Calibration V_{CC} = 15V ±1.5V or 12V ±0.6 V								
J Grade			±2			±2	LSB	
K Grade			±1			±1	LSB	
V_{LOGIC} = 5V ±0.5V			±1/2			±1/2	LSB	
ANALOG INPUT								
Input Ranges	A_{IN}							
Bipolar 10 V_{IN}		−5		5	−5	5	V	
20 V_{IN}		−10		10	−10	10	V	
Unipolar 10 V_{IN}		0		10	0	10	V	
20 V_{IN}		0		20	0	20	V	
Input Impedance	R_{IN}							
10 V_{IN}		3	5	7	3	7	kΩ	
20 V_{IN}		6	10	14	6	14	kΩ	
DIGITAL INPUTS[3]								Inputs CE, $\overline{CS}$, R/$\overline{C}$, A0, 12/$\overline{8}$
Logical "1" Voltage	V_{IH}	2.0			2.0		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Current	I_{IN}	−5	0.1	5	−5	5	µA	
Capacitance[4]	C_{IN}		5				pF	

Micro Power Systems

MP674

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Description	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Conditions
DIGITAL OUTPUTS								DB11-DB0, STS
Logical "1" Voltage	V_{OH}	2.4			2.4		V	I_{SOURCE} = ≤ 500µA
Logical "0" Voltage	V_{OL}			0.4		0.4	V	I_{SINK} = ≤ 1.6mA
Output Leakage	I_{OL}	–5		5	–5	5	µA	DB11-DB0, Hi-Z State
Capacitance[4]	C_O		5				pF	
POWER SUPPLIES (Tmin to Tmax)								
Operating Range								
V_{LOGIC}	V_{LL}	4.5		5.5	4.5	5.5	V	
V_{CC}	V_{CC}	11.4		16.5	11.4	16.5	V	
V_{EE}	V_{EE}	–11.4		–16.5	–11.4	–16.5	V	
Operating Current								
I_{LOGIC}			3	6		8	mA	
I_{CC}			7	10		12	mA	
I_{EE}			8	12		14	mA	
POWER DISSIPATION	P_D							
V_{LOGIC} = +5 V, V_{CC} = +15 V, V_{EE} = –15 V			240	360		430	mW	
V_{LOGIC} = +5 V, V_{CC} = +12 V, V_{EE} = –12 V			200	300		360	mW	
INTERNAL REFERENCE								
Reference Voltage	V_{REF}	9.95	10.00	10.05	9.95	10.05		
Output Current (External Load)	I_{REF}	1.5	5		1.5		mA	External load should not change during conversion

NOTES
(1) Bipolar offset zero transition.
(2) ppm/°C information for reference only.
(3) Detailed timing specifications appear in the timing section.
(4) Guaranteed, but not production tested.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (1, 2) (T_A = +25°C unless otherwise noted)

V_{CC} to DGND ..... 0 to +16.5 V
V_{EE} to DGND ..... 0 to –16.5 V
V_{LOGIC} to DGND ..... 0 to +7 V
AGND to DGND ..... ±1 V
Control Inputs (CE, $\overline{CS}$, A0, 12/$\overline{8}$, R/$\overline{C}$) to DGND ..... –0.5 V to V_{LOGIC} +0.5 V
Analog Inputs (REF IN, OFFSET, 10 V_{IN}) to AGND ..... ±16.5 V
20 V_{IN} to AGND ..... ±24 V
REF OUT ..... Indefinite short to DGND, Momentary short to V_{CC}
Package Power Dissipation Rating to 75°C
PDIP, SOIC, PLCC 1000mW
Derates above 75°C ..... 14mW/°C
Lead Temperature, Soldering ..... +300°C, 10 Sec
Storage Temperature ..... –65°C to +150°C

NOTES:
(1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
(2) Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.

MP674

Micro Power Systems

APPLICATION DATA

The MP674 is a complete A/D converter system, with its own built-in reference and clock. It may be used by itself ("stand-alone" operation), or it may be interfaced with a microprocessor which can control both conversion and formatting of output.

Successful application of the MP674 requires careful attention to four main areas:

1) Physical layout.
2) Connection/Trimming according to mode of operation.
3) Conditioning of input signals.
4) Controlling and timing considerations.

Physical Layout

The 12-bit accuracy of the MP674 represents a dynamic range of 72dB. In order that this be preserved, thorough precautions must be taken to avoid any interfering signals, whether conducted or radiated. It is therefore recommended that one:

- Avoid placing the device and its analog signals near logic traces. In general, using a double sided printed circuit card with a good ground plane on the component side is recommended. Routing analog signals between ground traces will help isolate digital control logic. If these lines cross, do so at right angles.
- Power supplies should be quiet and well regulated. Grounds should be tied together at the package and back to the system ground with a single path. Bypass the supplies at the device with a 0.01 to 0.1μF ceramic cap and a 10-47 μF tantalum type, in parallel.
- Use well-regulated and filtered power supplies.

Connection/Trimming

There are two modes of operation, each with two submodes, Unipolar, 0 to +10 V or 0 to +20 V; and Bipolar, –5 V to +5 V or –10 V to +10 V. If the accuracy of the MP674 as supplied is sufficient for the application, connect the device as shown in *Figures 1 & 2.*

If greater accuracy is required, the part may be trimmed. The procedure is as follows:

Unipolar Mode: Connect MP674 as shown in *Figure 3.* R1 is used to adjust the converter offset so that an input voltage equivalent to 1/2 LSB will produce the first change in the output codes (0000 0000 0000 to 0000 0000 0001). This input is 1.22 mV for the 10 V scale (pin 13) or 2.44 mV for the 20 V scale (pin 14). Using one of these inputs, R1 should be adjusted until the output flickers between the above code values.

Having trimmed zero scale (adjusted the offset), the all –"1"s level can be set using R2 (gain adjust). Apply an input of 9.9963V to pin 13 (or 19.9927V to pin 14). This is 1.5 or 1 1/2 LSB less than 10 V (20 V). Adjust R2 until the output flickers between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Mode: In the bipolar mode the user can either adjust the ± Fullscale limits, or adjust the zero transition and gain (+ Fullscale), as is best suited to the end application.

1. To set ± Fullscale: Connect MP674 as shown in *Figure 4.* Apply –4.9988 V to pin 13 (or –9.9976 V to pin 14) and adjust R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Then apply +4.9963 V to pin 13 (or +9.9927 V to pin 14) and adjust R2 for flicker between output codes 1111 1111 1110 and 1111 1111 1111.
2. To set Zero Transition and Gain: Connect MP674 as shown in *Figure 4.* Apply 0.0000V to pin 13 (for +5 V fullscale applications) or pin 14 (for +10 V fullscale systems) and adjust R1 until the output code flickers between 0111 1111 1111 and 1000 0000 0000. Then apply +4.9963 V to pin 13 (or +9.9927 V to pin 14) and adjust R2 for flicker between output codes 1111 1111 1111 and 1111 1111 1110.

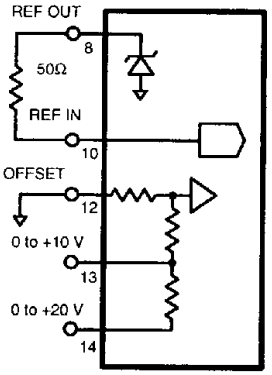


Figure 1.
Unipolar Operation

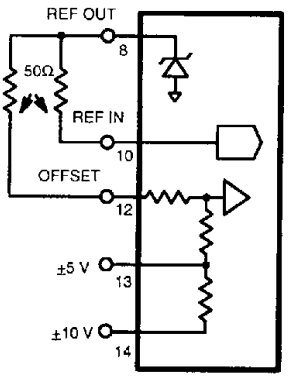


Figure 2.
Bipolar Operation

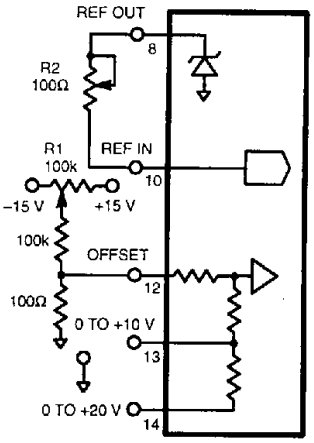


Figure 3.
Unipolar Operation
with
Trim Adjustments

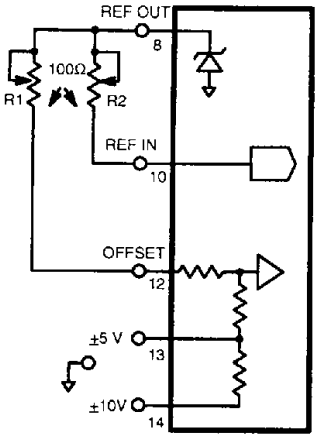


Figure 4.
Bipolar Operation
with
Trim Adjustments

Micro Power Systems

MP674

Control and Timing Considerations

The MP674 can be operated in the stand-alone mode, with one line for control and everything else hard-wired; or under microprocessor control, where changes can be made dynamically. There are 5 control lines: CE, $\overline{CS}$, R/$\overline{C}$, A0 and 12/$\overline{8}$ with their functions described in the box "Defining the Control Functions". The role each line plays in control is shown in the MP674 Truth Table.

TRUTH TABLE

Control Inputs					MP674 Operation
CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A0	
0	X	X	X	X	No Operation
X	1	X	X	X	No Operation
1	0	↓	X	0	Initiates 12-Bit Conversion
1	0	↓	X	1	Initiates 8-Bit Conversion
↑	0	0	X	0	Initiates 12-Bit Conversion
↑	0	0	X	1	Initiates 8-Bit Conversion
1	↓	0	X	0	Initiates 12-Bit Conversion
1	↓	0	X	1	Initiates 8-Bit Conversion
1	0	↑	1	X	Enables 12-Bit Parallel Output
1	0	↑	0	0	Enables 8 MSBs
1	0	↑	0	1	Enables 4 LSBs and 4 Trailing Zeros

TIMING

The MP674 is easily interfaced to a wide variety of microprocessors and other digital systems. Discussion of the timing requirements of the MP674 control signals will provide the system designer with useful insight into the operation of the device.

Figure 5. shows a complete timing diagram for the MP674 convert start operation. R/$\overline{C}$ should be low before both CE and $\overline{CS}$ are asserted; If R/$\overline{C}$ is high, a read operation will momentarily occur, possibly resulting in system bus contention.

Either CE or $\overline{CS}$ may be used to initiate a conversion. We recommend using CE, however, as it includes one less propagation delay than $\overline{CS}$. As shown in *Figure 5.*, CE is used. If $\overline{CS}$ is used to trigger the conversion the specified set-up times will be longer.

Once a conversion is started and the STS line goes high, convert start commands will be ignored until the conversion cycle is completed. The output data buffers cannot be enabled during conversion. However, all inputs and outputs which change during conversion can introduce noise.

CONVERT START TIMING – FULL CONTROL MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DSC}	STS Delay from CE	–	80	200	ns
t_{HEC}	CE Pulse Width	50	40	–	ns
t_{SSC}	$\overline{CS}$ to CE Setup	50	20	–	ns
t_{HSC}	$\overline{CS}$ Low During CE High	50	25	–	ns
t_{SRC}	R/$\overline{C}$ to CE Setup	50	0	–	ns
t_{HRC}	R/$\overline{C}$ Low During CE High	50	25	–	ns
t_{SAC}	A_0 CE Setup	0	0	–	ns
t_{HAC}	A_0 Valid During CE High	50	30	–	ns
t_C	Conversion Time 8-Bit Cycle 12-Bit Cycle	 3 6	 5 12	 10 15	 µs µs

Figure 6. shows the timing for data read operations. The MP674 features fast access times and short data latency times. This simplifies the interface to faster microprocessors. During data read operations, access time is measured from the point where CE and R/$\overline{C}$ both are high (assuming $\overline{CS}$ is already low).

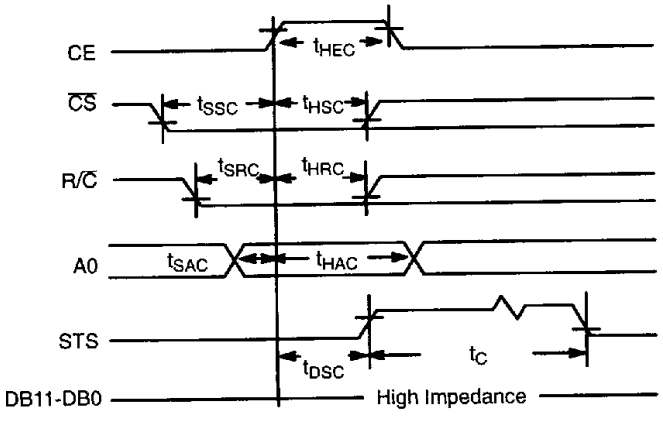


Figure 5. Convert Start Timing

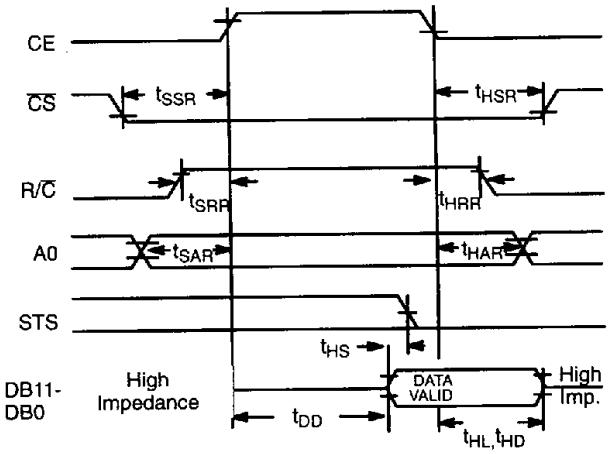


Figure 6. Read Cycle Timing

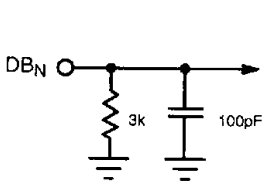
MP674

Micro Power Systems

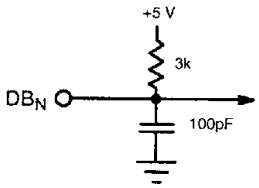
READ TIMING – FULL CONTROL MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DD}1	Access Time (from CE)	–	80	150	ns
t_{HD}	Data Valid after CE Low	25	35	–	ns
t_{HL}2	Output Float Delay	–	60	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup	50	0	–	ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0	0	–	ns
t_{SAR}	A0 to CE Setup	50	25	–	ns
t_{HSR}	$\overline{CS}$ Valid After CE Low	0	0	–	ns
t_{HRR}	R/$\overline{C}$ High After CE Low	0	0	–	ns
t_{HAR}	A0 Valid After CE Low	50	25	–	ns

1. t_{DD} is measured with the load circuit of *Figure 7.* and defined as the time required for an output to cross 0.4 V or 2.4 V.
2. t_{HL} is defined as the time required for the data lines to change 0.5 V when loaded with the circuit of *Figure 8.*

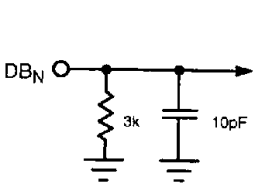


a. High-Z to Logic 1

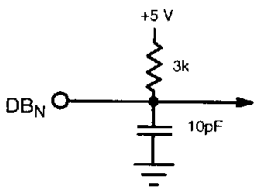


b. High-Z to Logic 0

Figure 7. Load Circuit for Access Time Test



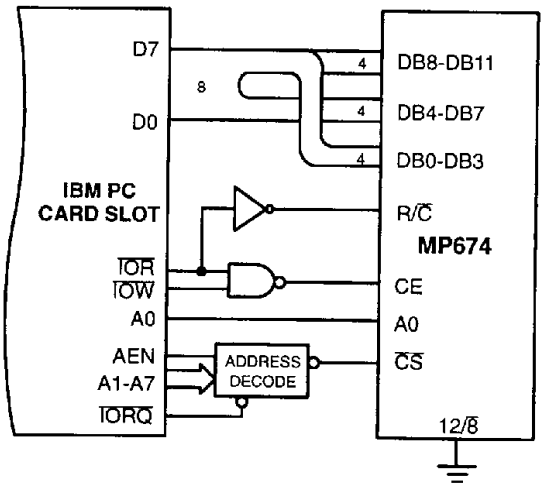
a. Logic 1 to High-Z



b. Logic 0 to High-Z

Figure 8. Load Circuit for Output Float Delay Test

IBM PC - MP674 INTERFACE



Micro Power Systems

MP674

"STAND-ALONE" OPERATION

The MP674 can be used in a "stand-alone" mode, which is useful in systems not requiring full computer bus interface capability.

In this mode, CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A0 are wired low, and conversion is controlled by R/C. The three-state buffers are enabled when R/$\overline{C}$ is high and a conversion starts when R/$\overline{C}$ goes low. This gives rise to two possible control signals – a high pulse or a low pulse. Operation with a low pulse is shown in *Figure 9.* In this case, the outputs are forced into the high impedance state in response to the falling edge of R/$\overline{C}$ and return to valid logic levels after the conversion cycle is completed. The STS line goes high 50 ns after R/$\overline{C}$ goes low and returns low 100 ns after data is valid.

If conversion is initiated by a high pulse as shown in *Figure 10.*, the data lines are enabled during the time when R/$\overline{C}$ is high. The falling edge of R/$\overline{C}$ starts the next conversion and the data lines return to three-state (and remain three-state) until the next high pulse of R/$\overline{C}$.

CONDITIONING OF INPUT SIGNALS

It is important that the signal being applied to the MP674 input not change during a conversion cycle (it should be stable to within 1/2 LSB). Since that input is being subjected to the DAC test signals (12 comparisons in 12µs = 1 MHz), the driving buffer should have a low impedance at 1 MHz.

STAND-ALONE MODE TIMING

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50	30	–	ns
t_{DS}	STS Delay from R/$\overline{C}$	–	60	200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	20	25	–	ns
t_{HL}	Output Float Delay	–	100	150	ns
t_{HS}	STS Delay After Data Valid	25	–	850	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150	50	–	ns
t_{DDR}	Data Access Time	–	90	150	ns

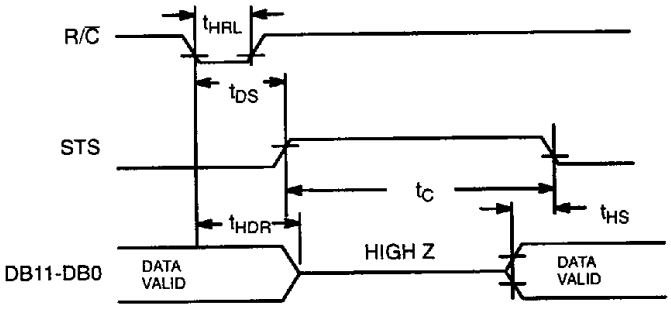


Figure 9. Low Pulse for R/$\overline{C}$. Outputs Enabled After Conversion

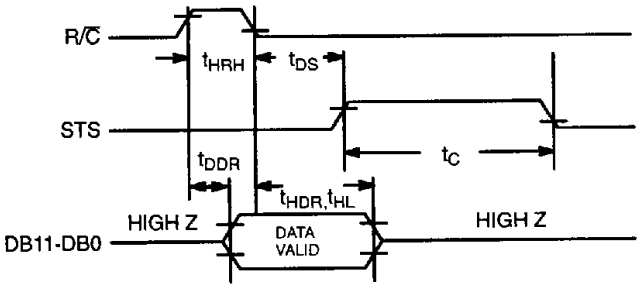


Figure 10. High Pulse for R/$\overline{C}$. Outputs Enabled While R/$\overline{C}$ High, Otherwise High-Z