October 27, 1997

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DESCRIPTION:

The MP60 series of power modules are economical 49W (nominal) switching DC:DC converters with an integral connector designed to Intel Corporation's Voltage Regulator Module specification for the Klamath Processor. The module has additional monitoring functions for Power Good Signal, Output Enable and Upgrade Present.

The output voltage can be set between 1.8V and 3.5V by means of a five bit voltage identification code, to support current and future versions of the Pentium® Pro, Klamath and OverDrive® processor variants.

To power Pentium® Pro processors (VRM 8.0) use MP60-E.

FEATURES:

- Integral 40-pin header connector
- Programmable output voltage to suit processor (by VID code); adjustable from 1.8 to 3.5V
- Maximum output current 14A
- Efficiency >80% at full load
- Designed to specifications for Intel Klamath Processor voltage regulator module
- Fast transient response

APPLICATIONS:

- Intel Klamath Power Supply

ORDERING INFORMATION:

DEVICE	V_{OUT} (volts)
MP60-F	Programmable

ELECTRICAL CHARACTERISTICS

Conditions: V_O = 3.1V, V_{IN} = 4.75 - 5.25V, I_O = 10A, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Output Voltage	V_O	0.96lV_Ol		1.05lV_Ol	V
Output Current	I_O			14	A
Current Surge Limit	I_S		16		A
Output Over Voltage Protection		Setpoint + 20%			V
Output Slew Rate		30			A/µs
Quiescent Current	I_Q	1			mA
Temperature Coefficient	T_C		TBD		%/°C
Temperature Stability	T_S		TBD		%
Operating Efficiency (full load)	η	80	86		%
Switching Frequency	f_{SW}		100		kHz
DC Output Ripple Voltage				48	mV_{p-p}
Operating Temperature Range	T_J	0		60	°C

NOTES:
(1) Low duty cycle pulse testing with Kelvin connections required.
(2) Bandwidth of 10 Hz to 10 kHz.

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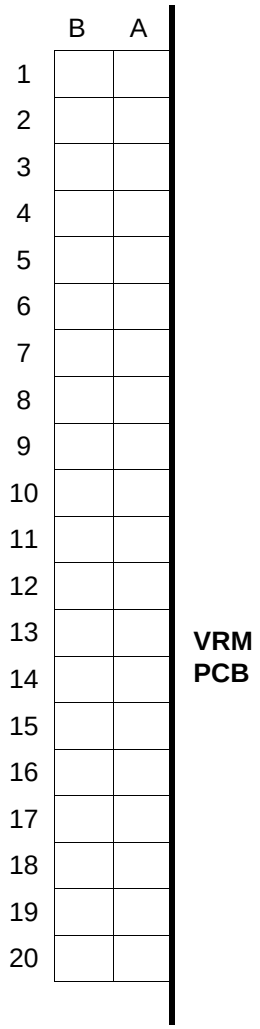
INPUT AND OUTPUT CONNECTIONS			
Pin No.	**Row A**	**Row B**	**Pin No.**
1	5V in	5V in	1
2	5V in	5V in	2
3	5V in	Reserved	3
4	12V in	12V in	4
5	Reserved	UP#	5
6	I Share	OUTEN	6
7	VID0	VID1	7
8	VID2	VID3	8
9	VID4	PWRGD	9
10	V_{CCVID}	V_{SS}	10
11	V_{SS}	V_{CCVID}	11
12	V_{CCVID}	V_{SS}	12
13	V_{SS}	V_{CCVID}	13
14	V_{CCVID}	V_{SS}	14
15	V_{SS}	V_{CCVID}	15
16	V_{CCVID}	V_{SS}	16
17	V_{SS}	V_{CCVID}	17
18	V_{CCVID}	V_{SS}	18
19	V_{SS}	V_{CCVID}	19
20	V_{CCVID}	V_{SS}	20



End view of VRM connector
(viewed from motherboard side)

VOLTAGE REGULATOR MODULE CONNECTOR PIN REFERENCE

Pin Name	Pin Function
PWRGD	**Power Good:** When the output voltage is not within specifications (nominal or selected voltage ± 7%) this signal will be in the low state. The PWRGD signal will change to the proper state within 5ms of the output coming into or going out of specification.
OUTEN	**Output Enable:** A low state disables the output voltage. When disabled, the PWRGD signal will be in the low state.
UP#	**Upgrade Present:** Used to indicate the presence of an upgrade processor. Typical state is high (standard processor in system). When in the low or ground state (OverDrive™ processor in system) the output voltage shall be disabled unless the converter can supply to an OverDrive processor's specifications. When disabled, the PWRGD output will be in the low state.
VID(0:4)	**Voltage Identification:** The module will accept five open collector signals, used to indicate the voltage required by the processor, as defined by Intel
5V in	Main power input for regulation.
12V in	Must also be connected (input for control circuits only)

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VOLTAGE IDENTIFICATION CODE

Klamath Pins					V_{CCP}
VID4	VID3	VID2	VID1	VID0	(VDC)
0	0	1	0	1	1.800
0	0	1	0	0	1.850
0	0	0	1	1	1.900
0	0	0	1	0	1.950
0	0	0	0	1	2.000
0	0	0	0	0	2.050
1	1	1	1	1	2.000
1	1	1	1	0	2.100
1	1	1	0	1	2.200
1	1	1	0	0	2.300
1	1	0	1	1	2.400
1	1	0	1	0	2.500
1	1	0	0	1	2.600
1	1	0	0	0	2.700
1	0	1	1	1	2.800
1	0	1	1	0	2.900
1	0	1	0	1	3.000
1	0	1	0	0	3.100
1	0	0	1	1	3.200
1	0	0	1	0	3.300
1	0	0	0	1	3.400
1	0	0	0	0	3.500

0 = processor pin connected to V_{SS}, 1 = open

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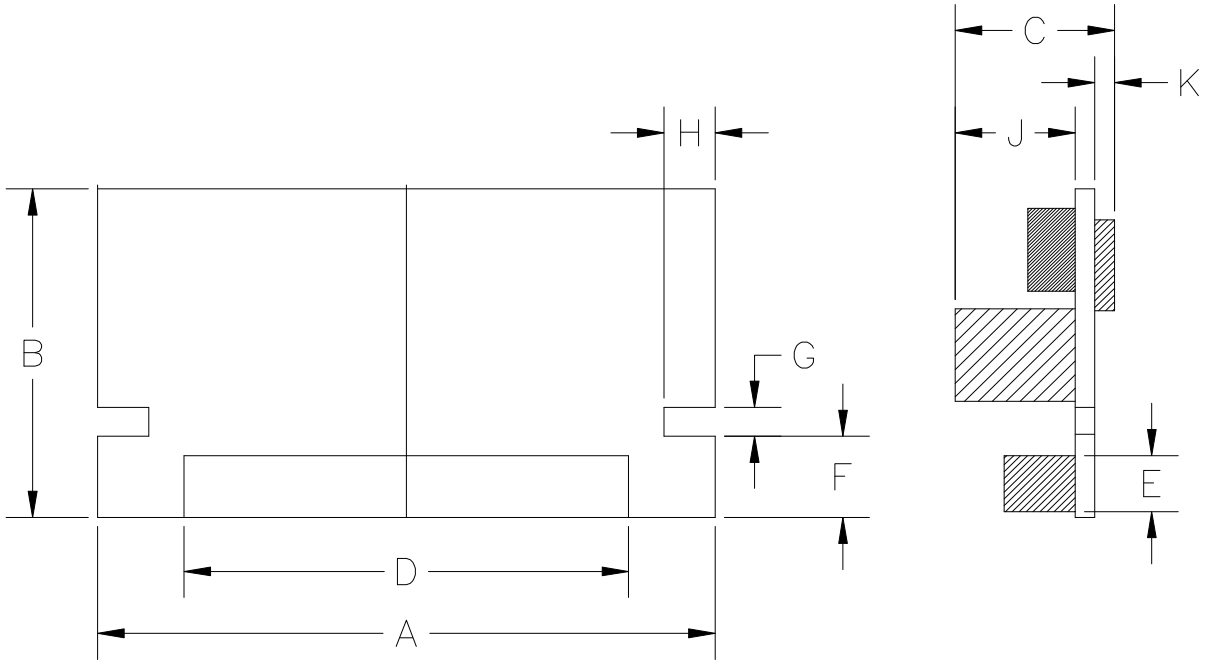
MECHANICAL DIMENSIONS



Dimension	Millimeters	Inches	
A	79.7	3.14	Max
B	38.1	1.50	Max
C	24.4	0.96	Max
D	57.4	2.26	Typ
E	8.13	0.32	Typ
F	10.67 ± 0.13	0.420 ± 0.005	Typ
G	3.81	0.15	Typ
H	6.50	0.26	Min
J	21.6	0.85	Max
K	2.5	0.10	Min

Component size and location for illustration only