

## 500-kHz Half-Bridge DC/DC Controller with Integrated Secondary Synchronous Rectification Drivers

### DESCRIPTION

Si9122A is a half-bridge controller IC ideally suited to fixed telecom applications where high efficiency is required at low output voltages (e.g. < 3.3 V). Designed to operate within the fixed telecom voltage range of 33 V to 75 V and withstand 100 V, 100 ms transients, the IC is capable of controlling and driving both the low and high-side switching devices of a half bridge circuit and also controlling the switching devices on the secondary side of the bridge. Due to the very low on-resistance of the secondary MOSFETs, a significant increase in conversion efficiency can be achieved as compared with conventional Schottky diodes. Control of the secondary devices is by means of a pulse transformer and a pair of inverters. Such a system has efficiencies well in excess of 90 % even for low output voltages. On-chip control of the dead time delays between the primary and secondary synchronous signals keep efficiencies high and prevent accidental destruction of the power transformer. An external resistor sets the switching frequency from 200 kHz to 625 kHz.

Si9122A has advanced current monitoring and control circuitry which allow the user to set the maximum current in the primary circuit. Such a feature acts as protection against output shorting and also provides constant current into large capacitive loads during start-up or when paralleling power supplies. Current sensing is by means of a sense resistor on the low-side primary device.

### FEATURES

- 28 V to 75 V input voltage range
- Compatible with ETSI 300 132-2
- Integrated  $\pm 1$  A half-bridge primary drivers
- Secondary synchronous rectifier control signals with programmable deadtime delay
- Voltage mode control
- Voltage feedforward compensation
- High voltage pre-regulator operates during start-up
- Current sensing on low-side primary device
- Frequency foldback eliminates constant current tail
- Advanced maximum current control during start-up and shorted load
- Low input voltage detection
- Programmable soft-start function
- Over temperature protection


**RoHS  
COMPLIANT**

### APPLICATIONS

- Network cards
- Power supply modules

### FUNCTIONAL BLOCK DIAGRAM

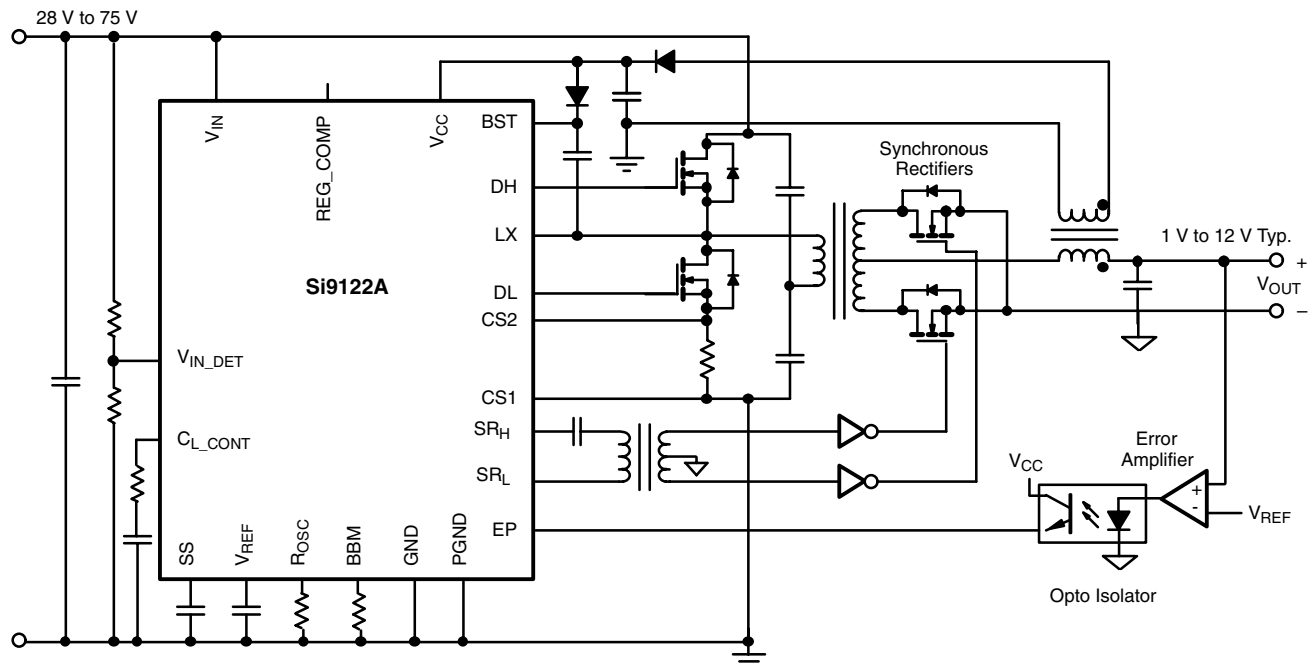


Figure 1.

## TECHNICAL DESCRIPTION

Si9122A is a voltage mode controller for the half-bridge topology. With 100 V depletion mode MOSFET capability, the Si9122A is capable of powering directly from the high voltage bus to  $V_{CC}$  through an external PNP pass transistor, or may be powered through an external regulator directly through the  $V_{CC}$  pin. With PWM control, Si9122A provides peak efficiency throughout the entire line and load range. In order to simplify the design of efficient secondary synchronous rectification circuitry, Si9122A provides intelligent gate drive signals to control the secondary MOSFETs. With independent gate drive signals from the controller, transformer design is no longer limited by the gate to source rating of the secondary-side MOSFETs. Si9122A provides constant  $V_{GS}$  voltage, independent of line voltage to minimize the gate charge loss as well as conduction loss.

A break-before-make function is included to prevent shoot through current or transformer shorting. Adjustable Break-Before-Make time is incorporated into the IC and is programmable by an external resistor value.

Si9122A is packaged in lead (Pb)-free TSSOP-20 and MLP65-20 packages. To satisfy stringent ambient temperature requirements, Si9122A is rated to handle the industrial temperature range of  $-40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$ . When a situation arises which results in a rapid increase in primary (or secondary current) such as output shorted or start-up with a large output capacitor, control of the PWM generator is handed over to the current loop. Monitoring of the load current is by means of an external current sense resistor in the source of the primary low-side switch.

## SI9122 BLOCK DIAGRAM

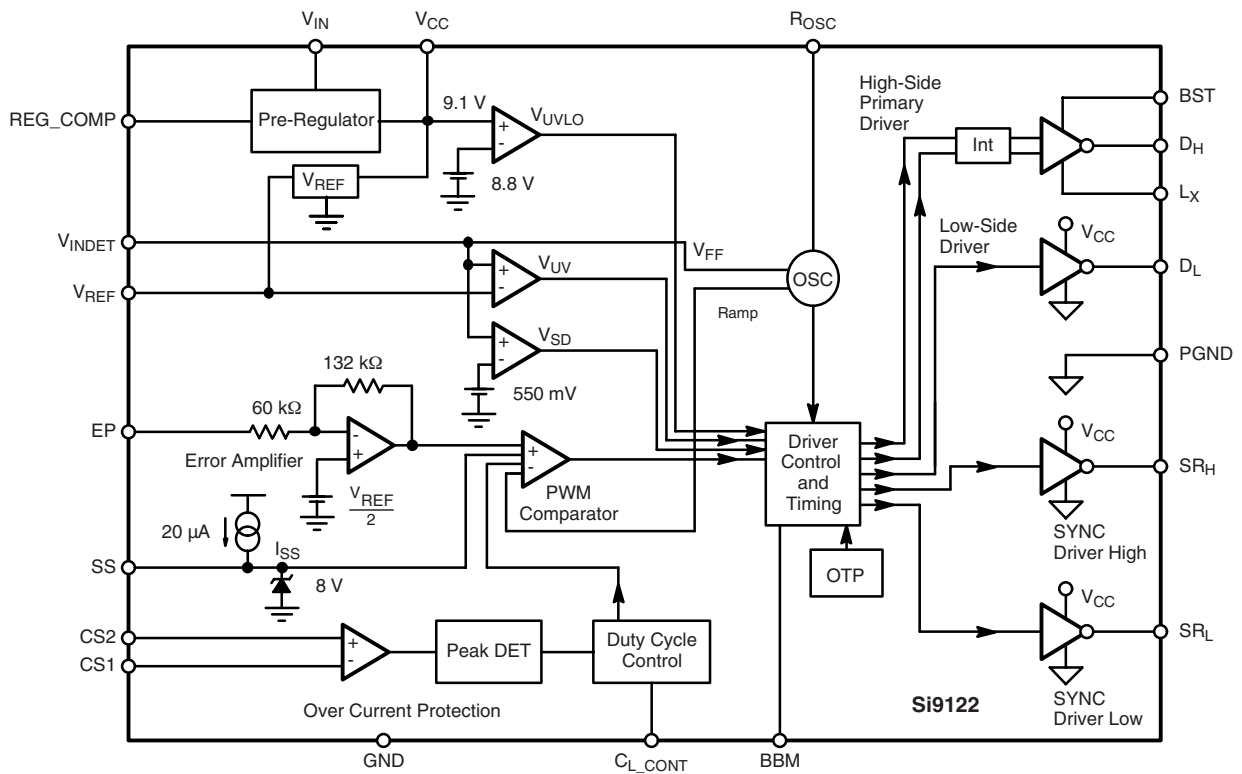


Figure 2.



| <b>ABSOLUTE MAXIMUM RATINGS</b> All voltages referenced to GND = 0 V |                       |                                |      |
|--|-----------------------|--------------------------------|------|
| Parameter  |                       | Limit                          | Unit |
| V <sub>IN</sub> (Continuous)   |                       | 80                             | V    |
| V <sub>IN</sub> (100 ms)   |                       | 100                            |      |
| V <sub>CC</sub>  |                       | 14.5                           |      |
| V <sub>BST</sub>   | Continuous            | 95                             |      |
|  | 100 ms                | 113.2                          |      |
| V <sub>LX</sub>  |                       | 100                            |      |
| V <sub>BST</sub> - V <sub>LX</sub>                                   |                       | 15                             |      |
| V <sub>REF</sub> R <sub>OSC</sub>                                    |                       | - 0.3 to V <sub>CC</sub> + 0.3 |      |
| Logic Inputs   |                       | - 0.3 to V <sub>CC</sub> + 0.3 |      |
| Analog Inputs  |                       | - 0.3 to V <sub>CC</sub> + 0.3 |      |
| HV Pre-Regulator Input Current (Continuous)                          |                       | 5                              | mA   |
| Storage Temperature  |                       | - 65 to 150                    | °C   |
| Operating Junction Temperature                                       |                       | 150                            |      |
| Power Dissipation <sup>a</sup>                                       | TSSOP-20 <sup>b</sup> | 850                            | mW   |
|  | MLP65-20 <sup>c</sup> | 2500                           |      |
| Thermal Impedance (θ <sub>JA</sub> )                                 | TSSOP-20              | 75                             | °C/W |
|  | MLP65-20              | 38                             |      |

Notes:

- a. Device Mounted on JEDEC compliant 1S2P test board.
- b. Derate - 14 mW/°C above 25 °C.
- c. Derate - 26 mW/°C above 25 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| <b>RECOMMENDED OPERATING RANGE</b> All voltages referenced to GND = 0 V |  |                              |      |
|---|--|------------------------------|------|
| Parameter   |  | Limit                        | Unit |
| V <sub>IN</sub>   |  | 28 to 75                     | V    |
| V <sub>CC</sub> Operating   |  | 10.5 to 13.2                 |      |
| C <sub>VCC</sub>  |  | ≥ 4.7                        | μF   |
| f <sub>OSC</sub>  |  | 200 to 625                   | kHz  |
| R <sub>OSC</sub>  |  | 22.6 to 72                   |      |
| R <sub>BBM</sub>  |  | 22 to 50                     | μF   |
| C <sub>REF</sub>  |  | 0.1                          |      |
| C <sub>BOOST</sub>  |  | 0.1                          |      |
| Analog Inputs   |  | 0 V to V <sub>CC</sub> - 2 V | V    |
| Digital Inputs  |  | 0 V to V <sub>CC</sub>       |      |
| Reference Voltage Output Current  |  | 0 to 2.5                     | mA   |

| SPECIFICATIONS <sup>a</sup>      |                                  |  |                                  |                   |                   |                  |    |
|----------------------------------|----------------------------------|--|----------------------------------|-------------------|-------------------|------------------|----|
| Parameter                        | Symbol                           | Test Conditions<br>Unless Otherwise Specified<br>$f_{\text{NOM}} = 500 \text{ kHz}$ , $V_{\text{IN}} = 75 \text{ V}$<br>$V_{\text{INDET}} = 7.5 \text{ V}$ ; $10.5 \text{ V} \leq V_{\text{CC}} \leq 13.2 \text{ V}$ | Limits<br>- 40 to 85 °C          |                   |                   | Unit             |    |
|                                  |                                  |  | Min. <sup>b</sup>                | Typ. <sup>c</sup> | Max. <sup>b</sup> |                  |    |
| <b>Reference (3.3 V)</b>         |                                  |  |                                  |                   |                   |                  |    |
| Output Voltage                   | $V_{\text{REF}}$                 | $V_{\text{CC}} = 12 \text{ V}$ , 25 °C Load = 0 mA   | 3.2                              | 3.3               | 3.4               | V                |    |
| Short Circuit Current            | $I_{\text{SREF}}$                | $V_{\text{REF}} = 0 \text{ V}$   |                                  |                   | - 50              | mA               |    |
| Load Regulation                  | dVr/dir                          | $I_{\text{REF}} = 0$ to - 2.5 mA   |                                  | - 30              | - 75              | mV               |    |
| Power Supply Rejection           | PSRR                             | at 100 Hz  |                                  | 60                |                   | dB               |    |
| <b>Oscillator</b>                |                                  |  |                                  |                   |                   |                  |    |
| Accuracy (1 % $R_{\text{OSC}}$ ) |                                  | $R_{\text{OSC}} = 30 \text{ k}\Omega$ , $f_{\text{NOM}} = 500 \text{ kHz}$   | - 20                             |                   | 20                | %                |    |
| Max Frequency <sup>h</sup>       | $F_{\text{MAX}}$                 | $R_{\text{OSC}} = 22.6 \text{ k}\Omega$  | 500                              | 625               | 750               | kHz              |    |
| Foldback Frequency <sup>d</sup>  | $F_{\text{FOBK}}$                | $f_{\text{NOM}} = 500 \text{ kHz}$ , $V_{\text{CS2}} - V_{\text{CS1}} > 150 \text{ mV}$  |                                  | 100               |                   |                  |    |
| <b>Error Amplifier</b>           |                                  |  |                                  |                   |                   |                  |    |
| Input Bias Current               | $I_{\text{BIAS}}$                | $V_{\text{EP}} = 0 \text{ V}$  | - 40                             |                   | - 15              | $\mu\text{A}$    |    |
| Gain                             | $A_{\text{V}}$                   |  |                                  | - 2.2             |                   | V/V              |    |
| Bandwidth                        | BW                               |  |                                  | 5                 |                   | MHz              |    |
| Power Supply Rejection           | PSRR                             | at 100 Hz  |                                  | 60                |                   | dB               |    |
| Slew Rate                        | SR                               |  |                                  | 0.5               |                   | V/ $\mu\text{s}$ |    |
| <b>Current Sense Amplifier</b>   |                                  |  |                                  |                   |                   |                  |    |
| Input Voltage CM Range           | $V_{\text{CM}}$                  | $V_{\text{CS1}} - \text{GND}$ , $V_{\text{CS2}} - \text{GND}$  |                                  | $\pm 150$         |                   | mV               |    |
| Input Amplifier Gain             | $A_{\text{VOL}}$                 |  |                                  | 17.5              |                   | dB               |    |
| Input Amplifier Bandwidth        | BW                               |  |                                  | 5                 |                   | MHz              |    |
| Input Amplifier Offset Voltage   | $V_{\text{OS}}$                  |  |                                  | $\pm 5$           |                   | mV               |    |
| CL_CONT Current                  | $I_{\text{CL\_CONT}}$            | $dV_{\text{CS}} = 0$   |                                  | 120               |                   | $\mu\text{A}$    |    |
|                                  |                                  | $dV_{\text{CS}} = 100 \text{ mV}$  |                                  | 0                 |                   |                  |    |
|                                  |                                  | $dV_{\text{CS}} = 170 \text{ mV}$  |                                  | > 2               |                   |                  | mA |
| Lower Current Limit Threshold    | $V_{\text{TLCL}}$                | $I_{\text{PD}} = I_{\text{PU}} - I_{\text{CL\_CONT}} = 0$<br>See Figure 6  |                                  | 100               |                   | mV               |    |
| Upper Current Limit Threshold    | $V_{\text{THCL}}$                | $I_{\text{PD}} > 2 \text{ mA}$   |                                  | 150               |                   |                  |    |
| Hysteresis                       |                                  | $I_{\text{PU}} < 500 \mu\text{A}$  |                                  | - 50              |                   |                  |    |
| CL_CONT Clamp Level              | $C_{\text{L\_CONT}}(\text{min})$ | $I_{\text{PU}} = 500 \mu\text{A}$  | 0.6                              |                   | 1.5               | V                |    |
| <b>PWM Operation</b>             |                                  |  |                                  |                   |                   |                  |    |
| Duty Cycle <sup>e</sup>          | $D_{\text{MAX}}$                 | $f_{\text{OSC}} = 500 \text{ kHz}$<br>$V_{\text{CS2}} - V_{\text{CS1}} > 150 \text{ mV}$   | $V_{\text{EP}} = 0 \text{ V}$    | 90                | 92                | 95               | %  |
|                                  | $D_{\text{MIN}}$                 |  | $V_{\text{EP}} = 1.75 \text{ V}$ |                   | < 15              |                  |    |
| <b>Pre-Regulator</b>             |                                  |  |                                  |                   |                   |                  |    |
| Input Voltage                    | $+ V_{\text{IN}}$                | $I_{\text{IN}} = 10 \mu\text{A}$   | 28                               |                   | 75                | V                |    |
| Input Leakage Current            | $I_{\text{LKG}}$                 | $V_{\text{IN}} = 75 \text{ V}$ , $V_{\text{CC}} > V_{\text{REG}}$  |                                  |                   | 10                | $\mu\text{A}$    |    |
| Regulator Bias Current           | $I_{\text{REG1}}$                | $V_{\text{IN}} = 75 \text{ V}$ , $V_{\text{INDET}} < V_{\text{SD}}$  |                                  | 86                | 200               |                  |    |
|                                  | $I_{\text{REG2}}$                | $V_{\text{IN}} = 75 \text{ V}$ , $V_{\text{INDET}} > V_{\text{REF}}$   |                                  | 8                 | 14                | mA               |    |
| Regulator_Comp                   | $I_{\text{SOURCE}}$              | $V_{\text{CC}} = 12 \text{ V}$   | - 29                             | - 19              | - 9               | $\mu\text{A}$    |    |
|                                  | $I_{\text{SINK}}$                |  | 50                               | 82                | 110               |                  |    |
| Pre-Regulator Drive Capacity     | $I_{\text{START}}$               | $V_{\text{CC}} < V_{\text{REG}}$   | 20                               |                   |                   | mA               |    |



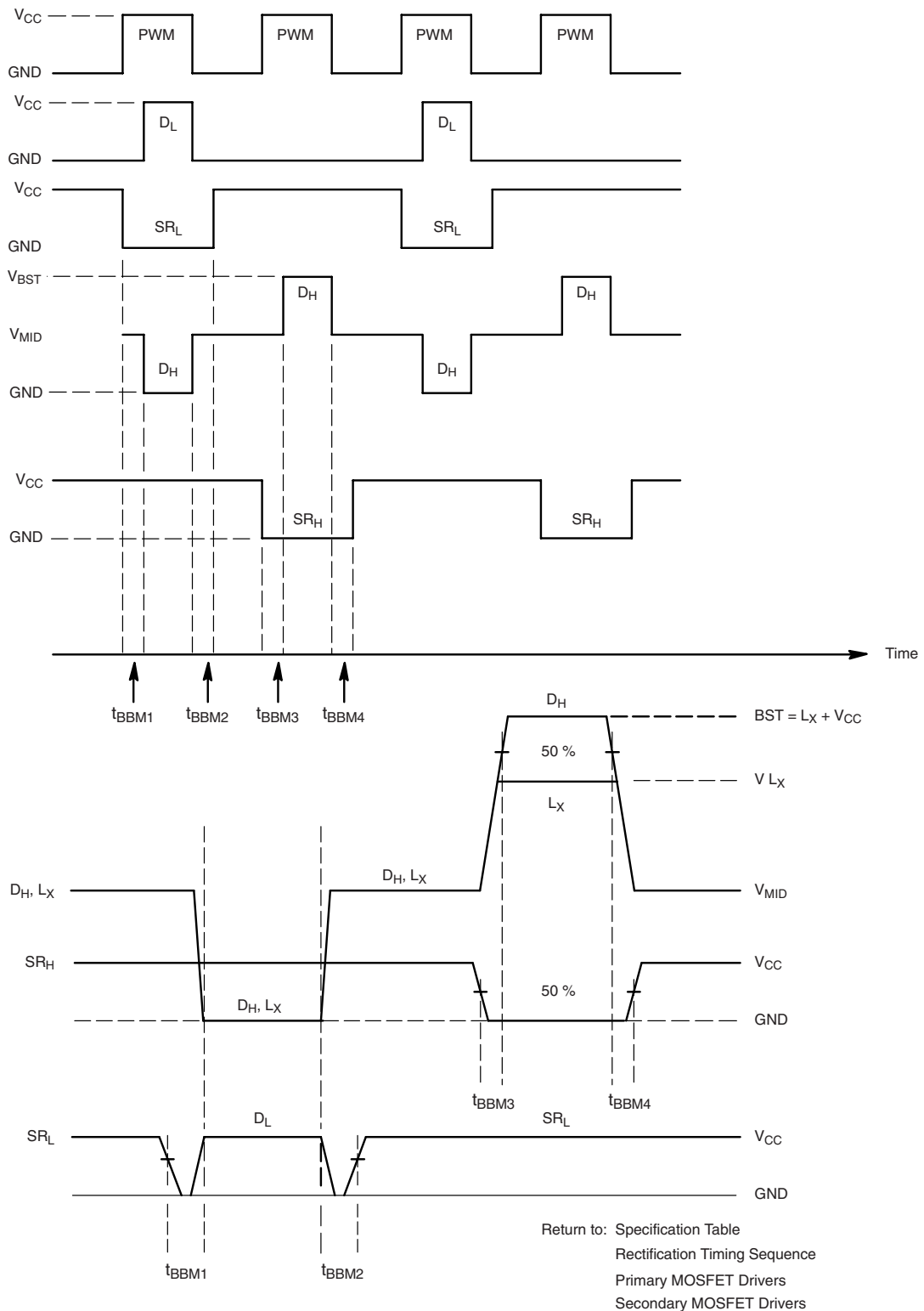
| <b>SPECIFICATIONS<sup>a</sup></b>                      |                |  |                         |                   |                   |               |     |
|--|----------------|--|-------------------------|-------------------|-------------------|---------------|-----|
| Parameter  | Symbol         | Test Conditions<br>Unless Otherwise Specified<br>$f_{NOM} = 500 \text{ kHz}$ , $V_{IN} = 75 \text{ V}$<br>$V_{INDET} = 7.5 \text{ V}$ ; $10.5 \text{ V} \leq V_{CC} \leq 13.2 \text{ V}$ | Limits<br>- 40 to 85 °C |                   |                   | Unit          |     |
|  |                |  | Min. <sup>b</sup>       | Typ. <sup>c</sup> | Max. <sup>b</sup> |               |     |
| <b>Pre-Regulator</b>                                   |                |  |                         |                   |                   |               |     |
| $V_{CC}$ Pre-Regulator Turn Off Threshold Voltage      | $V_{REG1}$     | $V_{INDET} > V_{REF}$  | 7.4                     | 9.1               | 10.4              | V             |     |
|  | $V_{REG2}$     | $V_{INDET} = 0 \text{ V}$  | 8.5                     | 9.1               | 9.7               |               |     |
| Undervoltage Lockout                                   | $V_{UVLO}$     | $V_{CC}$ Rising  | $T_A = 25 \text{ °C}$   | 7.15              | 8.8               |               | 9.8 |
|  |                |  | $T_A = 25 \text{ °C}$   | 8.1               | 8.8               |               | 9.3 |
| $V_{UVLO}$ Hysteresis <sup>9</sup>                     | $V_{UVLOHYS}$  |  |                         | 0.5               |                   |               |     |
| <b>Soft-Start</b>                                      |                |  |                         |                   |                   |               |     |
| Soft-Start Current Output                              | $I_{SS}$       | Start-Up Condition   | 12                      | 20                | 28                | $\mu\text{A}$ |     |
| Soft-Start Completion Voltage                          | $V_{SS\_COMP}$ | Normal Operation   | 7.35                    | 8.05              | 8.85              | V             |     |
| <b>Shutdown</b>  |                |  |                         |                   |                   |               |     |
| $V_{INDET}$ Shutdown                                   | $V_{SD}$       | $V_{INDET}$ Rising   | 350                     | 550               | 720               | mV            |     |
| $V_{SD}$ Hysteresis                                    |                | $V_{INDET}$  |                         | 200               |                   |               |     |
| <b><math>V_{INDET}</math> Input Threshold Voltages</b> |                |  |                         |                   |                   |               |     |
| $V_{INDET} - V_{IN}$ Under Voltage                     | $V_{UV}$       | $V_{INDET}$ Rising   | 3.13                    | 3.3               | 3.46              | V             |     |
| $V_{UV}$ Hysteresis                                    |                | $V_{INDET}$  | 0.23                    | 0.3               | 0.35              |               |     |
| <b>Over Temperature Protection</b>                     |                |  |                         |                   |                   |               |     |
| Activating Temperature                                 |                | $T_J$ Increasing   |                         | 160               |                   | °C            |     |
| De-Activating Temperature                              |                | $T_J$ Decreasing   |                         | 130               |                   |               |     |
| <b>Converter Supply Current (<math>V_{CC}</math>)</b>  |                |  |                         |                   |                   |               |     |
| Shutdown   | $I_{CC1}$      | Shutdown, $V_{INDET} = 0 \text{ V}$  | 50                      |                   | 350               | $\mu\text{A}$ |     |
| Switching Disabled                                     | $I_{CC2}$      | $V_{INDET} < V_{REF}$  | 4                       | 8                 | 12                | mA            |     |
| Switching w/o Load                                     | $I_{CC3}$      | $V_{INDET} > V_{REF}$ , $f_{NOM} = 500 \text{ kHz}$  | 5                       | 10                | 15                |               |     |
| Switching with $C_{LOAD}$                              | $I_{CC4}$      | $V_{CC} = 12 \text{ V}$ , $C_{DH} = C_{DL} = 3 \text{ nF}$<br>$C_{SRH} = C_{SRL} = 0.3 \text{ nF}$   |                         | 21                |                   |               |     |
| <b>Output MOSFET DH Driver (High-Side)</b>             |                |  |                         |                   |                   |               |     |
| Output High Voltage                                    | $V_{OH}$       | Sourcing 10 mA   | $V_{BST} - 0.3$         |                   |                   | V             |     |
| Output Low Voltage                                     | $V_{OL}$       | Sinking 10 mA  |                         |                   | $V_{LX} + 0.3$    |               |     |
| Boost Current  | $I_{BST}$      | $V_{LX} = 75 \text{ V}$ , $V_{BST} = V_{LX} + V_{CC}$  | 1.3                     | 1.9               | 2.7               | mA            |     |
| $L_X$ Current  | $I_{LX}$       | $V_{LX} = 75 \text{ V}$ , $V_{BST} = V_{LX} + V_{CC}$  | - 1.3                   | - 0.7             | - 0.4             |               |     |
| Peak Output Source                                     | $I_{SOURCE}$   | $V_{CC} = 10.5 \text{ V}$  |                         | - 1.0             | - 0.75            | A             |     |
| Peak Output Sink                                       | $I_{SINK}$     |  | 0.75                    | 1.0               |                   |               |     |
| Rise Time  | $t_r$          | $C_{DH} = 3 \text{ nF}$  |                         | 35                |                   | ns            |     |
| Fall Time  | $t_f$          |  |                         | 35                |                   |               |     |
| <b>Output MOSFET DL Driver (Low-Side)</b>              |                |  |                         |                   |                   |               |     |
| Output High Voltage                                    | $V_{OH}$       | Sourcing 10 mA   | $V_{CC} - 0.3$          |                   |                   | V             |     |
| Output Low Voltage                                     | $V_{OL}$       | Sinking 10 mA  |                         |                   | 0.3               |               |     |
| Peak Output Source                                     | $I_{SOURCE}$   | $V_{CC} = 10.5 \text{ V}$  |                         | - 1.0             | - 0.75            | A             |     |
| Peak Output Sink                                       | $I_{SINK}$     |  | 0.75                    | 1.0               |                   |               |     |
| Rise Time  | $t_r$          | $C_{DL} = 3 \text{ nF}$  |                         | 35                |                   | ns            |     |
| Fall Time  | $t_f$          |  |                         | 35                |                   |               |     |

| SPECIFICATIONS <sup>a</sup>                     |              |  |                         |                   |                   |      |
|---|--------------|--|-------------------------|-------------------|-------------------|------|
| Parameter                                       | Symbol       | Test Conditions<br>Unless Otherwise Specified<br>$f_{NOM} = 500 \text{ kHz}$ , $V_{IN} = 75 \text{ V}$<br>$V_{INDET} = 7.5 \text{ V}$ ; $10.5 \text{ V} \leq V_{CC} \leq 13.2 \text{ V}$ | Limits<br>- 40 to 85 °C |                   |                   | Unit |
|   |              |  | Min. <sup>b</sup>       | Typ. <sup>c</sup> | Max. <sup>b</sup> |      |
| <b>Synchronous Rectifier (SRH, SRL) Drivers</b> |              |  |                         |                   |                   |      |
| Output High Voltage                             | $V_{OH}$     | Sourcing 10 mA   | $V_{CC} - 0.4$          |                   |                   | V    |
| Output Low Voltage                              | $V_{OL}$     | Sinking 10 mA  |                         |                   | 0.4               |      |
| Break-Before-Make Time <sup>f</sup>             | $t_{BBM1}$   | $T_A = 25 \text{ °C}$ , $R_{BBM} = 33 \text{ k}\Omega$ , See Figure 3  |                         | 55                |                   | ns   |
|   | $t_{BBM2}$   |  |                         | 40                |                   |      |
|   | $t_{BBM3}$   | $T_A = 25 \text{ °C}$ , $R_{BBM} = 33 \text{ k}\Omega$ , $L_X = 75 \text{ V}$  |                         | 35                |                   |      |
|   | $t_{BBM4}$   |  |                         | 55                |                   |      |
| Peak Output Source                              | $I_{SOURCE}$ | $V_{CC} = 10.5 \text{ V}$  |                         | - 100             |                   | mA   |
| Peak Output Sink                                | $I_{SINK}$   |  |                         | 100               |                   |      |
| Rise Time                                       | $t_r$        | $C_{SRH} = C_{SRL} = 0.3 \text{ nF}$   |                         | 35                |                   | ns   |
| Fall Time                                       | $t_f$        |  |                         | 35                |                   |      |
| <b>Voltage Mode</b>                             |              |  |                         |                   |                   |      |
| Error Amplifier                                 | $t_{d1DH}$   | Input to High-Side Switch Off  |                         | < 200             |                   | ns   |
|   | $t_{d2DL}$   | Input to Low-Side Switch Off   |                         | < 200             |                   |      |
| <b>Current Mode</b>                             |              |  |                         |                   |                   |      |
| Current Amplifier                               | $t_{d3DH}$   | Input to High-Side Switch Off  |                         | < 200             |                   | ns   |
|   | $t_{d4DL}$   | Input to Low-Side Switch Off   |                         | < 200             |                   |      |

## Notes:

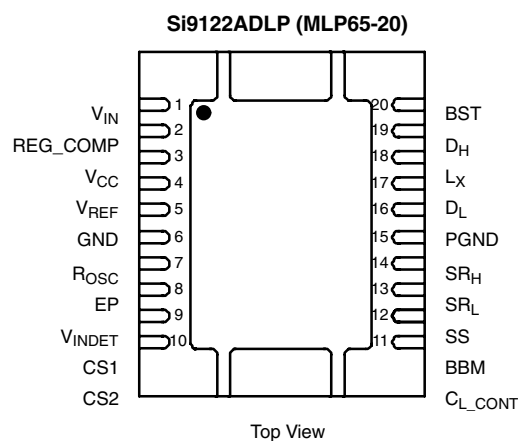
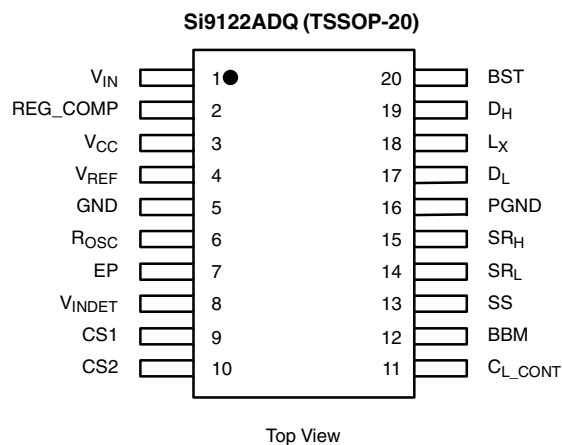
- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum (- 40 °C to 85 °C).
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- $F_{MIN}$  when  $V_{CL\_CONT}$  at clamp level. Typical foldback frequency change + 20 %, - 30 % over temperature.
- Measured on SRL or SRH outputs.
- See figure 3 for Break-Before-Make time definition.
- $V_{UVLO}$  tracks  $V_{REG1}$  by a diode drop.
- Guaranteed by design and characterization, not tested in production.

**TIMING DIAGRAM FOR MOS DRIVERS**



**Figure 3.**

## PIN CONFIGURATION



## ORDERING INFORMATION

| Part Number      | Temperature Range | Package  |
|------------------|-------------------|----------|
| Si9122ADQ-T1-E3  | - 40 °C to 85 °C  | TSSOP-20 |
| Si9122ADLP-T1-E3 |                   | MLP65-20 |

| Eval Board      | Temperature Range | Board Type                  |
|-----------------|-------------------|-----------------------------|
| Contact Factory | - 10 °C to 70 °C  | Surface Mount and Thru-Hole |

## PIN DESCRIPTION

| Pin Number | Name            | Function  |
|------------|-----------------|---|
| 1          | $V_{IN}$        | Input supply voltage for the start-up circuit   |
| 2          | REG_COMP        | Control signal for an external pass transistor  |
| 3          | $V_{CC}$        | Supply voltage for internal circuitry   |
| 4          | $V_{REF}$       | 3.3 V reference   |
| 5          | GND             | Ground  |
| 6          | $R_{OSC}$       | External resistor connection to oscillator  |
| 7          | EP              | Voltage control input   |
| 8          | $V_{INDET}$     | $V_{IN}$ under voltage detect and shutdown function input. Shuts down or disables switching when $V_{INDET}$ falls below preset threshold voltages and provides the feed forward voltage. |
| 9          | CS1             | Current limit amplifier negative input  |
| 10         | CS2             | Current limit amplifier positive input  |
| 11         | $C_{L\_CONT}$   | Current limit compensation  |
| 12         | BBM             | Programmable break-before-make time connection to an external resistor to set time delay  |
| 13         | SS              | Soft-start control - external capacitor connection  |
| 14         | SR <sub>L</sub> | Signal transformer drive, sequenced with the primary side   |
| 15         | SR <sub>H</sub> | Signal transformer drive, sequenced with the primary side   |
| 16         | PGND            | Power ground.   |
| 17         | DL              | Low-side gate drive signal - primary  |
| 18         | L <sub>X</sub>  | High-side source and transformer connection node  |
| 19         | D <sub>H</sub>  | High-side gate drive signal - primary   |
| 20         | BST             | Bootstrap voltage to drive the high-side N-Channel MOSFET switch  |



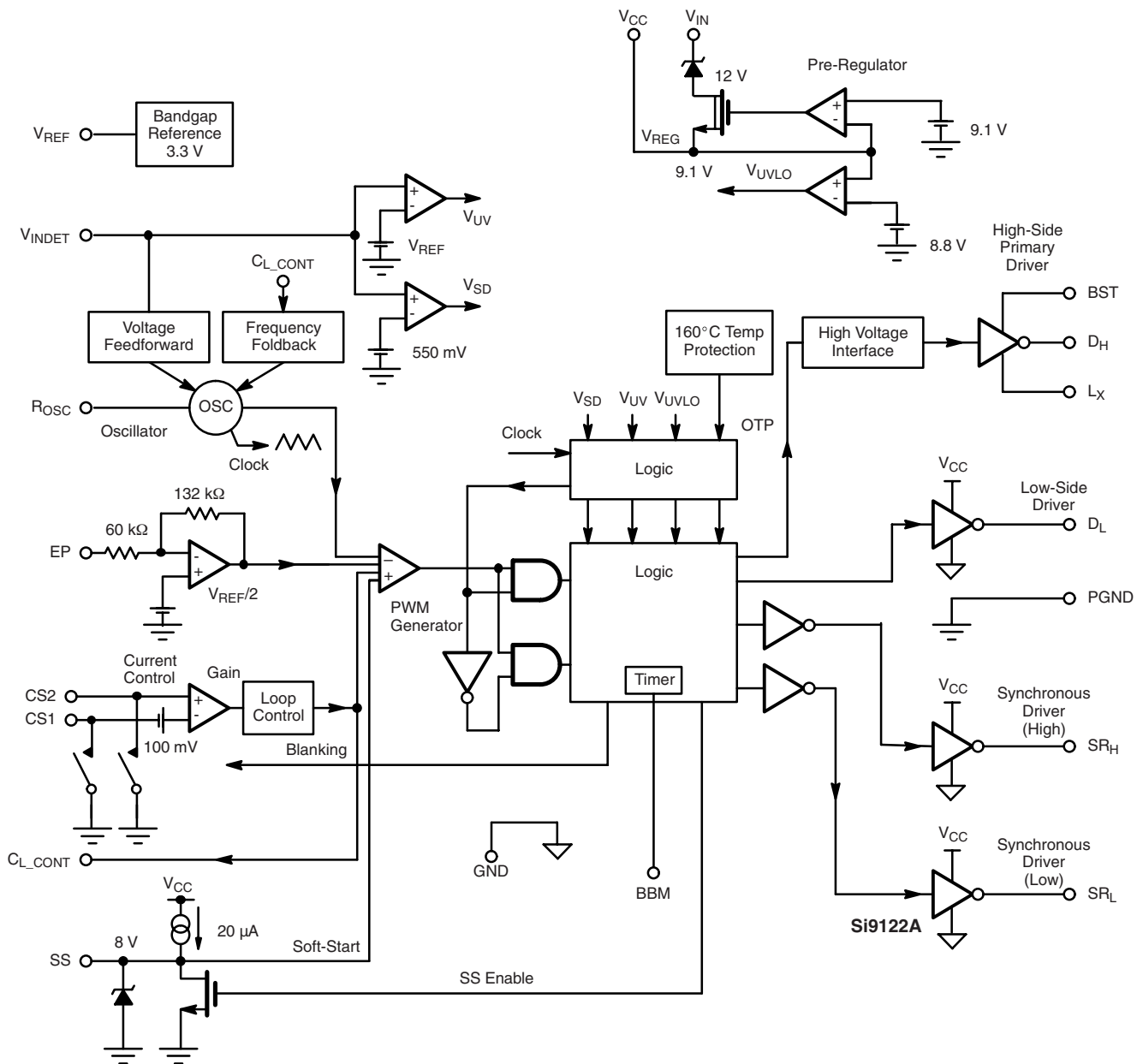


Figure 4. Detailed Si9122A Block Diagram

## DETAILED OPERATION

### Start-Up

When  $V_{INEXT}$  rises above 0 V, the internal pre-regulator begins to charge up the  $V_{CC}$  capacitor. Current into the external  $V_{CC}$  capacitor is limited to typically 40 mA by the internal DMOS device. When  $V_{CC}$  exceeds the UVLO voltage of 8.8 V a soft-start cycle of the switch mode supply is initiated. The  $V_{CC}$  supply continues to be charged by the pre-regulator until  $V_{CC}$  equals  $V_{REG}$ . During this period, between  $V_{UVLO}$  and  $V_{REG}$ , excessive load current will result in  $V_{CC}$  falling below  $V_{UVLO}$  and stopping switch mode operation. This situation is avoided by the hysteresis between  $V_{REG}$  and  $V_{UVLO}$  and correct sizing of the  $V_{CC}$

capacitor, bootstrap capacitor and the soft-start capacitor. The value of the  $V_{CC}$  capacitor should therefore be chosen to be capable of maintaining switch mode operation until the required  $V_{CC}$  current can be supplied from the external circuit (e.g via a power transformer winding and zener regulator). Feedback from the output of the switch mode supply charges  $V_{CC}$  above  $V_{REG}$  and fully disconnects the pre-regulator, isolating  $V_{CC}$  from  $V_{IN}$ .  $V_{CC}$  is then maintained above  $V_{REG}$  for the duration of switch mode operation. In the event of an over voltage condition on  $V_{CC}$ , an internal voltage clamp turns on at 14.5 V to shunt excessive current to GND.

Care needs to be taken if there is a delay prior to the external circuit feeding back to the  $V_{CC}$  supply. To prevent excessive power dissipation within the IC it is advisable to use an external PNP device. A pin has been incorporated on the IC, (REG\_COMP) to provide compensation when employing the external device. In this case the  $V_{IN}$  pin is connected to the base of the PNP device and controls the current, while the REG\_COMP pin determines the frequency compensation of the circuit. The value of the REG\_COMP capacitor cannot be too big, otherwise it will slow down the response of the pre-regulator in the case that fault situations occur and pre-regulator needs to be turned on again. To understand the operation please refer to Figure 5.

The soft-start circuit is designed for the dc-dc converter to start-up in an orderly manner and reduce component stress on the IC. This feature is programmable by selecting an external  $C_{SS}$ . An internal 20  $\mu$ A current source charges  $C_{SS}$  from 0 V to the final clamped voltage of 8 V. In the event of UVLO or shutdown,  $V_{SS}$  will be held low (< 1 V) disabling driver switching. To prevent oscillations, a longer soft-start time may be needed for highly capacitive loads and/or high peak output current applications.

#### Reference

The reference voltage of Si9122A is set at 3.3 V. The reference voltage should be de-coupled externally with 0.1  $\mu$ F capacitor. The  $V_{REF}$  voltage is 0 V in shutdown mode and has 50 mA source capability.

#### Voltage Mode PWM Operation

Under normal load conditions, the IC operates in voltage mode and generates a fixed frequency pulse width modulated signal to the drivers. Duty cycle is controlled over a wide range to maintain output voltage under line and load variation. Voltage feed forward is also included to take account of variations in supply voltage  $V_{IN}$ .

In the half-bridge topology requiring isolation between output and input, the reference voltage and error amplifier must be supplied externally, usually on the secondary side. The error information is thus passed to the power controller through an opto-coupling device. This information is inverted, hence 0 V represents the maximum duty cycle, whilst 2 V represents minimum duty cycle. The error information enters the IC via pin EP, and is passed to the PWM generator via an inverting amplifier. The relationship between duty cycle and  $V_{EP}$  is shown in the typical characteristic Graph, duty cycle vs.  $V_{EP}$  25 °C, page 11. Voltage feedforward is implemented by taking the attenuated  $V_{IN}$  signal at  $V_{INDET}$  and directly modulating the duty cycle.

At start-up, i.e., once  $V_{CC}$  is greater than  $V_{UVLO}$ , switching is initiated under soft-start control which increases primary switch on-times linearly from  $D_{MIN}$  to  $D_{MAX}$  over the soft-start period. Start-up from a  $V_{INDET}$  power down is also initiated under soft-start control.

#### Half-Bridge and Synchronous Rectification Timing Sequence

The PWM signal generated within the Si9122A controls the low and high-side bridge drivers on alternative cycles. A period of inactivity always results after initiation of the soft-start cycle until the soft-start voltage reaches approximately 1.2 V and PWM controlled switching begins. The first bridge driver to switch is always the low-side ( $D_L$ ), as this allows charging of the high-side boost capacitor.

The timing and coordination of the drives to the primary and secondary stages is very important and shown in figure 3. It is essential to avoid the situation where both of the secondary MOSFETs are on when either the high or the low-side switch are active. In this situation the transformer would effectively be presented with a short across the output. To avoid this, a dedicated break-before-make circuit is included which will generate non overlapping waveforms for the primary and the secondary drive signals. This is achieved by a programmable timer which delays the switching on of the primary driver relative to the switching off of the related secondary and subsequently delays the switching on of the secondary relative to the switching off of the related primary.

Typical variations of BBM times with respect to  $R_{BBM}$  and other operating parameters are shown on page 13 and 14.

#### Primary High- and Low-Side MOSFET Drivers

The drive voltage for the low-side MOSFET switch is provided directly from  $V_{CC}$ . The high-side MOSFET however requires the gate voltage to be enhanced above  $V_{IN}$ . This is achieved by bootstrapping the  $V_{CC}$  voltage onto the  $L_X$  voltage (the high-side MOSFET source). In order to provide the bootstrapping an external diode and capacitor are required as shown on the application schematic. The capacitor will charge up after the low-side driver has turned on. The switch gate drive signals  $D_H$  and  $D_L$  are shown in figure 3.

#### Secondary MOSFET Drivers

The secondary side MOSFETs are driven from the Si9122A via a center tapped pulse transformer and inverter drivers. The waveforms from SRH and SRL are shown in figure 3. Of importance is the relative voltage between SRH and SRL, i.e. that which is presented across the primary of the pulse transformer. When both potentials of SRL and SRH are equal then by the action of the inverting drivers both secondary MOSFETs are turned on.

#### Oscillator

The oscillator is designed to operate at a nominal frequency of 500 kHz. The 500 kHz operating frequency allows the converter to minimize the inductor and capacitor size, improving the power density of the converter. The oscillator and therefore the switching frequency is programmable by attaching a resistor to the  $R_{OSC}$  pin. Under overload conditions the oscillator frequency is reduced by the current overload protection to enable a constant current to be maintained into a low impedance circuit.

## Current Limit

Current mode control providing constant current operation is achieved by monitoring the differential voltage  $V_{CS}$  between the CS1 and CS2 pins, which are connected to a current sense resistor on the primary low-side MOSFET. In the absence of an overcurrent condition,  $V_{CS}$  is less than lower current limit threshold  $V_{TLCL}$  (typical 100 mV);  $C_{L\_CONT}$  is pulled up linearly via the 120  $\mu\text{A}$  current source ( $I_{PU}$ ) and both DL and DH switch at half the oscillator set frequency. When a moderate overcurrent condition occurs ( $V_{TLCL} < V_{CS} < V_{THCL}$ ), the  $C_{L\_CONT}$  capacitor will be discharged at a rate that is proportional to  $V_{CS} - 100$  mV by the  $I_{PD}$  current source. Both driver outputs are in frequency fold-back mode and the switching frequency becomes roughly 20 % of normal switching frequency. When a severe overcurrent condition occurs ( $V_{THCL} < V_{CS}$ ), the NMOS discharges  $C_{L\_CONT}$  capacitor immediately at 2 mA rate and the  $C_{L\_CONT}$  voltage will be clamped to 1.2 V disabling both DL and DH outputs.

Before  $V_{CS}$  reaches severe overcurrent condition, a lowering of the  $C_{L\_CONT}$  voltage results in PWM control of the output drive being taken over by the current limit control loop through  $C_{L\_CONT}$ . Current control initially reduces the switching duty cycle toward the minimum the chip can reach ( $D_{MIN}$ ). If this duty cycle reduction still cannot lower the load current, then the switching frequency will start to fold back to minimum 1/5 of the nominal frequency. This prevents the on-time of the primary drivers from being reduced to below 100 ns and avoids current tails. If  $V_{CS} > V_{THCL}$ , the switching will then stop.

With constant current mode control and frequency foldback protection of the MOSFET switches is increased. The converter reverts to voltage mode operation immediately when the primary current falls below the limit level, and  $C_{L\_CONT}$  capacitor is charged up and clamped to 6.5 V. The soft-start function does not apply during current limit period, as this would constitute hiccup mode operation.

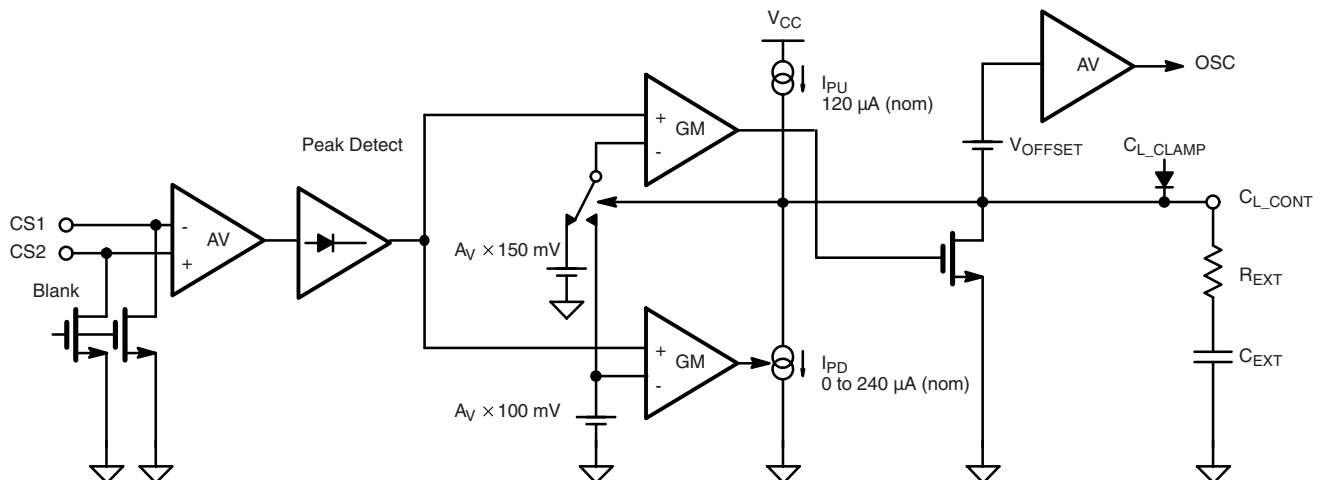


Figure 6 . Current Limit Circuit

## $V_{IN}$ Voltage Monitor - $V_{INDET}$

The chip provides a means of sensing the voltage of  $V_{IN}$ , and withholding operation of the output drivers until a minimum voltage of  $V_{REF}$  (3.3 V, 300 mV hysteresis), is achieved. This is achieved by choosing an appropriate resistive tap between the ground and  $V_{IN}$ , and comparing this voltage with the reference voltage. When the applied voltage is greater than  $V_{REF}$ , the output drivers are activated as normal.  $V_{INDET}$  also provides the input to the voltage feed forward function.

However, if the divided voltage applied to the  $V_{INDET}$  pin is greater than  $V_{CC} - 0.3$  V, the high-side driver,  $D_H$ , will stop switching until the voltage drops below  $V_{CC} - 0.3$  V. Thus, the resistive tap on the  $V_{IN}$  divider must be set to accommodate the normal  $V_{CC}$  operating voltage to avoid this condition. Alternatively, a zener clamp diode from  $V_{INDET}$  to GND may also be used.

## Shutdown Mode

If  $V_{INDET}$  is forced below the lower  $V_{SD}$  threshold, the device will enter SHUTDOWN mode. This powers down all unnecessary functions of the controller, ensures that the primary switches are off, and results in a low level current demand from the  $V_{IN}$  or  $V_{CC}$  supplies.

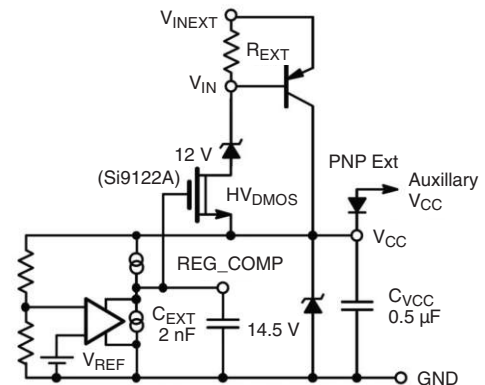
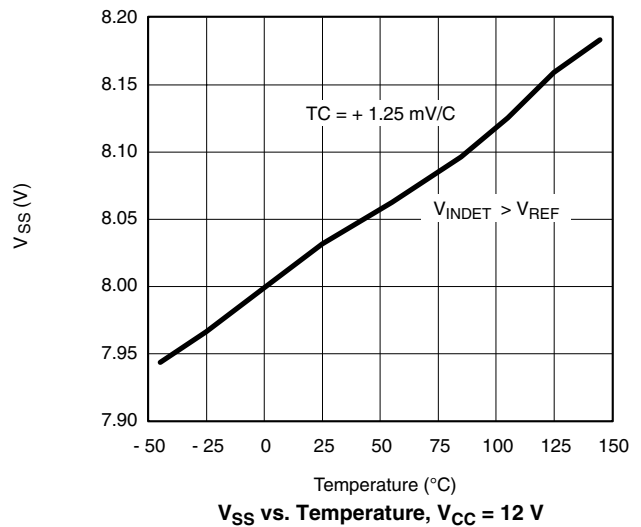
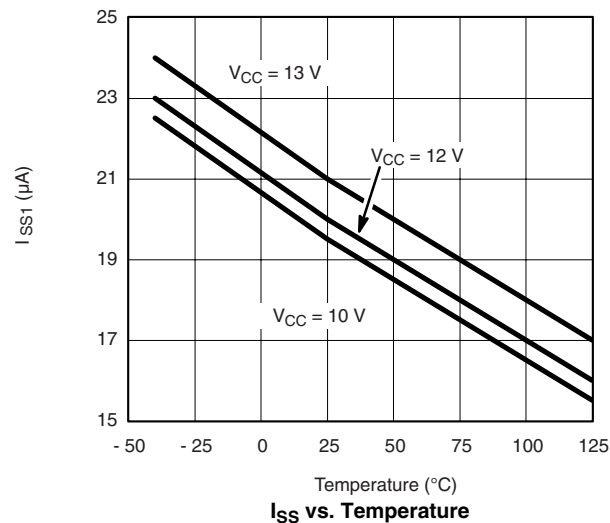
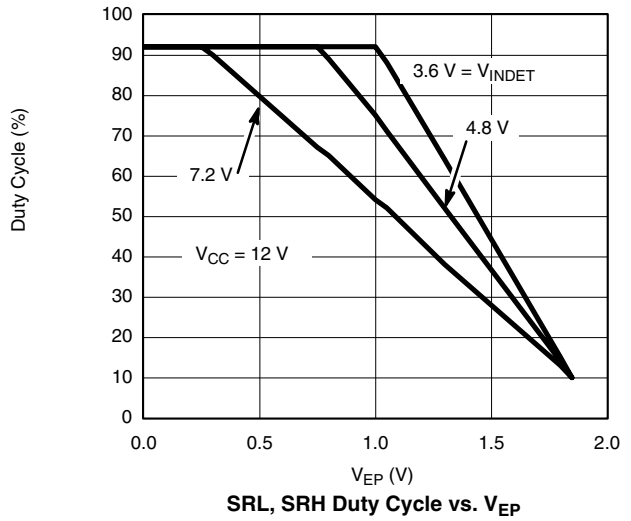
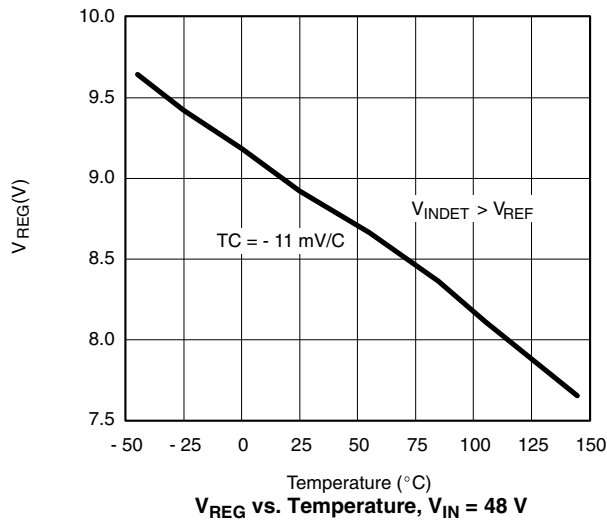
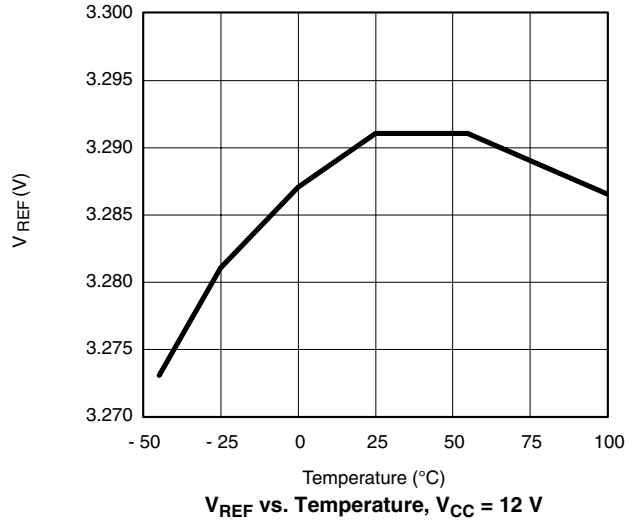
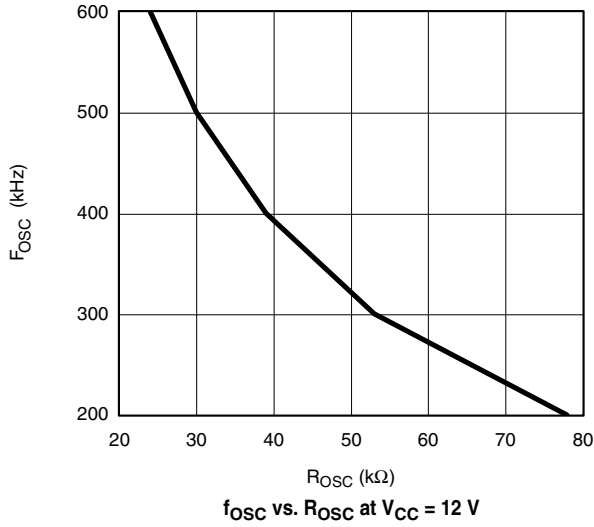
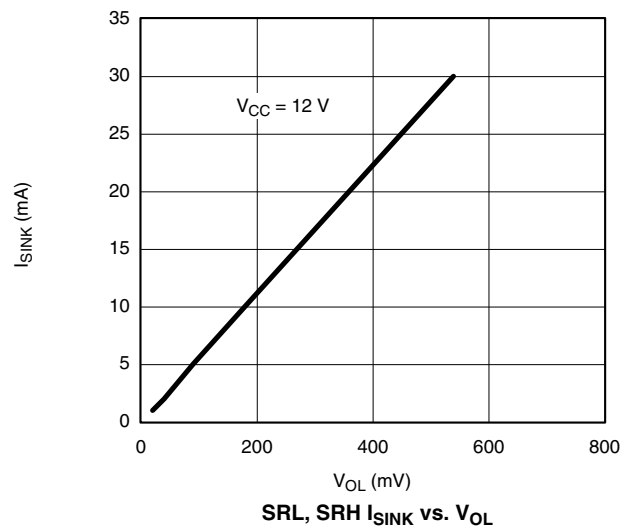
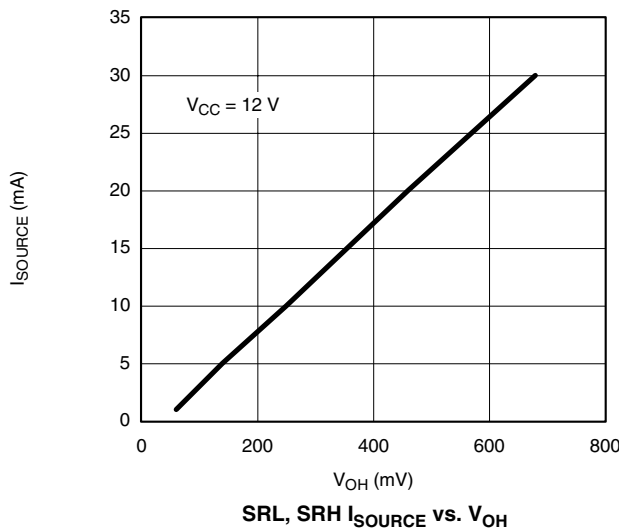
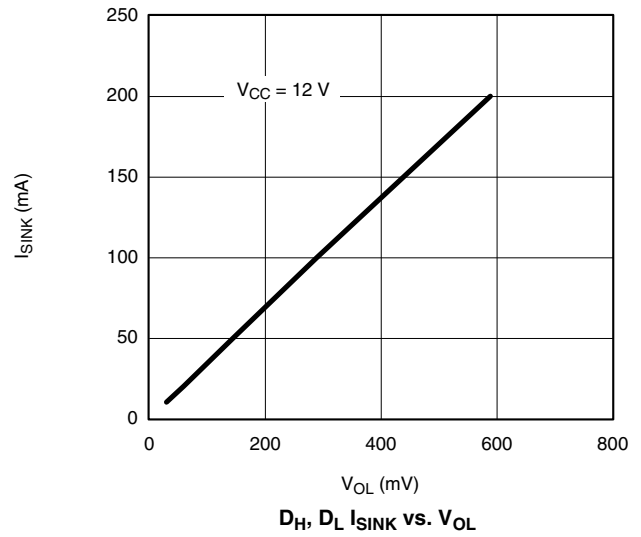
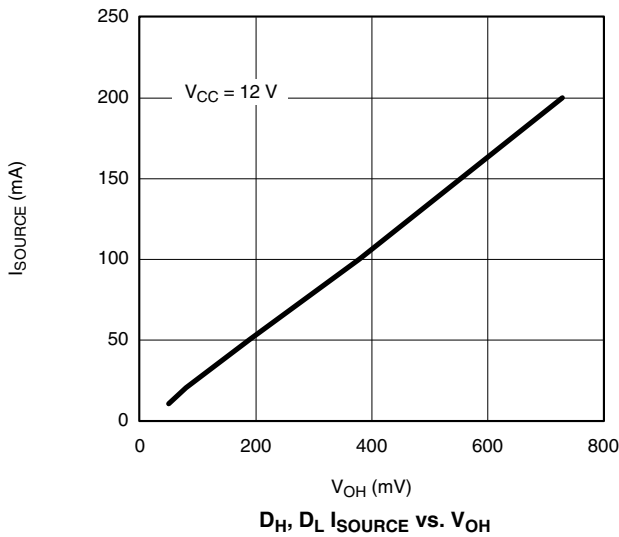
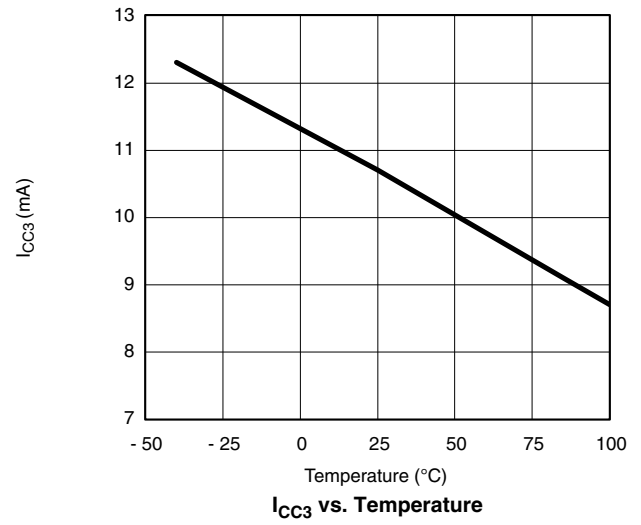
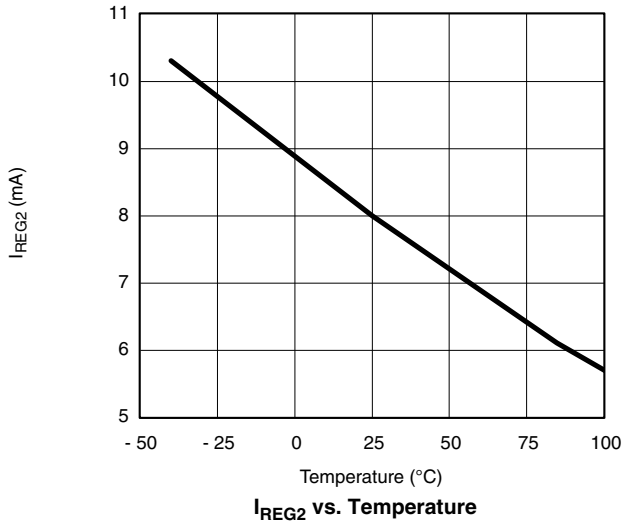


Figure 5. High-Voltage Pre-Regulator Circuit

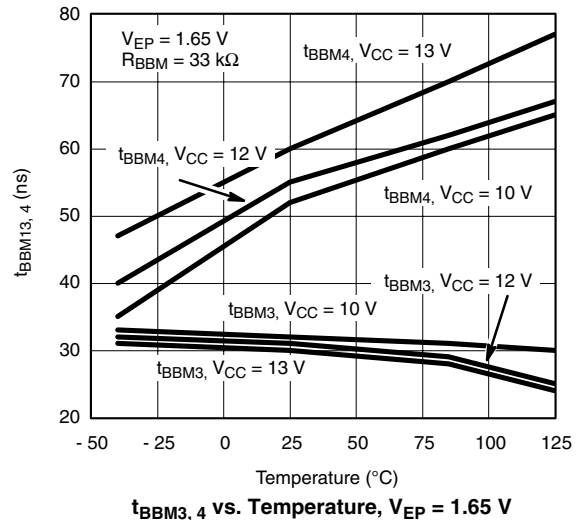
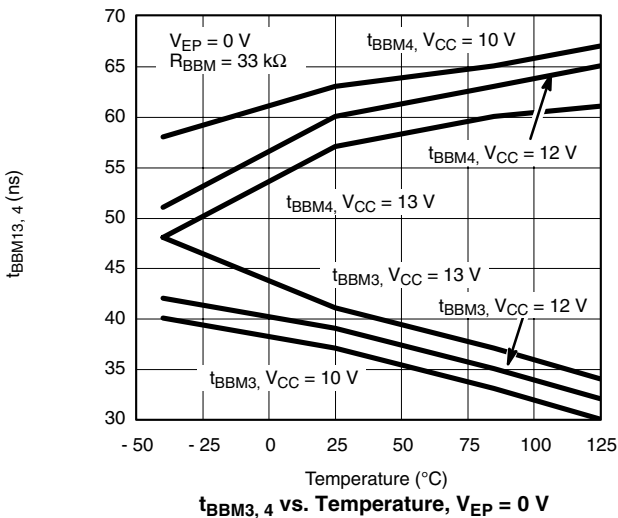
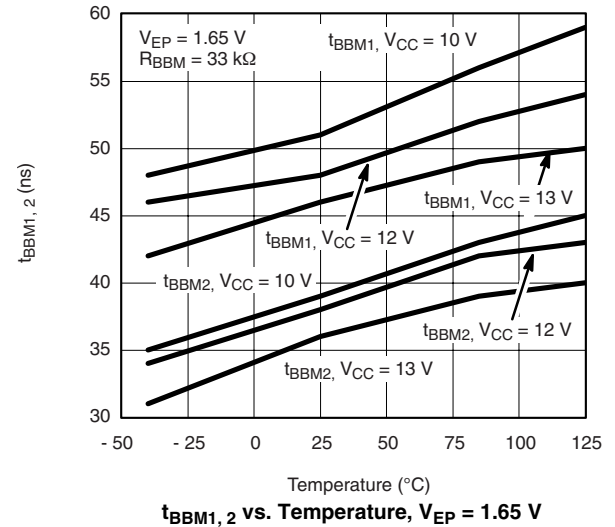
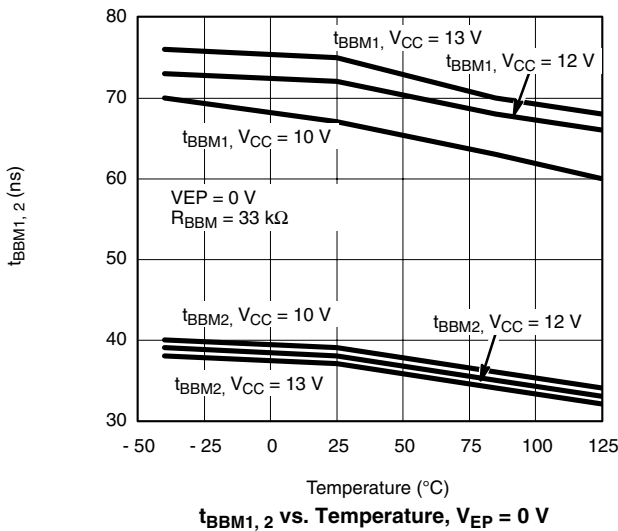
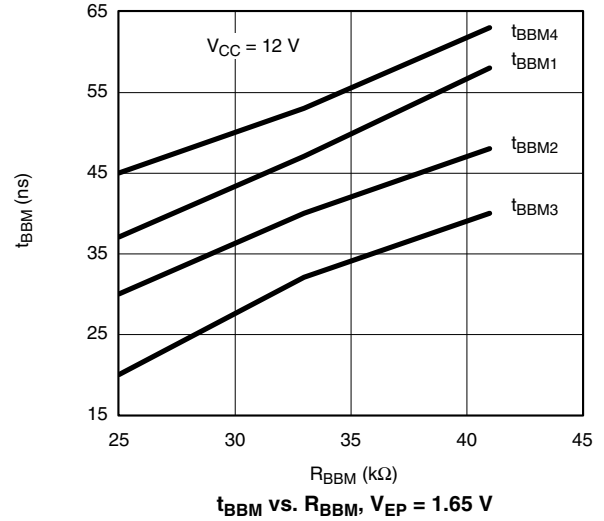
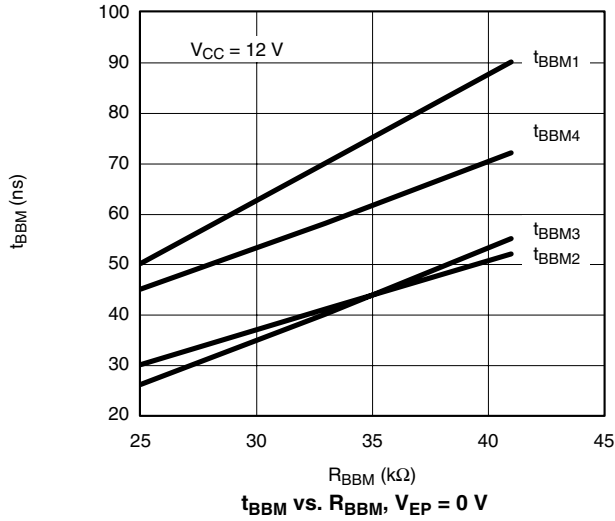
## TYPICAL CHARACTERISTICS



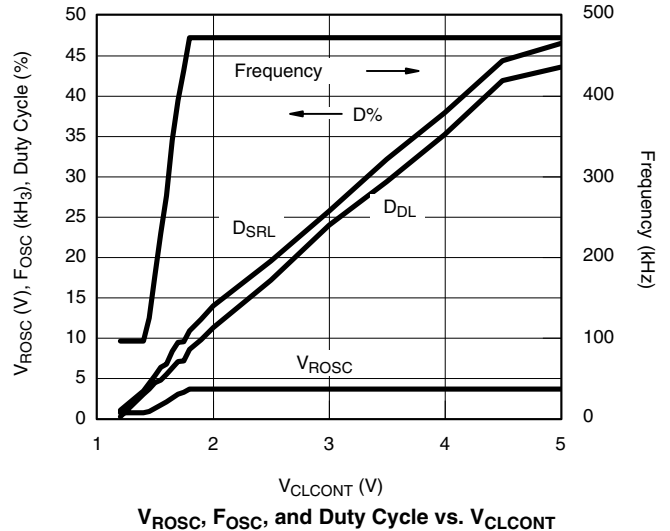
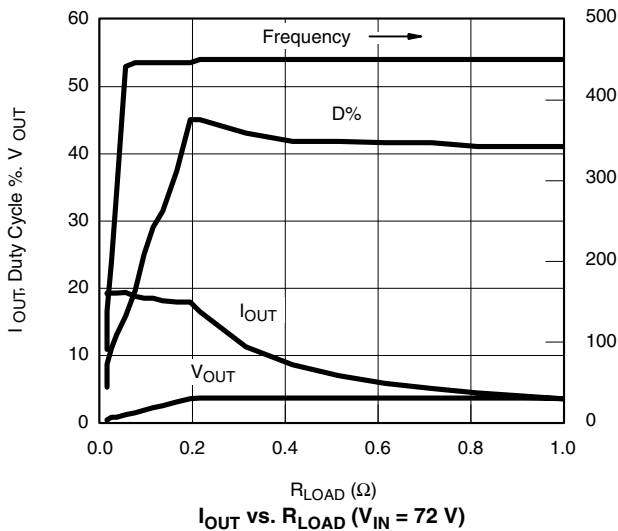
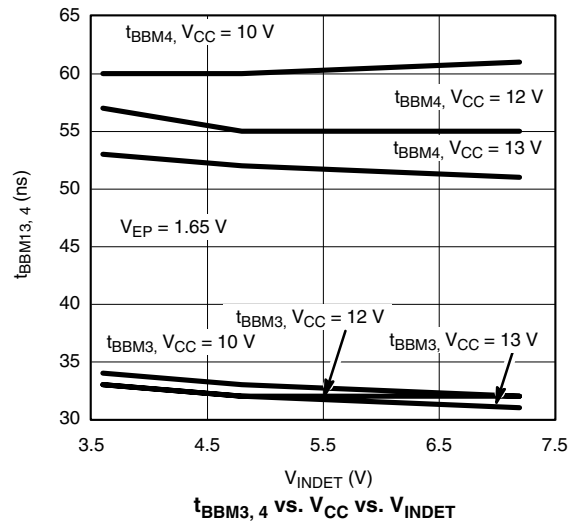
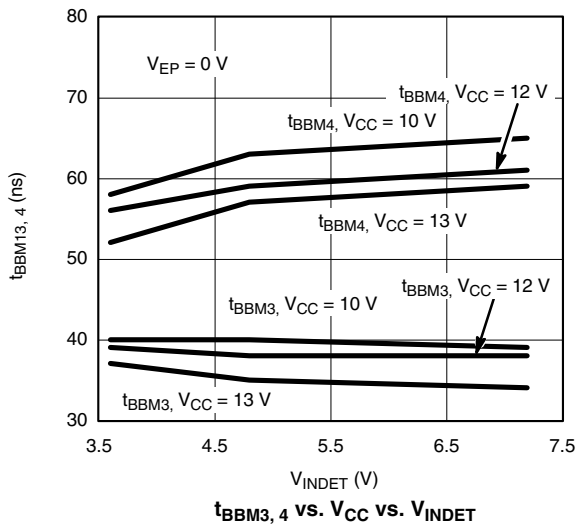
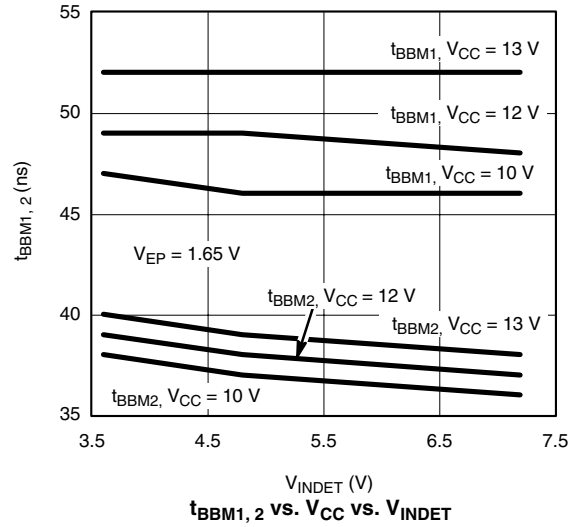
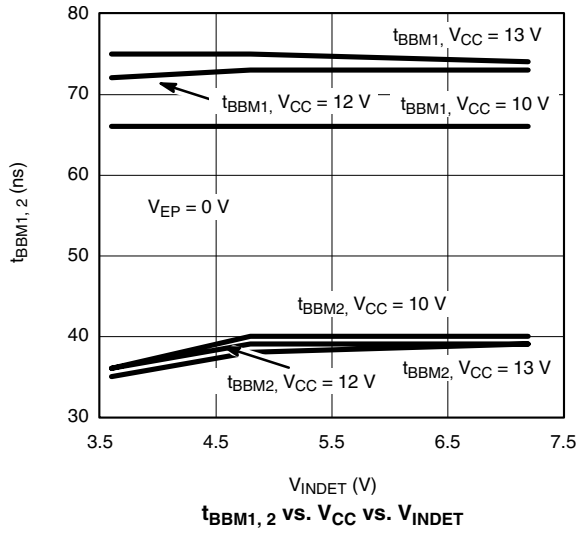
**TYPICAL CHARACTERISTICS**



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**TYPICAL WAVEFORMS**

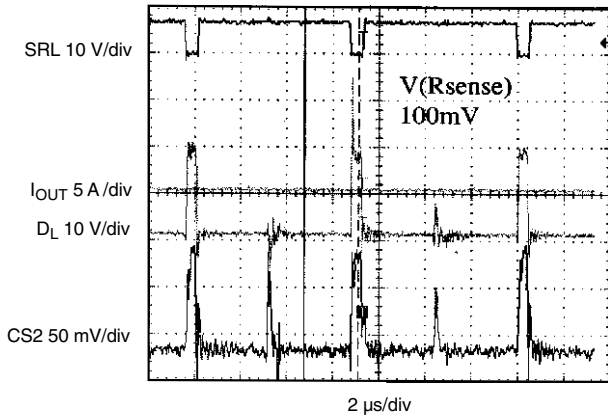


Figure 7. Foldback Mode,  $R_L = 0.02 \Omega$

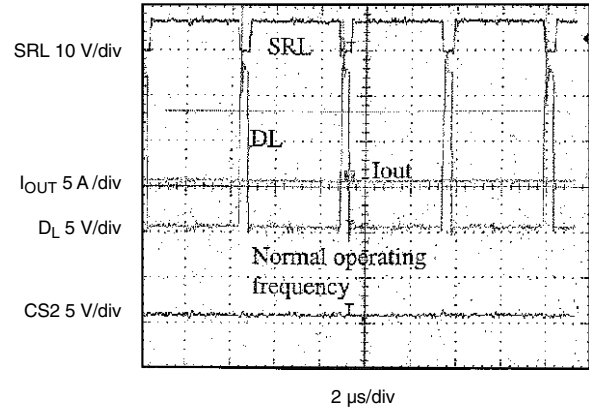


Figure 8. Normal Mode,  $R_L = 0.1 \Omega$

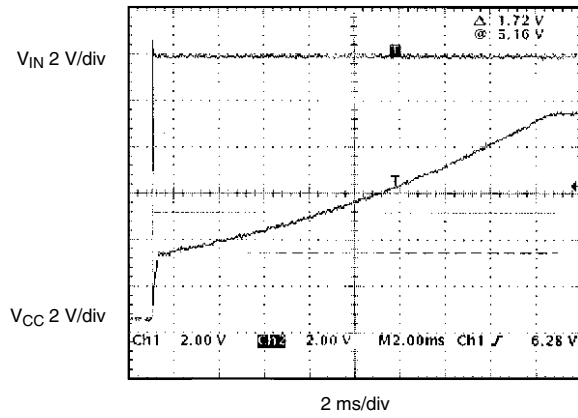


Figure 9.  $V_{CC}$  Ramp-Up

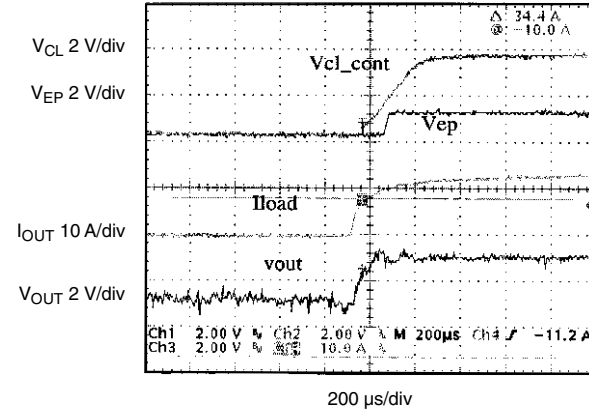


Figure 10. Overload Recovery

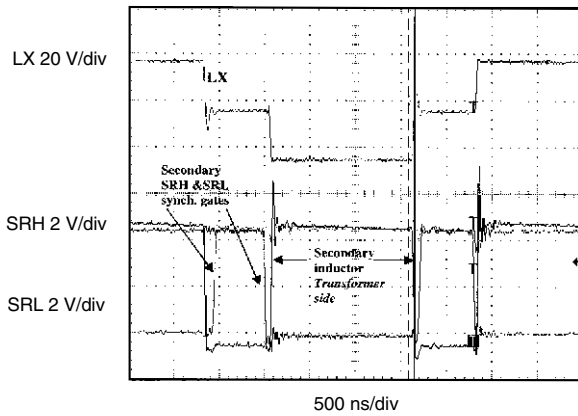


Figure 11. Effective BBM - Measured On Secondary

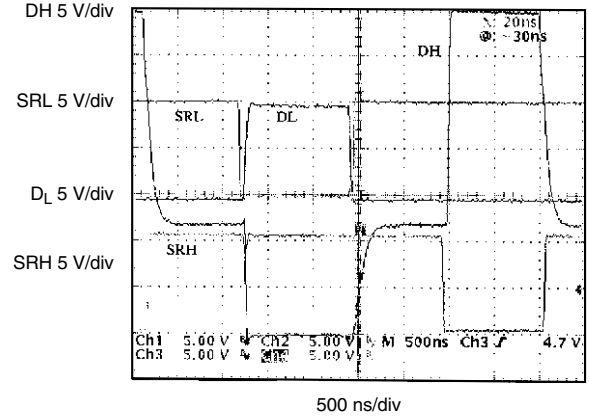


Figure 12. Drive Waveforms

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