

SSD1322

Product Preview

**480 x 128, Dot Matrix High Power OLED/PLED
Segment/Common Driver with Controller**

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SSD1322

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CONTENTS

1	GENERAL DESCRIPTION	6
2	FEATURES	6
3	ORDERING INFORMATION	6
4	BLOCK DIAGRAM	7
5	DIE PAD FLOOR PLAN	8
6	PIN ARRANGEMENT	12
6.1	SSD1322UR1 PIN ASSIGNMENT	12
7	PIN DESCRIPTIONS	14
8	FUNCTIONAL BLOCK DESCRIPTIONS	17
8.1	MCU INTERFACE	17
8.1.1	MCU Parallel 6800-series Interface	17
8.1.2	MCU Parallel 8080-series Interface	18
8.1.3	MCU Serial Interface (4-wire SPI).....	19
8.1.4	MCU Serial Interface (3-wire SPI).....	20
8.2	RESET CIRCUIT	21
8.3	GDDRAM	21
8.3.1	GDDRAM structure in Gray Scale mode.....	21
8.3.2	Data bus to RAM mapping	21
8.4	COMMAND DECODER	22
8.5	OSCILLATOR & TIMING GENERATOR	22
8.6	SEG/COM DRIVING BLOCK	23
8.7	SEG / COM DRIVER	24
8.8	GRAY SCALE DECODER.....	28
8.9	POWER ON AND OFF SEQUENCE.....	29
8.10	V _{DD} REGULATOR	30
9	COMMAND TABLE	31
10	COMMAND	35
10.1.1	Enable Gray Scale Table (00h).....	35
10.1.2	Set Column Address (15h).....	35
10.1.3	Write RAM Command (5Ch).....	35
10.1.4	Read RAM Command (5Dh).....	35
10.1.5	Set Row Address (75h).....	36
10.1.6	Set Re-map & Dual COM Line Mode (A0h).....	37
10.1.7	Set Display Start Line (A1h).....	40
10.1.8	Set Display Offset (A2h).....	41
10.1.9	Set Display Mode (A4h ~ A7h).....	42
10.1.10	Enable Partial Display (A8h).....	43
10.1.11	Exit Partial Display (A9h).....	43
10.1.12	Set Function selection (ABh).....	43
10.1.13	Set Display ON/OFF (AEh / AFh)	43
10.1.14	Set Phase Length (B1h).....	43
10.1.15	Set Front Clock Divider / Oscillator Frequency (B3h).....	43
10.1.16	Set GPIO (B5h).....	43
10.1.17	Set Second Pre-charge period (B6h).....	44
10.1.18	Set Gray Scale Table (B8h).....	44
10.1.19	Select Default Linear Gray Scale Table (B9h).....	44
10.1.20	Set Pre-charge voltage (BBh).....	44
10.1.21	Set V _{COMH} Voltage (BEh).....	44
10.1.22	Set Contrast Current (C1h).....	44
10.1.23	Master Current Control (C7h).....	45

10.1.24	Set Multiplex Ratio (CAh)	45
10.1.25	Set Command Lock (FDh)	45
11	MAXIMUM RATINGS	46
12	DC CHARACTERISTICS	47
13	AC CHARACTERISTICS	48
14	APPLICATION EXAMPLES	53
15	PACKAGE INFORMATION	55
15.1	SSD1322UR1 DETAIL DIMENSION	55

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TABLES

TABLE 3-1 : ORDERING INFORMATION	6
TABLE 5-1: SSD1322Z BUMP DIE PAD COORDINATES	9
TABLE 6-1: SSD1322UR1 PIN ASSIGNMENT TABLE	13
TABLE 7-1: SSD1352 PIN DESCRIPTION	14
TABLE 7-2 : BUS INTERFACE SELECTION	14
TABLE 8-1 : MCU INTERFACE ASSIGNMENT UNDER DIFFERENT BUS INTERFACE MODE	17
TABLE 8-2 : CONTROL PINS OF 6800 INTERFACE.....	17
TABLE 8-3 : CONTROL PINS OF 8080 INTERFACE (FORM 1)	19
TABLE 8-4 : CONTROL PINS OF 4-WIRE SERIAL INTERFACE.....	19
TABLE 8-5: CONTROL PINS OF 3-WIRE SERIAL INTERFACE.....	20
TABLE 8-6 : GDDRAM IN GRAY SCALE MODE (RESET)	21
TABLE 8-7 : DATA BUS USAGE	21
TABLE 9-1 : COMMAND TABLE	31
TABLE 11-1 : MAXIMUM RATINGS	46
TABLE 12-1 : DC CHARACTERISTICS	47
TABLE 13-1 : AC CHARACTERISTICS	48
TABLE 13-2 : 6800-SERIES MCU PARALLEL INTERFACE TIMING CHARACTERISTICS.....	49
TABLE 13-3 : 8080-SERIES MCU PARALLEL INTERFACE TIMING CHARACTERISTICS.....	50
TABLE 13-4 : SERIAL INTERFACE TIMING CHARACTERISTICS (4-WIRE SPI)	51
TABLE 13-5: SERIAL INTERFACE TIMING CHARACTERISTICS (3-WIRE SPI).....	52

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FIGURES

FIGURE 4-1 : SSD1322 BLOCK DIAGRAM.....	7
FIGURE 5-1: SSD1322Z DIE DRAWING	8
FIGURE 5-2: SSD1322Z ALIGNMENT MARK DIMENSION	8
FIGURE 6-1: SSD1322UR1 PIN ASSIGNMENT	12
FIGURE 8-1 : DATA READ BACK PROCEDURE - INSERTION OF DUMMY READ	18
FIGURE 8-2 : EXAMPLE OF WRITE PROCEDURE IN 8080 PARALLEL INTERFACE MODE.....	18
FIGURE 8-3 : EXAMPLE OF READ PROCEDURE IN 8080 PARALLEL INTERFACE MODE	18
FIGURE 8-4 : DISPLAY DATA READ BACK PROCEDURE - INSERTION OF DUMMY READ	19
FIGURE 8-5 : WRITE PROCEDURE IN 4-WIRE SERIAL INTERFACE MODE.....	20
FIGURE 8-6: WRITE PROCEDURE IN 3-WIRE SERIAL INTERFACE MODE.....	20
FIGURE 8-7 : OSCILLATOR CIRCUIT	22
FIGURE 8-8 : I_{REF} CURRENT SETTING BY RESISTOR VALUE	23
FIGURE 8-9 : SEGMENT AND COMMON DRIVER BLOCK DIAGRAM – SINGLE COM MODE	24
FIGURE 8-10 : SEGMENT AND COMMON DRIVER BLOCK DIAGRAM – DUAL COM MODE.....	25
FIGURE 8-11 : SEGMENT AND COMMON DRIVER SIGNAL WAVEFORM	26
FIGURE 8-12 : GRAY SCALE CONTROL BY PWM IN SEGMENT	27
FIGURE 8-13 : RELATION BETWEEN GDDRAM CONTENT AND GRAY SCALE TABLE ENTRY (UNDER COMMAND B9H ENABLE LINEAR GRAY SCALE TABLE).....	28
FIGURE 8-14 : THE POWER ON SEQUENCE.....	29
FIGURE 8-15 : THE POWER OFF SEQUENCE.....	29
FIGURE 8-16 $V_{CI} > 2.6V$, V_{DD} REGULATOR ENABLE PIN CONNECTION SCHEME	30
FIGURE 8-17 V_{DD} REGULATOR DISABLE PIN CONNECTION SCHEME	30
FIGURE 10-110-2 : EXAMPLE OF COLUMN AND ROW ADDRESS POINTER MOVEMENT (GRAY SCALE MODE).....	36
FIGURE 10-3 : ADDRESS POINTER MOVEMENT OF HORIZONTAL ADDRESS INCREMENT MODE	37
FIGURE 10-4: ADDRESS POINTER MOVEMENT OF VERTICAL ADDRESS INCREMENT MODE.....	37
FIGURE 10-5: GDDRAM IN GRAY SCALE MODE WITH OR WITHOUT COLUMN ADDRESS (A[1]) & NIBBLE REMAPPING (A[2])	38
FIGURE 10-6 : COM PINS HARDWARE CONFIGURATION – 1 (MUX RATIO: 128).....	39
FIGURE 10-7 : COM PINS HARDWARE CONFIGURATION – 2 (MUX RATIO: 64).....	39
FIGURE 10-8 : EXAMPLE OF SET DISPLAY START LINE WITH NO REMAP	40
FIGURE 10-9 : EXAMPLE OF SET DISPLAY OFFSET WITH NO REMAP	41
FIGURE 10-10 : EXAMPLE OF NORMAL DISPLAY	42
FIGURE 10-11 : EXAMPLE OF ENTIRE DISPLAY ON	42
FIGURE 10-12 : EXAMPLE OF ENTIRE DISPLAY OFF	42
FIGURE 10-13 : EXAMPLE OF INVERSE DISPLAY	42
FIGURE 10-14 : EXAMPLE OF PARTIAL MODE DISPLAY	43
FIGURE 10-15 : EXAMPLE OF GAMMA CORRECTION BY GAMMA LOOK UP TABLE SETTING.....	44
FIGURE 13-1 : 6800-SERIES MCU PARALLEL INTERFACE CHARACTERISTICS.....	49
FIGURE 13-2 : 8080-SERIES MCU PARALLEL INTERFACE CHARACTERISTICS.....	50
FIGURE 13-3 : SERIAL INTERFACE CHARACTERISTICS (4-WIRE SPI).....	51
FIGURE 13-4: SERIAL INTERFACE CHARACTERISTICS (3-WIRE SPI)	52
FIGURE 14-1 : SSD1322 APPLICATION EXAMPLE FOR 8-BIT 6800-PARALLEL INTERFACE MODE (INTERNAL REGULATED V_{DD})	53
FIGURE 14-2 : SSD1322 APPLICATION EXAMPLE FOR 8-BIT 6800-PARALLEL INTERFACE, DUAL COM MODE (INTERNAL V_{DD})	54
FIGURE 15-1: SSD1322UR1 DETAIL DIMENSION.....	55

1 GENERAL DESCRIPTION

SSD1322 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. It consists of 480 segments and 128 commons. This IC is designed for Common Cathode type OLED/PLED panel.

SSD1322 displays data directly from its internal 480 x 128 x 4 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from general MCU through the hardware selectable 6800-/8080-series compatible Parallel Interface or Serial Peripheral Interface. This driver IC has a 256 steps contrast control and can be widely used in many applications such as automotive and industrial control panel.

2 FEATURES

- Resolution: 480 x 128 dot matrix panel
- Power supply
 - $V_{DD} = 2.4V - 2.6V$ (Core V_{DD} power supply, can be regulated from V_{CI})
 - $V_{DDIO} = 1.65V - V_{CI}$ (MCU interface logic level)
 - $V_{CI} = 2.4V - 3.5V$ (Low voltage power supply)
 - $V_{CC} = 10.0V - 20.0V$ (Panel driving power supply)
- When V_{CI} is lower than 2.6V, V_{DD} should be supplied by external power source
- For matrix display
 - OLED driving output voltage, 20V maximum
 - Segment maximum source current: 300uA
 - Common maximum sink current: 80mA
 - 256 step contrast brightness current control, 16 step master current control
- 16 gray scale levels supported by embedded 480 x 128 x 4 bit SRAM display buffer
- Selectable MCU Interfaces:
 - 8-bit 6800/8080-series parallel interface
 - 3/4-wire Serial Peripheral Interface
- Selectable Common current sinking mode:
 - Dual COM mode
 - Single COM mode
- 8-bit programmable Gray Scale Look Up Table
- High Power Protection
- Programmable Frame Rate and Multiplexing Ratio
- Row re-mapping and Column re-mapping
- Sleep mode current <10uA with ram data kept
- Operating temperature range -40°C to 85°C.

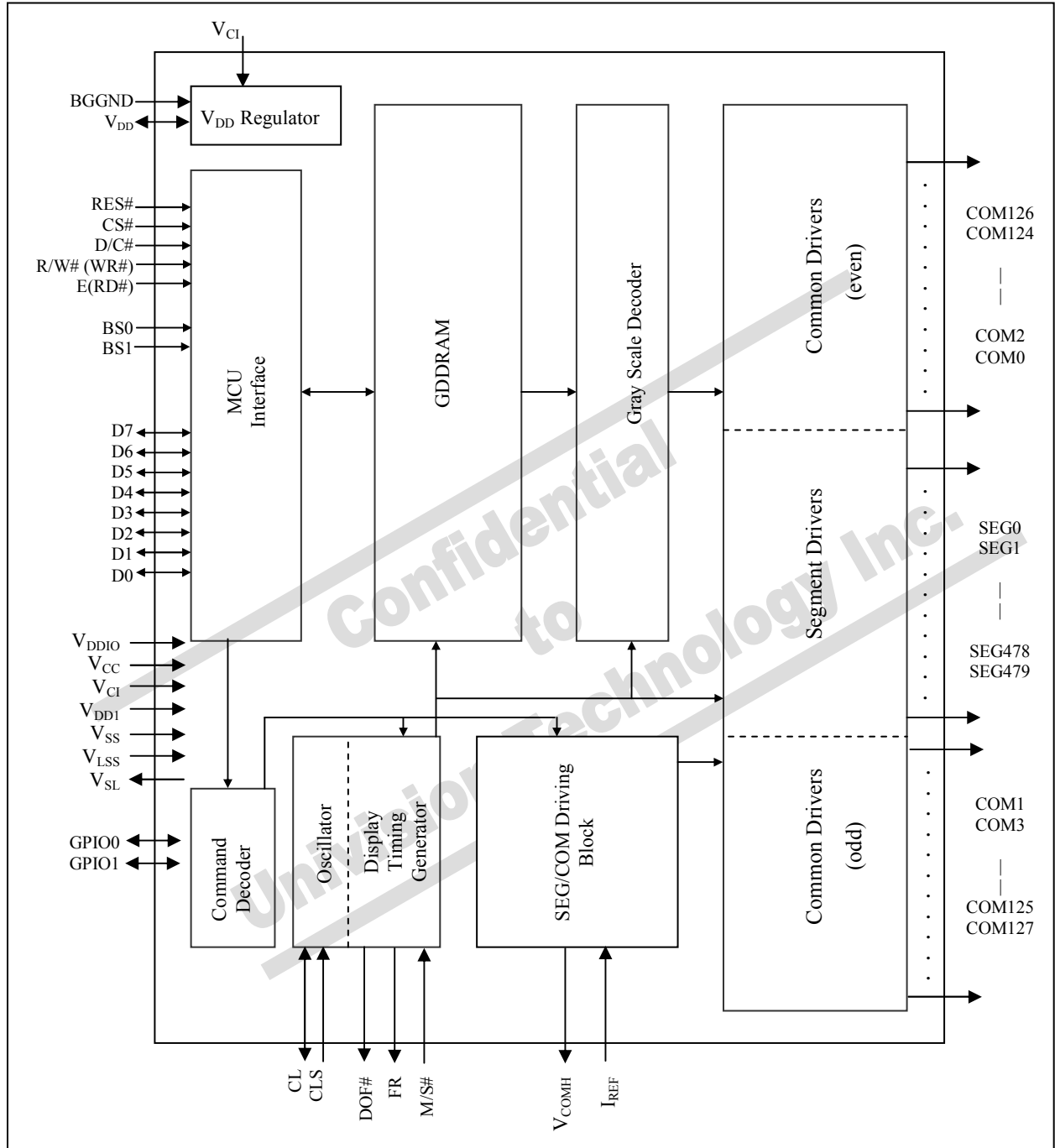
3 ORDERING INFORMATION

Table 3-1 : Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD1322Z	480	128	Gold bump Die	Page 8	<ul style="list-style-type: none"> • Min SEG pitch: 25um • Min COM pitch: 35um • Die thickness: 300 +/- 25um
SSD1322UR1	256	64 (dual COM)	COF	Page 12, 55	<ul style="list-style-type: none"> • 70mm film, 4 SPH • 8-bit 80/68/SPI interfaces • SEG, COM lead pitch 0.12mm x 0.999 = 0.11988mm • Also support 128 MUX (single COM) • Die thickness: 457 +/- 25um

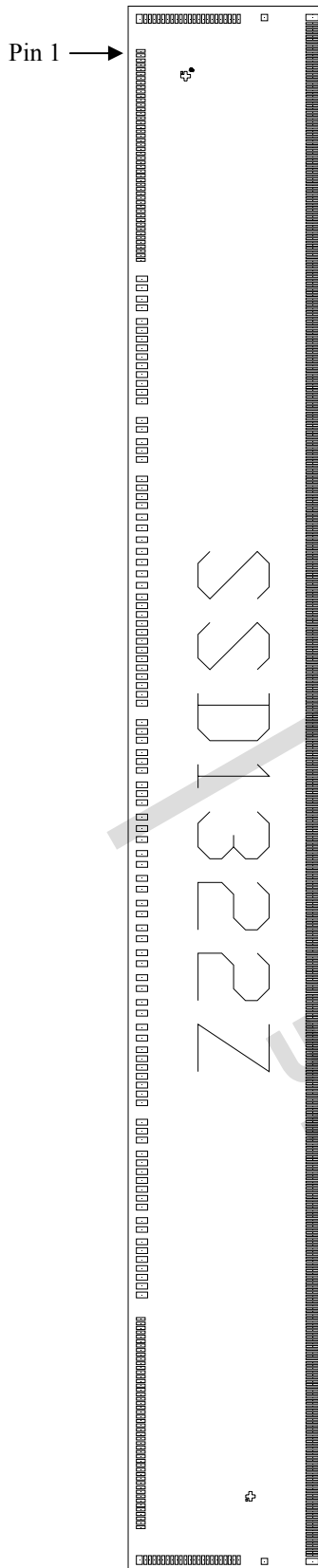
4 BLOCK DIAGRAM

Figure 4-1 : SSD1322 Block Diagram



5 DIE PAD FLOOR PLAN

Figure 5-1: SSD1322Z Die Drawing



Die size	12.4 mm x 1.53 mm
Die thickness	300 +/- 25um
Min I/O pad pitch	70um
Min SEG pad pitch	25um
Min COM pad pitch	35um
Bump height	Nominal 15um

Bump size		
Pad#	X[um]	Y[um]
1-48, 146-193	26	60
195-216, 706-727	60	26
49-145	45	90
194, 728	60	50
217, 705	50	50
218, 704	50	94
219-703	16	94

Alignment mark	Position	Size
+ shape	(5583.95,200.78)	75um x 75um
+ shape	(-5634.61,-309.88)	75um x 75um
SSL Logo	(-5682.11,-258.98)	-

(For details dimension please see Figure 5-2)

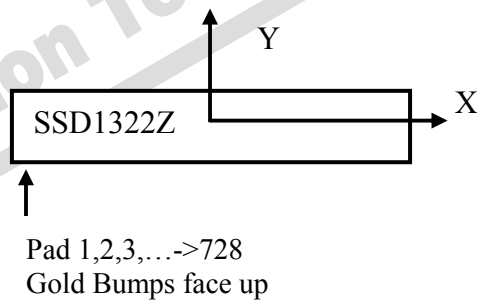
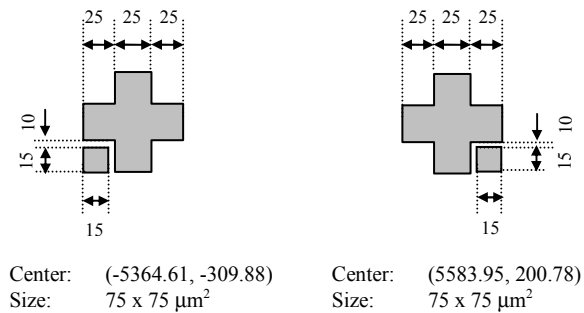


Figure 5-2: SSD1322Z alignment mark dimension



Pad no.	Pin name	X-pos	Y-pos
641	SEG417	-4500	687.81
642	SEG418	-4525	687.81
643	SEG419	-4550	687.81
644	SEG420	-4575	687.81
645	SEG421	-4600	687.81
646	SEG422	-4625	687.81
647	SEG423	-4650	687.81
648	SEG424	-4675	687.81
649	SEG425	-4700	687.81
650	SEG426	-4725	687.81
651	SEG427	-4750	687.81
652	SEG428	-4775	687.81
653	SEG429	-4800	687.81
654	SEG430	-4825	687.81
655	SEG431	-4850	687.81
656	SEG432	-4875	687.81
657	SEG433	-4900	687.81
658	SEG434	-4925	687.81
659	SEG435	-4950	687.81
660	SEG436	-4975	687.81
661	SEG437	-5000	687.81
662	SEG438	-5025	687.81
663	SEG439	-5050	687.81
664	SEG440	-5075	687.81
665	SEG441	-5100	687.81
666	SEG442	-5125	687.81
667	SEG443	-5150	687.81
668	SEG444	-5175	687.81
669	SEG445	-5200	687.81
670	SEG446	-5225	687.81
671	SEG447	-5250	687.81
672	SEG448	-5275	687.81
673	SEG449	-5300	687.81
674	SEG450	-5325	687.81
675	SEG451	-5350	687.81
676	SEG452	-5375	687.81
677	SEG453	-5400	687.81
678	SEG454	-5425	687.81
679	SEG455	-5450	687.81
680	SEG456	-5475	687.81
681	SEG457	-5500	687.81
682	SEG458	-5525	687.81
683	SEG459	-5550	687.81
684	SEG460	-5575	687.81
685	SEG461	-5600	687.81
686	SEG462	-5625	687.81
687	SEG463	-5650	687.81
688	SEG464	-5675	687.81
689	SEG465	-5700	687.81
690	SEG466	-5725	687.81
691	SEG467	-5750	687.81
692	SEG468	-5775	687.81
693	SEG469	-5800	687.81
694	SEG470	-5825	687.81
695	SEG471	-5850	687.81
696	SEG472	-5875	687.81
697	SEG473	-5900	687.81
698	SEG474	-5925	687.81
699	SEG475	-5950	687.81
700	SEG476	-5975	687.81
701	SEG477	-6000	687.81
702	SEG478	-6025	687.81
703	SEG479	-6050	687.81
704	VCC	-6097.34	687.81
705	VSL	-6097.34	311.09
706	LVSS	-6092.34	108.29
707	LVSS	-6092.34	73.29
708	COM64	-6092.34	37.85
709	COM65	-6092.34	2.85
710	COM66	-6092.34	-32.15
711	COM67	-6092.34	-67.15
712	COM68	-6092.34	-102.15
713	COM69	-6092.34	-137.15
714	COM70	-6092.34	-172.15
715	COM71	-6092.34	-207.15
716	COM72	-6092.34	-242.15
717	COM73	-6092.34	-277.15
718	COM74	-6092.34	-312.15
719	COM75	-6092.34	-347.15
720	COM76	-6092.34	-382.15

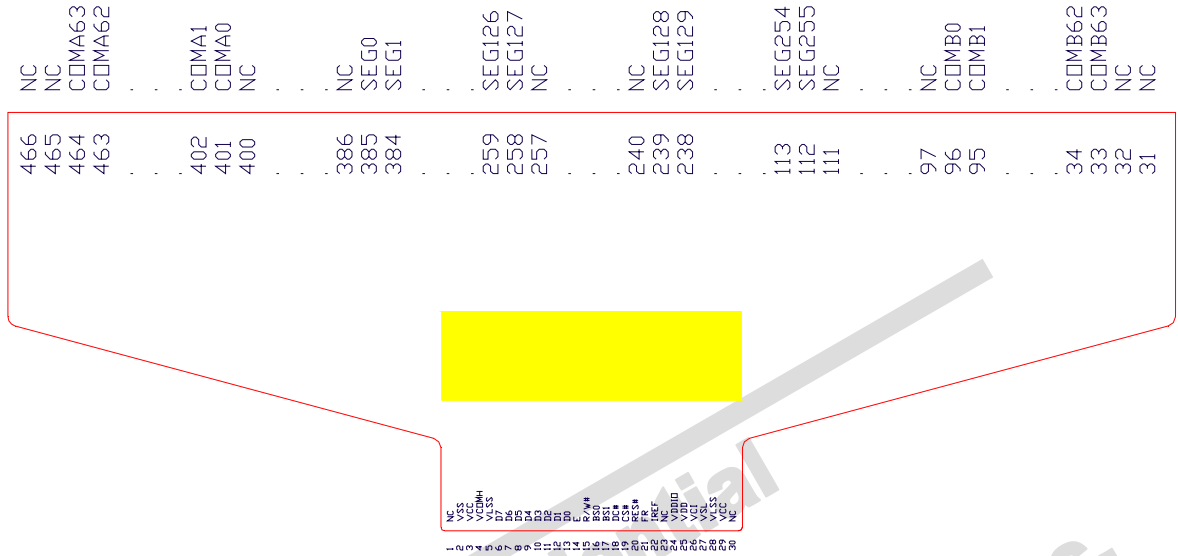
Pad no.	Pin name	X-pos	Y-pos
721	COM77	-6092.34	-417.15
722	COM78	-6092.34	-452.15
723	COM79	-6092.34	-487.15
724	COM80	-6092.34	-522.15
725	COM81	-6092.34	-557.15
726	COM82	-6092.34	-592.15
727	COM83	-6092.34	-627.15
728	LVSS	-6092.34	-674.15

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6 PIN ARRANGEMENT

6.1 SSD1322UR1 pin assignment

Figure 6-1: SSD1322UR1 Pin Assignment



Note:

(1) COM sequence is listed in terms of dual COM mode; refer to Table 9-1 for details.

Table 6-1: SSD132UR1 Pin Assignment Table

Pad no.	Pin name	Pad no.	Pin name	Pad no.	Pin name	Pad no.	Pin name	Pad no.	Pin name	Pad no.	Pin name
1	NC	81	COMB15	161	SEG206	241	NC	321	SEG64	401	COMA0
2	VSS	82	COMB14	162	SEG205	242	NC	322	SEG63	402	COMA1
3	VCC	83	COMB13	163	SEG204	243	NC	323	SEG62	403	COMA2
4	VCOMH	84	COMB12	164	SEG203	244	NC	324	SEG61	404	COMA3
5	VLSS	85	COMB11	165	SEG202	245	NC	325	SEG60	405	COMA4
6	D7	86	COMB10	166	SEG201	246	NC	326	SEG59	406	COMA5
7	D6	87	COMB9	167	SEG200	247	NC	327	SEG58	407	COMA6
8	D5	88	COMB8	168	SEG199	248	NC	328	SEG57	408	COMA7
9	D4	89	COMB7	169	SEG198	249	NC	329	SEG56	409	COMA8
10	D3	90	COMB6	170	SEG197	250	NC	330	SEG55	410	COMA9
11	D2	91	COMB5	171	SEG196	251	NC	331	SEG54	411	COMA10
12	D1	92	COMB4	172	SEG195	252	NC	332	SEG53	412	COMA11
13	D0	93	COMB3	173	SEG194	253	NC	333	SEG52	413	COMA12
14	E/RD#	94	COMB2	174	SEG193	254	NC	334	SEG51	414	COMA13
15	RW#	95	COMB1	175	SEG192	255	NC	335	SEG50	415	COMA14
16	BS0	96	COMB0	176	SEG191	256	NC	336	SEG49	416	COMA15
17	BS1	97	NC	177	SEG190	257	NC	337	SEG48	417	COMA16
18	DC#	98	NC	178	SEG189	258	SEG127	338	SEG47	418	COMA17
19	CS#	99	NC	179	SEG188	259	SEG126	339	SEG46	419	COMA18
20	RES#	100	NC	180	SEG187	260	SEG125	340	SEG45	420	COMA19
21	FR	101	NC	181	SEG186	261	SEG124	341	SEG44	421	COMA20
22	IREF	102	NC	182	SEG185	262	SEG123	342	SEG43	422	COMA21
23	NC	103	NC	183	SEG184	263	SEG122	343	SEG42	423	COMA22
24	VDDIO	104	NC	184	SEG183	264	SEG121	344	SEG41	424	COMA23
25	VDD	105	NC	185	SEG182	265	SEG120	345	SEG40	425	COMA24
26	VCI	106	NC	186	SEG181	266	SEG119	346	SEG39	426	COMA25
27	VSL	107	NC	187	SEG180	267	SEG118	347	SEG38	427	COMA26
28	VLSS	108	NC	188	SEG179	268	SEG117	348	SEG37	428	COMA27
29	VCC	109	NC	189	SEG178	269	SEG116	349	SEG36	429	COMA28
30	NC	110	NC	190	SEG177	270	SEG115	350	SEG35	430	COMA29
31	NC	111	NC	191	SEG176	271	SEG114	351	SEG34	431	COMA30
32	NC	112	SEG255	192	SEG175	272	SEG113	352	SEG33	432	COMA31
33	COMB63	113	SEG254	193	SEG174	273	SEG112	353	SEG32	433	COMA32
34	COMB62	114	SEG253	194	SEG173	274	SEG111	354	SEG31	434	COMA33
35	COMB61	115	SEG252	195	SEG172	275	SEG110	355	SEG30	435	COMA34
36	COMB60	116	SEG251	196	SEG171	276	SEG109	356	SEG29	436	COMA35
37	COMB59	117	SEG250	197	SEG170	277	SEG108	357	SEG28	437	COMA36
38	COMB58	118	SEG249	198	SEG169	278	SEG107	358	SEG27	438	COMA37
39	COMB57	119	SEG248	199	SEG168	279	SEG106	359	SEG26	439	COMA38
40	COMB56	120	SEG247	200	SEG167	280	SEG105	360	SEG25	440	COMA39
41	COMB55	121	SEG246	201	SEG166	281	SEG104	361	SEG24	441	COMA40
42	COMB54	122	SEG245	202	SEG165	282	SEG103	362	SEG23	442	COMA41
43	COMB53	123	SEG244	203	SEG164	283	SEG102	363	SEG22	443	COMA42
44	COMB52	124	SEG243	204	SEG163	284	SEG101	364	SEG21	444	COMA43
45	COMB51	125	SEG242	205	SEG162	285	SEG100	365	SEG20	445	COMA44
46	COMB50	126	SEG241	206	SEG161	286	SEG99	366	SEG19	446	COMA45
47	COMB49	127	SEG240	207	SEG160	287	SEG98	367	SEG18	447	COMA46
48	COMB48	128	SEG239	208	SEG159	288	SEG97	368	SEG17	448	COMA47
49	COMB47	129	SEG238	209	SEG158	289	SEG96	369	SEG16	449	COMA48
50	COMB46	130	SEG237	210	SEG157	290	SEG95	370	SEG15	450	COMA49
51	COMB45	131	SEG236	211	SEG156	291	SEG94	371	SEG14	451	COMA50
52	COMB44	132	SEG235	212	SEG155	292	SEG93	372	SEG13	452	COMA51
53	COMB43	133	SEG234	213	SEG154	293	SEG92	373	SEG12	453	COMA52
54	COMB42	134	SEG233	214	SEG153	294	SEG91	374	SEG11	454	COMA53
55	COMB41	135	SEG232	215	SEG152	295	SEG90	375	SEG10	455	COMA54
56	COMB40	136	SEG231	216	SEG151	296	SEG89	376	SEG9	456	COMA55
57	COMB39	137	SEG230	217	SEG150	297	SEG88	377	SEG8	457	COMA56
58	COMB38	138	SEG229	218	SEG149	298	SEG87	378	SEG7	458	COMA57
59	COMB37	139	SEG228	219	SEG148	299	SEG86	379	SEG6	459	COMA58
60	COMB36	140	SEG227	220	SEG147	300	SEG85	380	SEG5	460	COMA59
61	COMB35	141	SEG226	221	SEG146	301	SEG84	381	SEG4	461	COMA60
62	COMB34	142	SEG225	222	SEG145	302	SEG83	382	SEG3	462	COMA61
63	COMB33	143	SEG224	223	SEG144	303	SEG82	383	SEG2	463	COMA62
64	COMB32	144	SEG223	224	SEG143	304	SEG81	384	SEG1	464	COMA63
65	COMB31	145	SEG222	225	SEG142	305	SEG80	385	SEG0	465	NC
66	COMB30	146	SEG221	226	SEG141	306	SEG79	386	NC	466	NC
67	COMB29	147	SEG220	227	SEG140	307	SEG78	387	NC		
68	COMB28	148	SEG219	228	SEG139	308	SEG77	388	NC		
69	COMB27	149	SEG218	229	SEG138	309	SEG76	389	NC		
70	COMB26	150	SEG217	230	SEG137	310	SEG75	390	NC		
71	COMB25	151	SEG216	231	SEG136	311	SEG74	391	NC		
72	COMB24	152	SEG215	232	SEG135	312	SEG73	392	NC		
73	COMB23	153	SEG214	233	SEG134	313	SEG72	393	NC		
74	COMB22	154	SEG213	234	SEG133	314	SEG71	394	NC		
75	COMB21	155	SEG212	235	SEG132	315	SEG70	395	NC		
76	COMB20	156	SEG211	236	SEG131	316	SEG69	396	NC		
77	COMB19	157	SEG210	237	SEG130	317	SEG68	397	NC		
78	COMB18	158	SEG209	238	SEG129	318	SEG67	398	NC		
79	COMB17	159	SEG208	239	SEG128	319	SEG66	399	NC		
80	COMB16	160	SEG207	240	NC	320	SEG65	400	NC		

7 PIN DESCRIPTIONS

Key:

I = Input	NC = Not Connected
O = Output	Pull LOW= connect to Ground
IO = Bi-directional (input/output)	Pull HIGH= connect to V_{DDIO}
P = Power pin	

Table 7-1: SSD1352 Pin Description

Pin Name	Pin Type	Description										
V_{DD}	P	Power supply pin for core logic operation. A capacitor is required to connect between this pin and V_{SS} . Refer to Section 8.10 for details.										
V_{DDIO}	P	Power supply for interface logic level. It should be matched with the MCU interface voltage level. Refer to Section 8.10 for details.										
V_{CI}	P	Low voltage power supply. V_{CI} must always be equal to or higher than V_{DD} and V_{DDIO} . Refer to Section 8.10 for details.										
V_{CC}	P	Power supply for panel driving voltage. This is also the most positive power voltage supply pin.										
V_{DD1}	P	Power supply and it should be connected to V_{DD} .										
V_{SS}	P	Ground pin.										
V_{LSS}	P	Analog system ground pin.										
V_{COMH}	P	COM signal deselected voltage level. A capacitor should be connected between this pin and V_{SS} .										
BGGND	P	It should be connected to ground.										
GPIO0	IO	This is a reserved pin. It should be kept NC.										
GPIO1	IO	This is a reserved pin. It should be kept NC.										
V_{SL}	P	This is segment voltage reference pin. When external V_{SL} is used, connect with resistor and diode to ground (details depend on application).										
BS[1:0]	I	MCU bus interface selection pins. Select appropriate logic setting as described in the following table. <div style="text-align: center;"> <p>Table 7-2 : Bus Interface selection</p> <table border="1"> <thead> <tr> <th>BS[1:0]</th> <th>Bus Interface Selection</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>4 line SPI</td> </tr> <tr> <td>01</td> <td>3 line SPI</td> </tr> <tr> <td>10</td> <td>8-bit 8080 parallel</td> </tr> <tr> <td>11</td> <td>8-bit 6800 parallel</td> </tr> </tbody> </table> </div> <p>Note (1) 0 is connected to V_{SS} (2) 1 is connected to V_{DDIO}</p>	BS[1:0]	Bus Interface Selection	00	4 line SPI	01	3 line SPI	10	8-bit 8080 parallel	11	8-bit 6800 parallel
BS[1:0]	Bus Interface Selection											
00	4 line SPI											
01	3 line SPI											
10	8-bit 8080 parallel											
11	8-bit 6800 parallel											

Pin Name	Pin Type	Description
I _{REF}	I	This pin is the segment output current reference pin. A resistor should be connected between this pin and V _{SS} to maintain the current around 10uA. Please refer to section 8.6 for the formula of resistor value from I _{REF} .
M/S#	I	This pin must be connected to V _{DDIO} to enable the chip.
CL	IO	External clock input pin. When internal clock is enable (i.e. pull HIGH in CLS pin), this pin is not used and should be connected to Ground. When internal clock is disable (i.e. pull LOW is CLS pin), this pin is the external clock source input pin.
CLS	I	Internal clock selection pin. When this pin is pulled HIGH, internal oscillator is enabled (normal operation). When this pin is pulled LOW, an external clock signal should be connected to CL.
CS#	I	This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.
RES#	I	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin pull HIGH during normal operation.
D/C#	I	This pin is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the content at D[7:0] will be interpreted as data. When the pin is pulled LOW, the content at D[7:0] will be interpreted as command.
R/W# (WR#)	I	This pin is read / write control input pin connecting to the MCU interface. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin R/W (WR#) must be connected to V _{SS} .
E (RD#)	I	This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin E(RD#) must be connected to V _{SS} .
D[7:0]	IO	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. (Except for D2 pin in SPI mode) Refer to Section 8.1 for different bus interface connection.
DN[9:0]	IO	These are reserved pins and should be connected to V _{SS} .

Pin Name	Pin Type	Description
FR	O	This pin is No Connection pins. Nothing should be connected to this pin. This pin should be left open individually.
DOF#	O	This pin is No Connection pins. Nothing should be connected to this pin. This pin should be left open individually.
SEG[479:0]	O	These pins provide the OLED segment driving signals. These pins are V_{SS} state when display is OFF.
COM[127:0]	O	These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is OFF.



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8 FUNCTIONAL BLOCK DESCRIPTIONS

8.1 MCU Interface

SSD1322 MCU interface consist of 8 data pin and 5 control pins. The pin assignment at different interface mode is summarized in Table 8-1. Different MCU mode can be set by hardware selection on BS[1:0] pins (refer to Table 7-2 for BS[1:0] pins setting)

Table 8-1 : MCU interface assignment under different bus interface mode

Pin Name Bus Interface	Data/Command Interface							Control Signal					
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	CS#	D/C#	RES#
8-bit 8080	D[7:0]							RD#	WR#	CS#	D/C#	RES#	
8-bit 6800	D[7:0]							E	R/W#	CS#	D/C#	RES#	
3-wire SPI	Tie LOW				NC	SDIN	SCLK	Tie LOW	CS#	Tie LOW	RES#		
4-wire SPI	Tie LOW				NC	SDIN	SCLK	Tie LOW	CS#	D/C#	RES#		

8.1.1 MCU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation. A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write. The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

Table 8-2 : Control pins of 6800 interface

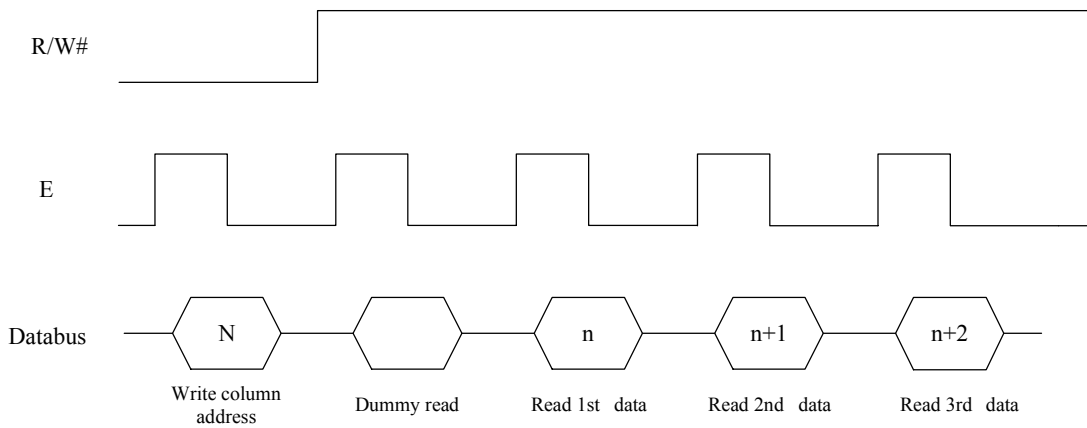
Function	E	R/W#	CS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note

- (1) ↓ stands for falling edge of signal
- (2) H stands for HIGH in signal
- (3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-1.

Figure 8-1 : Data read back procedure - insertion of dummy read



8.1.2 MCU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.

A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.

A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 8-2 : Example of Write procedure in 8080 parallel interface mode

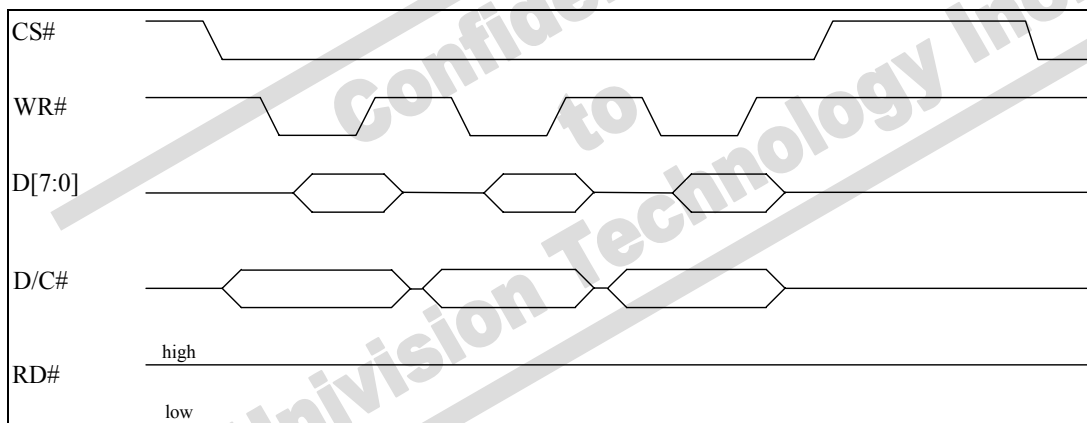


Figure 8-3 : Example of Read procedure in 8080 parallel interface mode

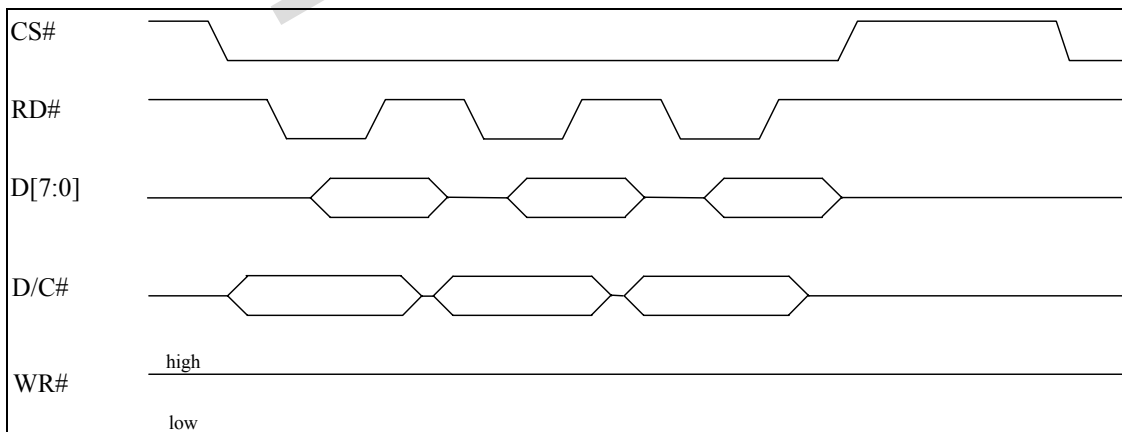


Table 8-3 : Control pins of 8080 interface (Form 1)

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

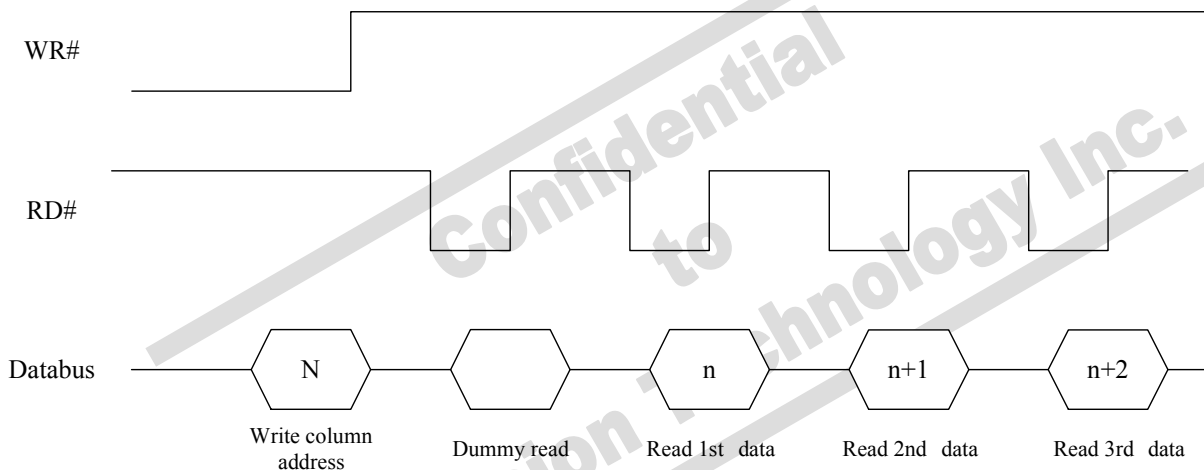
Note

- (1) ↑ stands for rising edge of signal
- (2) H stands for HIGH in signal
- (3) L stands for LOW in signal
- (4) Refer to

Figure 13-2 for Form 1 8080-Series MPU Parallel Interface Timing Characteristics

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-4.

Figure 8-4 : Display data read back procedure - insertion of dummy read



8.1.3 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, E and R/W# can be connected to an external ground.

Table 8-4 : Control pins of 4-wire Serial interface

Function	E(RD#)	R/W#(WR#)	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	L	↑
Write data	Tie LOW	Tie LOW	L	H	↑

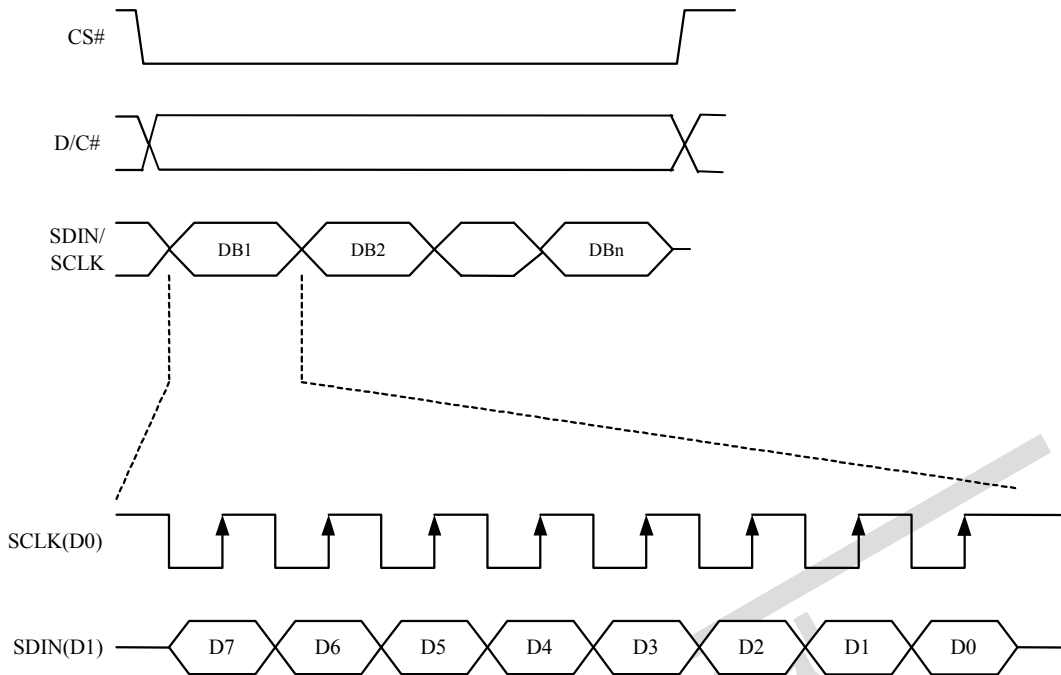
Note

- (1) H stands for HIGH in signal
- (2) L stands for LOW in signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

Figure 8-5 : Write procedure in 4-wire Serial interface mode



8.1.4 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#. In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, R/W# (WR#), E(RD#) and D/C# can be connected to an external ground.

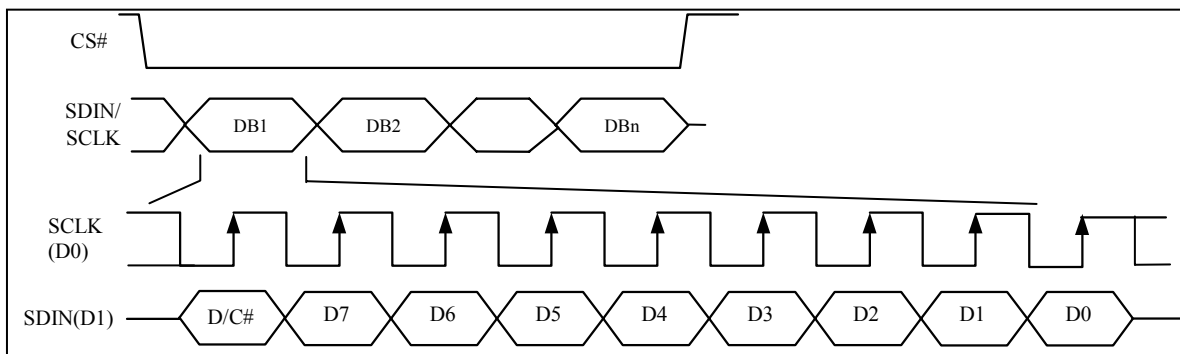
The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

Table 8-5: Control pins of 3-wire Serial interface

Function	E(RD#)	R/W#(WR#)	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	Tie LOW	↑
Write data	Tie LOW	Tie LOW	L	Tie LOW	↑

Note
(¹) L stands for LOW in signal

Figure 8-6: Write procedure in 3-wire Serial interface mode



8.2 Reset Circuit

When RES# input is pulled LOW, the chip is initialized with the following status:

1. Display is OFF
2. 128 MUX Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Display start line is set at display RAM address 0
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Contrast control register is set at 7Fh

8.3 GDDRAM

8.3.1 GDDRAM structure in Gray Scale mode

The GDDRAM address map in Table 8-6 shows the GDDRAM in Gray Scale mode. Since in Gray Scale mode, there are 16 gray levels. Therefore four bits (one nibble) are allocated for each pixel. For example D30480[3:0] in Table 8-6 corresponds to the pixel located in (COM127, SEG2). So the lower nibble and higher nibble of D0, D1, D2, ..., D30717, D30718, D30719 in Table 8-6 represent the 480x128 data nibbles in the GDDRAM.

Table 8-6 : GDDRAM in Gray Scale mode (RESET)

	SEG0	SEG1	SEG2	SEG3		SEG476	SEG477	SEG478	SEG479	SEG Outputs RAM Column address (HEX)
	00		00			77		77		
COM0	00	D1[3:0]	D1[7:4]	D0[3:0]	D0[7:4]	D239[3:0]	D239[7:4]	D238[3:0]	D238[7:4]	
COM1	01	D241[3:0]	D241[7:4]	D240[3:0]	D240[7:4]	D479[3:0]	D479[7:4]	D478[3:0]	D478[7:4]	
COM126	7E	D30241[3:0]	D30241[7:4]	D30240[3:0]	D30240[7:4]	D30479[3:0]	D30479[7:4]	D30478[3:0]	D30478[7:4]	
COM127	7F	D30481[3:0]	D30481[7:4]	D30480[3:0]	D30480[7:4]	D30719[3:0]	D30719[7:4]	D30718[3:0]	D30718[7:4]	
RAM COM Outputs Address (HEX)										Corresponding to one pixel

8.3.2 Data bus to RAM mapping

Table 8-7 : Data bus usage

Read / Write Data		Data bus D[7:0]							
Bus width	Input order	D7	D6	D5	D4	D3	D2	D1	D0
8 bits	1 st	3	3	3	3	2	2	2	2
	2 nd	1	1	1	1	0	0	0	0

Corresponding to one pixel

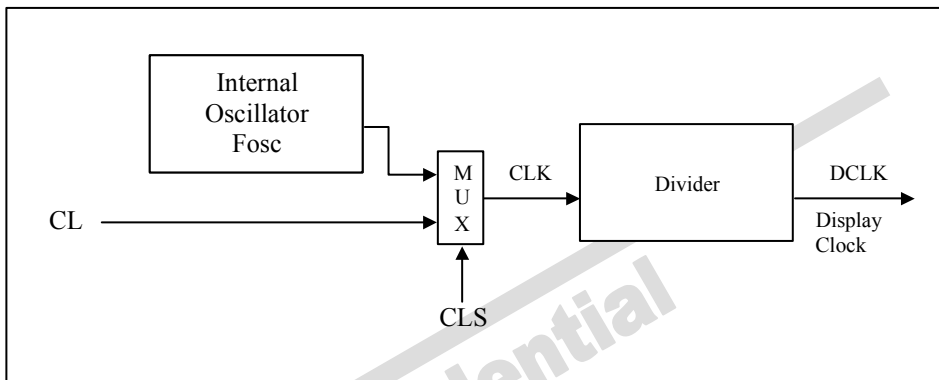
8.4 Command Decoder

This module determines whether the input should be interpreted as data or command based upon the input of the D/C# pin.

If D/C# pin is HIGH, data is written to Graphic Display Data RAM (GDDRAM). If it is LOW, the inputs at D0-D7 are interpreted as a Command and it will be decoded and be written to the corresponding command register.

8.5 Oscillator & Timing Generator

Figure 8-7 : Oscillator Circuit



This module is an On-Chip low power RC oscillator circuitry (Figure 8-7). The operation clock (CLK) can be generated either from internal oscillator or external source CL pin by CLS pin. If CLS pin is HIGH, internal oscillator is selected. If CLS pin is LOW, external clock from CL pin will be used for CLK. The frequency of internal oscillator F_{OSC} can be programmed by command B3h.

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor “D” can be programmed from 1 to 1024 by command B3h.

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula:

$$F_{FRM} = \frac{F_{osc}}{D \times K \times \text{No. of Mux}}$$

where

- D stands for clock divide ratio. It is set by command B3h A[3:0]. The divide ratio has the range from 1 to 1024.
- K is the number of display clocks per row. The value is derived by
 $K = \text{Phase 1 period} + \text{Phase 2 period} + X$
 $X = \text{DCLKs in current drive period. Default } X = \text{constant} + \text{GS15} = 10 + 112 = 122$
 Default K is $9 + 7 + 122 = 138$
- Number of multiplex ratio is set by command A8h. The reset value is 127 (i.e. 128MUX).
- F_{osc} is the oscillator frequency. It can be changed by command B3h A[7:4]. The higher the register setting results in higher frequency.

If the frame frequency is set too low, flickering may occur. On the other hand, higher frame frequency leads to higher power consumption on the whole system.

8.6 SEG/COM Driving Block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

- V_{CC} is the most positive voltage supply.
- V_{COMH} is the Common deselected level. It is internally regulated.
- V_{LSS} is the ground path of the analog and panel current.
- I_{REF} is a reference current source for segment current drivers I_{SEG} . The relationship between reference current and segment current of a color is:

$$I_{SEG} = \text{Contrast} / 256 * I_{REF} * \text{scale factor} * 2$$

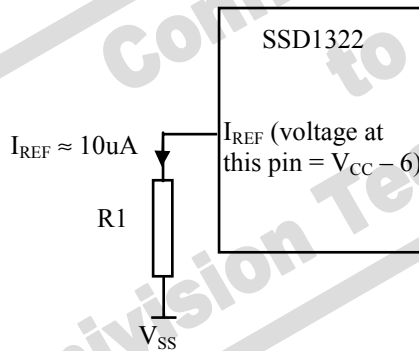
in which

the contrast (0~255) is set by Set Contrast command (C1h); and
the scale factor (1 ~ 16) is set by Master Current Control command (C7h).

For example, in order to achieve $I_{SEG} = 300\mu\text{A}$ at maximum contrast 255, I_{REF} is set to around $10\mu\text{A}$. This current value is obtained by connecting an appropriate resistor from I_{REF} pin to V_{SS} as shown in Figure 8-8.

Recommended $I_{REF} = 10\mu\text{A}$

Figure 8-8 : I_{REF} Current Setting by Resistor Value



Since the voltage at I_{REF} pin is $V_{CC} - 6\text{V}$, the value of resistor $R1$ can be found as below:

For $I_{REF} = 10\mu\text{A}$, $V_{CC} = 18\text{V}$:

$$\begin{aligned} R1 &= (\text{Voltage at } I_{REF} - V_{SS}) / I_{REF} \\ &= (18 - 6) / 10\mu\text{A} \\ &\approx 1.2\text{M}\Omega \end{aligned}$$

8.7 SEG / COM Driver

Segment drivers consist of 480 current sources to drive OLED panel. The driving current can be adjusted from 0 to 300uA with 8 bits, 256 steps by contrast setting command (C1h). Common drivers generate scanning voltage pulse. The block diagrams and waveforms of the segment and common driver are shown as follow.

Figure 8-9 : Segment and Common Driver Block Diagram – Single COM mode

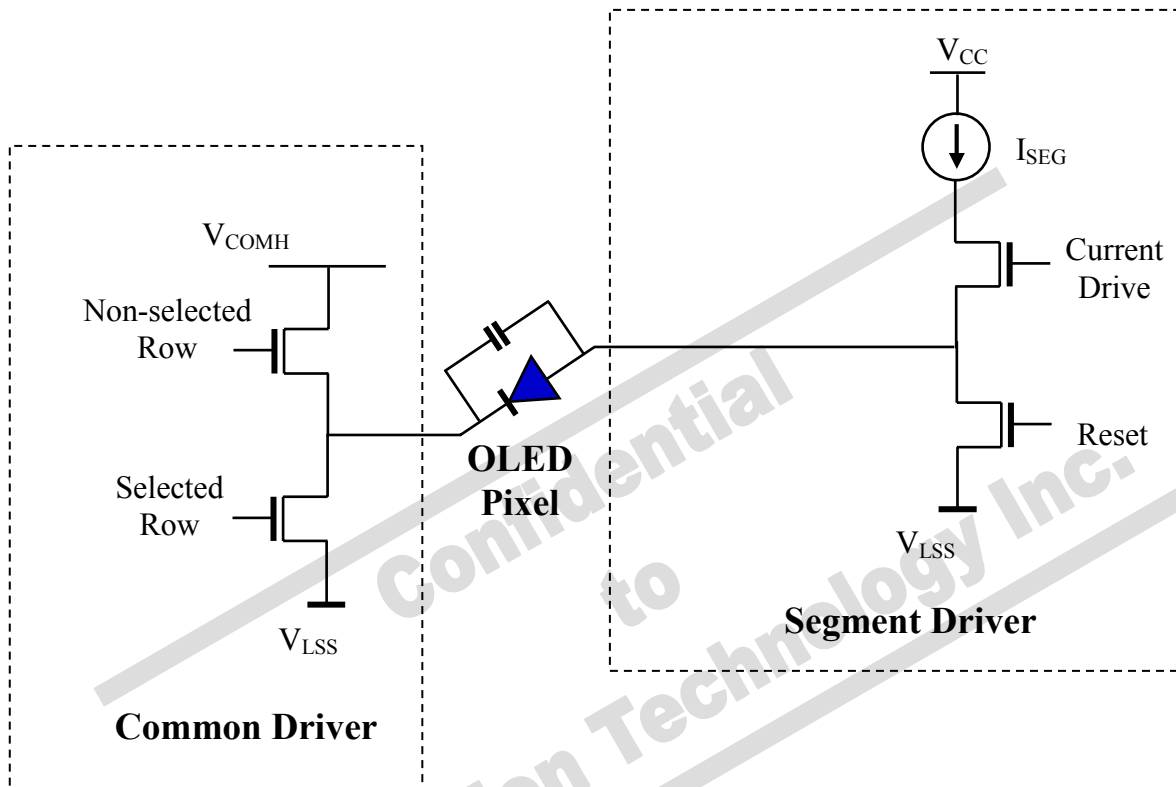
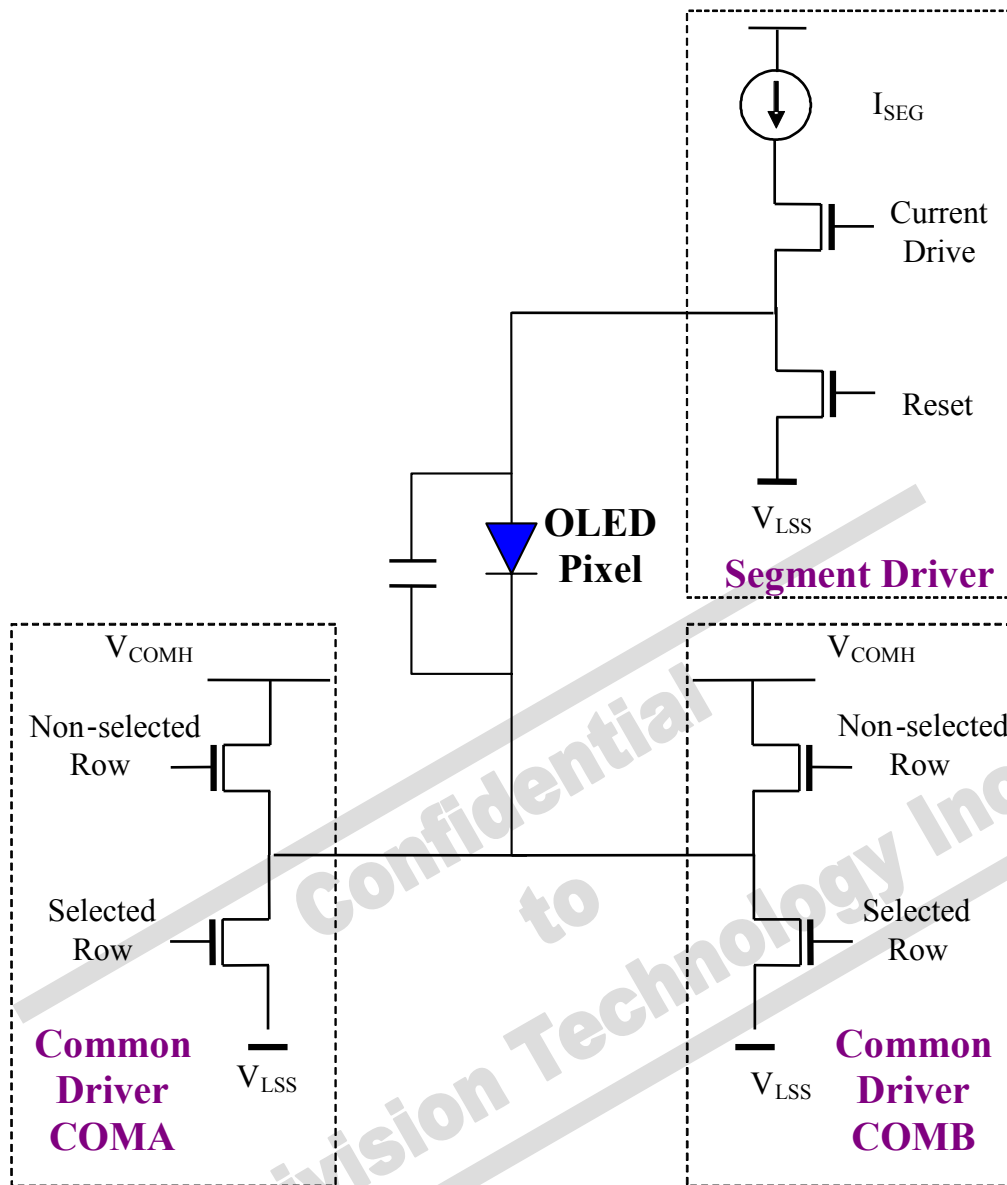


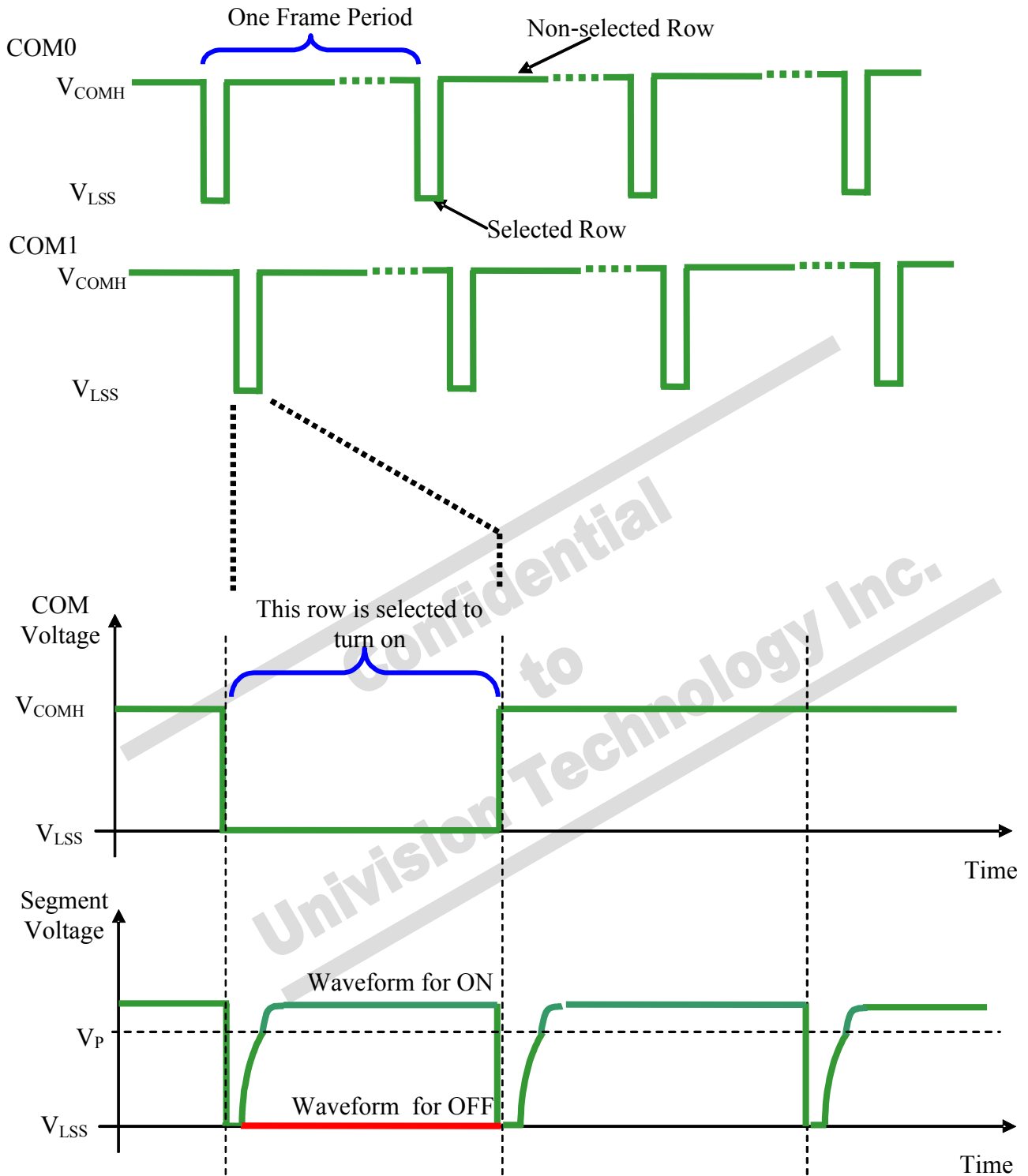
Figure 8-10 : Segment and Common Driver Block Diagram – Dual COM mode



The commons are scanned sequentially, row by row. If a row is not selected, all the pixels on the row are in reverse bias by driving those commons to voltage V_{COMH} as shown in Figure 8-11.

In the scanned row, the pixels on the row will be turned ON or OFF by sending the corresponding data signal to the segment pins. If the pixel is turned OFF, the segment current is kept at 0. On the other hand, the segment drives to I_{SEG} when the pixel is turned ON.

Figure 8-11 : Segment and Common Driver Signal Waveform



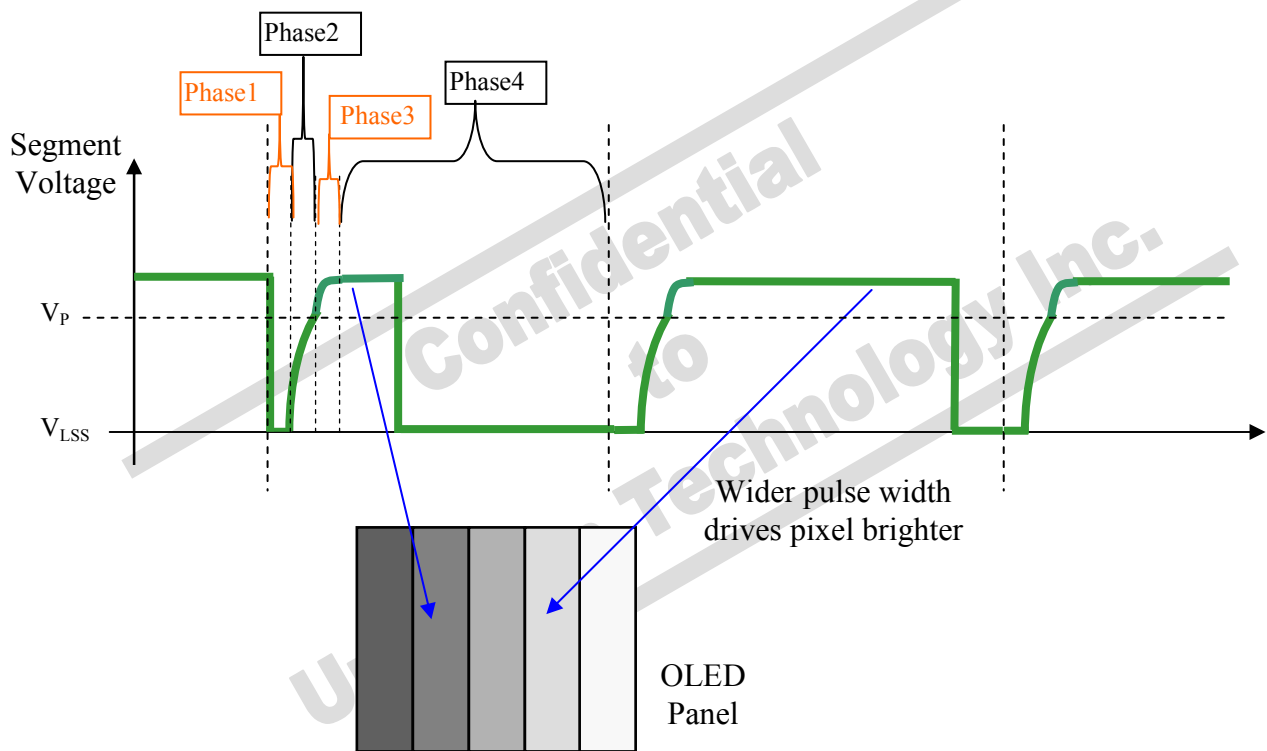
There are four phases to driving an OLED a pixel. In phase 1, the pixel is reset by the segment driver to V_{LSS} in order to discharge the previous data charge stored in the parasitic capacitance along the segment electrode. The period of phase 1 can be programmed by command B1h A[3:0]. An OLED panel with larger capacitance requires a longer period for discharging.

In phase 2, first pre-charge is performed. The pixel is driven to attain the corresponding voltage level V_P from V_{LSS} . The amplitude of V_P can be programmed by the command BBh. The period of phase 2 can be programmed by command B1h A[7:4]. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.

In phase 3, the OLED pixel is driven to the targeted driving voltage through second pre-charge. The second pre-charge can control the speed of the charging process. The period of phase 3 can be programmed by command B6h.

Last phase (phase 4) is current drive stage. The current source in the segment driver delivers constant current to the pixel. The driver IC employs PWM (Pulse Width Modulation) method to control the gray scale of each pixel individually. The gray scale can be programmed into different Gamma settings by command B8h/B9h. The bigger gamma setting (the wider pulse widths) in the current drive stage results in brighter pixels and vice versa (details refer to Section 8.8). This is shown in the following figure.

Figure 8-12 : Gray Scale Control by PWM in Segment



After finishing phase 4, the driver IC will go back to phase 1 to display the next row image data. This four-step cycle is run continuously to refresh image display on OLED panel.

The length of phase 4 is defined by command B8h or B9h. In the table, the gray scale is defined in incremental way, with reference to the length of previous table entry.

8.8 Gray Scale Decoder

The gray scale effect is generated by controlling the pulse width (PW) of current drive phase, except GS0 there is no pre-charge (phase 2, 3) and current drive (phase 4). The driving period is controlled by the gray scale settings (setting 0 ~ setting 180). The larger the setting, the brighter the pixel will be. The Gray Scale Table stores the corresponding gray scale setting of the 16 gray scale levels (GS0~GS15) through the software commands B8h or B9h.

As shown in Figure 8-13, GDDRAM data has 4 bits, represent the 16 gray scale levels from GS0 to GS15. Note that the frame frequency is affected by GS15 setting.

Figure 8-13 : Relation between GDDRAM content and Gray Scale table entry (under command B9h Enable Linear Gray Scale Table)

GDDRAM data (4 bits)	Gray Scale Table	Default Gamma Setting (Command B9h)
0000	GS0	Setting 0
0001	GS1 ⁽¹⁾	Setting 0
0010	GS2	Setting 8
0011	GS3	Setting 16
⋮	⋮	⋮
⋮	⋮	⋮
1101	GS13	Setting 96
1110	GS14	Setting 104
1111	GS15	Setting 112

Note:

⁽¹⁾ Both GS0 and GS1 have no 2nd pre-charge (phase 3) and current drive (phase 4), however GS1 has 1st pre-charge (phase 2).

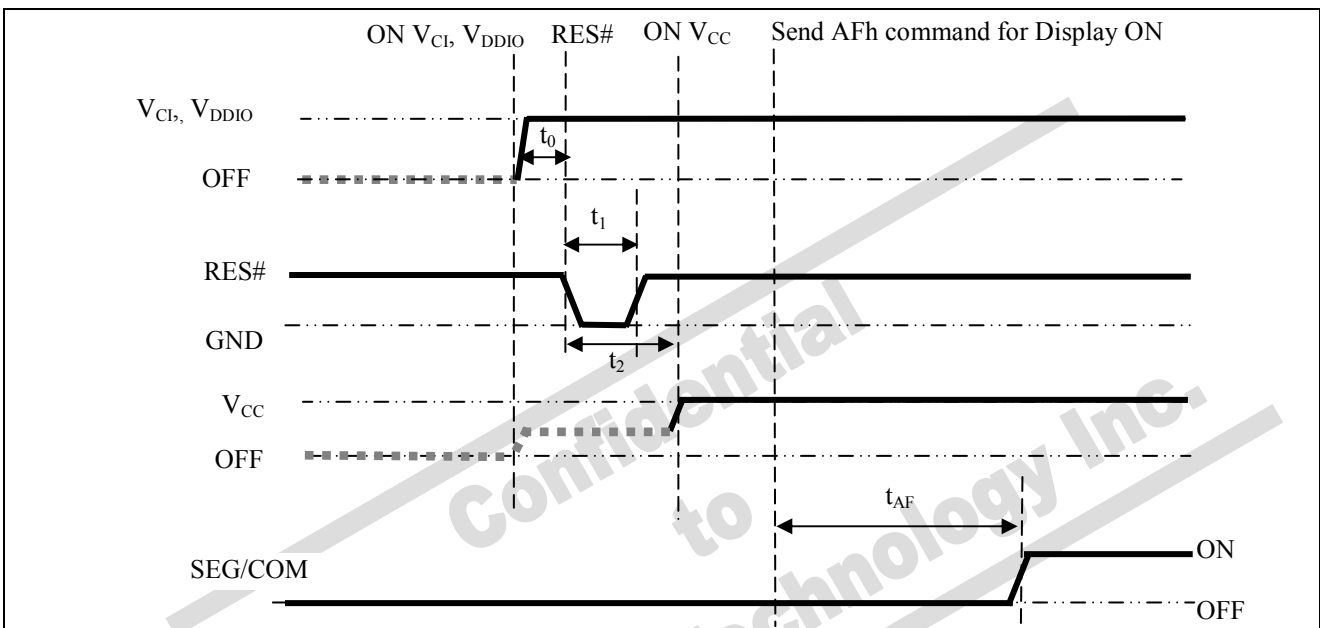
8.9 Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1322 (assume V_{CL} and V_{DDIO} are at the same voltage level and internal V_{DD} is used).

Power ON sequence:

1. Power ON V_{CL} , V_{DDIO} .
2. After V_{CL} , V_{DDIO} become stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 100us (t_1)⁽⁴⁾ and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON V_{CC} .⁽¹⁾
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms (t_{AF}).

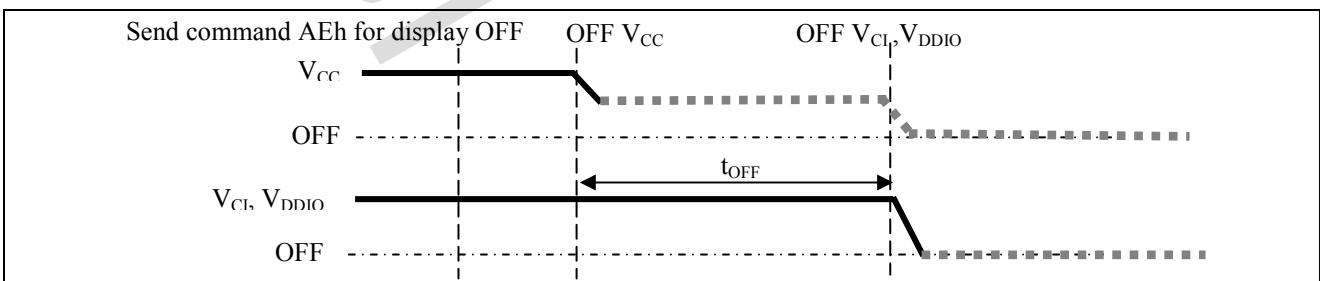
Figure 8-14 : The Power ON sequence.



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC} .^{(1), (2)}
3. Wait for t_{OFF} . Power OFF V_{CL}, V_{DDIO} . (where Minimum $t_{OFF}=0ms$ ⁽³⁾, Typical $t_{OFF}=100ms$)

Figure 8-15 : The Power OFF sequence



Note:

- (1) Since an ESD protection circuit is connected between V_{CL} , V_{DDIO} and V_{CC} , V_{CC} becomes lower than V_{CL} whenever V_{CL} , V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 8-14 and Figure 8-15.
- (2) V_{CC} should be kept float (disable) when it is OFF.
- (3) V_{CL} , V_{DDIO} should not be Power OFF before V_{CC} Power OFF.
- (4) The register values are reset after t_1 .
- (5) Power pins (V_{DD} , V_{CC}) can never be pulled to ground under any circumstance.

8.10 V_{DD} Regulator

In SSD1322, the power supply pin for core logic operation, V_{DD}, can be supplied by external source or internally regulated through the V_{DD} regulator.

The internal V_{DD} regulator is enabled by setting bit A[0] to 1b in command ABh “Function Selection”. V_{CI} should be larger than 2.6V when using the internal V_{DD} regulator. The typical regulated V_{DD} is about 2.5V

It should be notice that, no matter V_{DD} is supplied by external source or internally regulated; V_{CI} must always be set equivalent to or higher than V_{DD} and V_{DDIO}.

The following figure shows the V_{DD} regulator pin connection scheme:

Figure 8-16 V_{CI} > 2.6V, V_{DD} regulator enable pin connection scheme

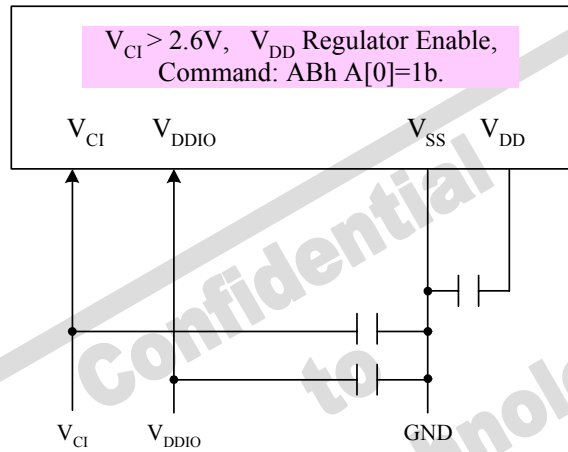
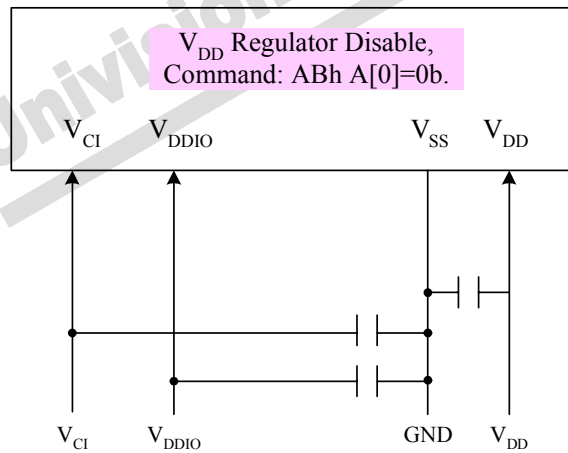


Figure 8-17 V_{DD} regulator disable pin connection scheme



9 COMMAND TABLE

Table 9-1 : Command table

(D/C#=0, R/W#(WR#) = 0, E(RD#)=1) unless specific setting is stated)

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	00	0	0	0	0	0	0	0	0	Enable Gray Scale table	This command is sent to enable the Gray Scale table setting (command B8h)
0 1 1	15 A[6:0] B[6:0]	0 * *	0 A ₆ B ₆	0 A ₅ B ₅	1 A ₄ B ₄	0 A ₃ B ₃	1 A ₂ B ₂	0 A ₁ B ₁	1 A ₀ B ₀	Set Column Address	Set Column start and end address A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=119] Range from 0 to 119
0	5C	0	1	0	1	1	1	0	0	Write RAM Command	Enable MCU to write Data into RAM
0	5D	0	1	0	1	1	1	0	1	Read RAM Command	Enable MCU to read Data from RAM
0 1 1	75 A[6:0] B[6:0]	0 * *	1 A ₆ B ₆	1 A ₅ B ₅	1 A ₄ B ₄	0 A ₃ B ₃	1 A ₂ B ₂	0 A ₁ B ₁	1 A ₀ B ₀	Set Row Address	Set Row start and end address A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=127] Range from 0 to 127
0 1 1	A0 A[7:0] B[4]	1 0 *	0 0 *	1 A ₅ 0	0 A ₄ B ₄	0 0 0	0 A ₂ 0	0 A ₁ 0	0 A ₀ 1	Set Re-map and Dual COM Line mode	<p>A[0]=0b, Horizontal address increment [reset] A[0]=1b, Vertical address increment</p> <p>A[1]=0b, Disable Column Address Re-map [reset] A[1]=1b, Enable Column Address Re-map</p> <p>A[2]=0b, Disable Nibble Re-map [reset] A[2]=1b, Enable Nibble Re-map</p> <p>A[4]=0b, Scan from COM0 to COM[N-1] [reset] A[4]=1b, Scan from COM[N-1] to COM0, where N is the Multiplex ratio</p> <p>A[5]=0b, Disable COM Split Odd Even [reset] A[5]=1b, Enable COM Split Odd Even</p> <p>B[4], Enable / disable Dual COM Line mode 00b, Disable Dual COM mode [reset] 01b, Enable Dual COM mode (MUX ≤ 63)</p> <p>Note ⁽¹⁾ COM Split Odd Even mode must be disabled (A[5]=0b) when enabling the Dual COM mode (B[4]=1b)</p> <p>Details refer to Section 10.1.6</p>
0 1	A1 A[6:0]	1 *	0 A ₆	1 A ₅	0 A ₄	0 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Display Start Line	Set display RAM display start line register from 0-127 Display start line register is reset to 00h after RESET

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description																																		
0 1	A2 A[6:0]	1 *	0 A ₆	1 A ₅	0 A ₄	0 A ₃	0 A ₂	1 A ₁	0 A ₀	Set Display Offset	Set vertical scroll by COM from 0-127 The value is reset to 00H after RESET																																		
0	A4~A7	1	0	1	0	0	X ₂	X ₁	X ₀	Set Display Mode	A4h = Entire Display OFF, all pixels turns OFF in GS level 0 A5h = Entire Display ON, all pixels turns ON in GS level 15 A6h = Normal Display [reset] A7h = Inverse Display (GS0 → GS15, GS1 → GS14, GS2 → GS13, ...)																																		
0 1 1	A8 A[6:0] B[6:0]	1 0 0	0 A ₆ B ₆	1 A ₅ B ₅	0 A ₄ B ₄	1 A ₃ B ₃	0 A ₂ B ₂	0 A ₁ B ₁	0 A ₀ B ₀	Enable Partial Display	This command turns ON partial mode. The partial mode display area is defined by the following two parameters, A[6:0]: Address of start row in the display area B[6:0]: Address of end row in the display area, where B[6:0] must be ≥ A[6:0]																																		
0	A9	1	0	1	0	1	0	0	1	Exit Partial Display	This command is sent to exit the Partial Display mode																																		
0 1	AB A[0]	1 0	0 0	1 0	0 0	1 0	0 0	1 0	1 A ₀	Function Selection	A[0]=0b, Select external V _{DD} A[0]=1b, Enable internal V _{DD} regulator [reset]																																		
0	AE~AF	1	0	1	0	1	1	1	X ₀	Set Sleep mode ON/OFF	AEh = Sleep mode ON (Display OFF) AFh = Sleep mode OFF (Display ON)																																		
0 1	B1 A[7:0]	1 A ₇	0 A ₆	1 A ₅	1 A ₄	0 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Phase Length	A[3:0] Phase 1 period (reset phase length) of 5~31 DCLK(s) clocks as follow: <table border="1" data-bbox="1021 1272 1428 1534"> <thead> <tr> <th>A[3:0]</th> <th>Phase 1 period</th> </tr> </thead> <tbody> <tr><td>0000</td><td>invalid</td></tr> <tr><td>0001</td><td>invalid</td></tr> <tr><td>0010</td><td>5 DCLKs</td></tr> <tr><td>0011</td><td>7 DCLKs</td></tr> <tr><td>0100</td><td>9 DCLKs [reset]</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>1111</td><td>31 DCLKs</td></tr> </tbody> </table> A[7:4] Phase 2 period (first pre-charge phase length) of 3~15 DCLK(s) clocks as follow: <table border="1" data-bbox="1029 1684 1420 1975"> <thead> <tr> <th>A[7:4]</th> <th>Phase 2 period</th> </tr> </thead> <tbody> <tr><td>0000</td><td>invalid</td></tr> <tr><td>0001</td><td>invalid</td></tr> <tr><td>0010</td><td>invalid</td></tr> <tr><td>0011</td><td>3 DCLKs</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>0111</td><td>7 DCLKs [reset]</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>1111</td><td>15 DCLKs</td></tr> </tbody> </table>	A[3:0]	Phase 1 period	0000	invalid	0001	invalid	0010	5 DCLKs	0011	7 DCLKs	0100	9 DCLKs [reset]	:	:	1111	31 DCLKs	A[7:4]	Phase 2 period	0000	invalid	0001	invalid	0010	invalid	0011	3 DCLKs	:	:	0111	7 DCLKs [reset]	:	:	1111	15 DCLKs
A[3:0]	Phase 1 period																																												
0000	invalid																																												
0001	invalid																																												
0010	5 DCLKs																																												
0011	7 DCLKs																																												
0100	9 DCLKs [reset]																																												
:	:																																												
1111	31 DCLKs																																												
A[7:4]	Phase 2 period																																												
0000	invalid																																												
0001	invalid																																												
0010	invalid																																												
0011	3 DCLKs																																												
:	:																																												
0111	7 DCLKs [reset]																																												
:	:																																												
1111	15 DCLKs																																												

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description																										
0 1	B3 A[7:0]	1 A ₇	0 A ₆	1 A ₅	1 A ₄	0 A ₃	0 A ₂	1 A ₁	1 A ₀	Set Front Clock Divider / Oscillator Frequency	A[3:0] [reset=0], divide by DIVSET where <table border="1" style="margin-left: 20px;"><thead><tr><th>A[3:0]</th><th>DIVSET</th></tr></thead><tbody><tr><td>0000</td><td>divide by 1</td></tr><tr><td>0001</td><td>divide by 2</td></tr><tr><td>0010</td><td>divide by 4</td></tr><tr><td>0011</td><td>divide by 8</td></tr><tr><td>0100</td><td>divide by 16</td></tr><tr><td>0101</td><td>divide by 32</td></tr><tr><td>0110</td><td>divide by 64</td></tr><tr><td>0111</td><td>divide by 128</td></tr><tr><td>1000</td><td>divide by 256</td></tr><tr><td>1001</td><td>divide by 512</td></tr><tr><td>1010</td><td>divide by 1024</td></tr><tr><td>>=1011</td><td>invalid</td></tr></tbody></table> A[7:4] Oscillator frequency, frequency increases as level increases [reset=1100b]	A[3:0]	DIVSET	0000	divide by 1	0001	divide by 2	0010	divide by 4	0011	divide by 8	0100	divide by 16	0101	divide by 32	0110	divide by 64	0111	divide by 128	1000	divide by 256	1001	divide by 512	1010	divide by 1024	>=1011	invalid
A[3:0]	DIVSET																																				
0000	divide by 1																																				
0001	divide by 2																																				
0010	divide by 4																																				
0011	divide by 8																																				
0100	divide by 16																																				
0101	divide by 32																																				
0110	divide by 64																																				
0111	divide by 128																																				
1000	divide by 256																																				
1001	divide by 512																																				
1010	divide by 1024																																				
>=1011	invalid																																				
0 1	B5 A[3:0]	1 *	0 *	1 *	1 *	0 A ₃	1 A ₂	0 A ₁	1 A ₀	Set GPIO	A[1:0] GPIO0: 00 pin HiZ, Input disabled 01 pin HiZ, Input enabled 10 pin output LOW [reset] 11 pin output HIGH A[3:2] GPIO1: 00 pin HiZ, Input disabled 01 pin HiZ, Input enabled 10 pin output LOW [reset] 11 pin output HIGH																										
0 1	B6 A[3:0]	1 *	0 *	1 *	1 *	0 A ₃	1 A ₂	1 A ₁	0 A ₀		Set Second Precharge Period	A[3:0] Second Pre-charge period 0000b 0 dclk 0001b 1 dclk 1000b 8 dclks [reset] 1111b 15 dclks																									
0 1 1 1 1 1 1	B8 A1[7:0] A2[7:0] . . . A14[7:0] A15[7:0]	1 A1 ₇ A2 ₇ . . . A14 ₇ A15 ₇	0 A1 ₆ A2 ₆ . . . A14 ₆ A15 ₆	1 A1 ₅ A2 ₅ . . . A14 ₅ A15 ₅	1 A1 ₄ A2 ₄ . . . A14 ₄ A15 ₄	1 A1 ₃ A2 ₃ . . . A14 ₃ A15 ₃	0 A1 ₂ A2 ₂ . . . A14 ₂ A15 ₂	0 A1 ₁ A2 ₁ . . . A14 ₁ A15 ₁	0 A1 ₀ A2 ₀ . . . A14 ₀ A15 ₀	Set Gray Scale Table		The next 15 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d) A1[7:0]: Gamma Setting for GS1, A2[7:0]: Gamma Setting for GS2, A14[7:0]: Gamma Setting for GS14, A15[7:0]: Gamma Setting for GS15 Note (1) 0 ≤ Setting of GS1 < Setting of GS2 < Setting of GS3..... < Setting of GS14 < Setting of GS15 Refer to Section 8.8 for details (2) The setting must be followed by the Enable Gray Scale Table command (00h)																									

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description																		
0	B9	1	0	1	1	1	0	0	1	Select Default Linear Gray Scale table	The default Linear Gray Scale table is set in unit of DCLK's as follow GS0 level pulse width = 0; GS1 level pulse width = 0; GS2 level pulse width = 8; GS3 level pulse width = 16; : : GS14 level pulse width = 104; GS15 level pulse width = 112 Refer to Section 8.8 for details																		
0 1	BB A[4:0]	1 *	0 *	1 *	1 A ₄	1 A ₃	0 A ₂	1 A ₁	1 A ₀	Set Pre-charge voltage	Set pre-charge voltage level.[reset = 17h] <table border="1"> <thead> <tr> <th>A[5:1]</th> <th>Hex code</th> <th>pre-charge voltage</th> </tr> </thead> <tbody> <tr> <td>00000</td> <td>00h</td> <td>0.20 x V_{CC}</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>11111</td> <td>3Eh</td> <td>0.60 x V_{CC}</td> </tr> </tbody> </table>	A[5:1]	Hex code	pre-charge voltage	00000	00h	0.20 x V _{CC}	:	:	:	11111	3Eh	0.60 x V _{CC}						
A[5:1]	Hex code	pre-charge voltage																											
00000	00h	0.20 x V _{CC}																											
:	:	:																											
11111	3Eh	0.60 x V _{CC}																											
0 1	BE A[3:0]	1 *	0 *	1 *	1 A ₃	1 A ₂	1 A ₁	1 A ₀	0	Set V _{COMH}	Set COM deselect voltage level [reset = 04h] A[3:0] = <table border="1"> <thead> <tr> <th>A[2:0]</th> <th>Hex code</th> <th>V_{COMH}</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>00h</td> <td>0.72 x V_{CC}</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>0100</td> <td>04h</td> <td>0.80 x V_{CC}</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>0111</td> <td>07h</td> <td>0.86 x V_{CC}</td> </tr> </tbody> </table>	A[2:0]	Hex code	V _{COMH}	0000	00h	0.72 x V _{CC}	:	:	:	0100	04h	0.80 x V _{CC}	:	:	:	0111	07h	0.86 x V _{CC}
A[2:0]	Hex code	V _{COMH}																											
0000	00h	0.72 x V _{CC}																											
:	:	:																											
0100	04h	0.80 x V _{CC}																											
:	:	:																											
0111	07h	0.86 x V _{CC}																											
0 1	C1 A[7:0]	1 A ₇	1 A ₆	0 A ₅	0 A ₄	0 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Contrast Current	A[7:0]: Contrast current value, range:00h~FFh, i.e. 256 steps for I _{SEG} current [reset = 7Fh]																		
0 1	C7 A[3:0]	1 *	1 *	0 *	0 A ₃	0 A ₂	1 A ₁	1 A ₀	1 A ₀	Master Contrast Current Control	A[3:0] = 0000b, reduce output currents for all colors to 1/16 0001b, reduce output currents for all colors to 2/16 : 1110b, reduce output currents for all colors to 15/16 1111b, no change [reset]																		
0 1	CA A[6:0]	1 *	1 A ₆	0 A ₅	0 A ₄	1 A ₃	0 A ₂	1 A ₁	0 A ₀	Set MUX Ratio	A[6:0]: Set MUX ratio from 16MUX ~ 128MUX A[6:0] = 15d represents 16MUX : A[6:0] = 127d represents 128MUX [reset]																		
0 1	FD A[2]	1 0	1 0	1 0	1 1	1 0	1 A ₂	0 1	1 0	Set Command Lock	A[2]: MCU protection status [reset = 12h] A[2] = 0b, Unlock OLED driver IC MCU interface from entering command [reset] A[2] = 1b, Lock OLED driver IC MCU interface from entering command Note (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command																		

Note

(1) "*" stands for "Don't care".

10 COMMAND

10.1.1 Enable Gray Scale Table (00h)

This command is sent to enable the Gray Scale Table setting (command B8h).

10.1.2 Set Column Address (15h)

This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command A0h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

10.1.3 Write RAM Command (5Ch)

After entering this single byte command, data entries will be written into the display RAM until another command is written. Address pointer is increased accordingly. This command must be sent before write data into RAM.

10.1.4 Read RAM Command (5Dh)

After entering this single byte command, data is read from display RAM until another command is written. Address pointer is increased accordingly. This command must be sent before read data from RAM.

10.1.5 Set Row Address (75h)

This triple byte command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. If vertical address increment mode is enabled by command A0h, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address.

The diagram below shows the way of column and row address pointer movement through the example: column start address is set to 1 and column end address is set to 118, row start address is set to 2 and row end address is set to 126. Horizontal address increment mode is enabled by command A0h. In this case, the graphic display data RAM column accessible range is from column 1 to column 118 and from row 1 to row 126 only. In addition, the column and row address pointers are set to 1 and 2, respectively. After finishing read/write four pixels of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation (*solid line in Figure 10-1*). Whenever the column address pointer finishes accessing the end column 118, it is reset back to column 1 and row address is automatically increased by 1 (*solid line in Figure 10-1*). While the end row 126 and end column 118 RAM location is accessed, the row address is reset back to 2 and the column address is reset back to 1 (*dotted line in Figure 10-1*).

Figure 10-110-2 : Example of Column and Row Address Pointer Movement (Gray Scale Mode)

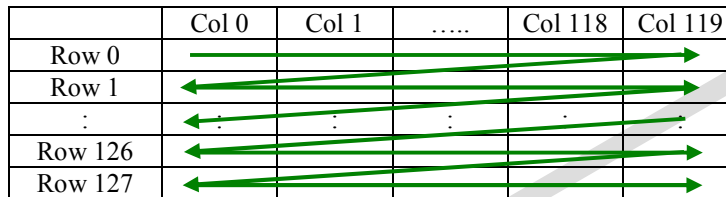
	0				1				118				119				Column address
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG472	SEG473	SEG474	SEG475	SEG476	SEG477	SEG478	SEG479	SEG Outputs
Row 0									..											
Row 1									..											
Row 2									..											
⋮									⋮											
⋮									⋮											
⋮									⋮											
Row 125									..											
Row 126									..											
Row 127									⋮											

10.1.6 Set Re-map & Dual COM Line Mode (A0h)

This command has multiple configurations and each bit setting is described as follows:

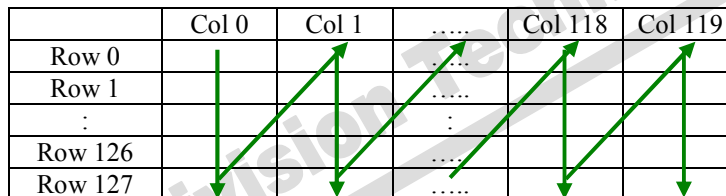
- Address increment mode (A[0])
When A[0] is set to 0, the driver is set as horizontal address increment mode. After the display RAM is read / written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and row address pointer is increased by 1. The sequence of movement of the row and column address point for horizontal address increment mode is shown in Figure 10-3.

Figure 10-3 : Address Pointer Movement of Horizontal Address Increment Mode



When A[0] is set to 1, the driver is set to vertical address increment mode. After the display RAM is read / written, the row address pointer is increased automatically by 1. If the row address pointer reaches the row end address, the row address pointer is reset to row start address and column address pointer is increased by 1. The sequence of movement of the row and column address point for vertical address increment mode is shown in Figure 10-4.

Figure 10-4: Address Pointer Movement of Vertical Address Increment Mode



- Column Address Remap (A[1])
This command bit is made for increasing the layout flexibility of segment signals in OLED module with segment arranged from left to right (when A[1] is set to 0) or vice versa (when A[1] is set to 1), as demonstrated in Figure 10-5.
A[1] = 0 (reset): RAM Column 0 ~ 119 maps to SEG0-SEG3 ~ SEG476-SEG479
A[1] = 1: RAM Column 0 ~ 119 maps to SEG476-SEG479 ~ SEG0-SEG3
- Nibble Remap (A[2])
A[2] = 0 (reset): Data bits direct mapping is performed
A[2] = 1: The four nibbles of the data bus for RAM access are re-mapped
The effects are demonstrated in Figure 10-5.

Figure 10-5: GDDRAM in Gray Scale mode with or without Column Address (A[1]) & Nibble remapping (A[2])

			SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	:	:	:	:	SEG472	SEG473	SEG474	SEG475	SEG476	SEG477	SEG478	SEG479	
Normal, A[1] = 0 & A[2] = 0											:	:	:	:									
Remap, A[1] = 1 & A[2] = 0			SEG479	SEG478	SEG477	SEG476	SEG475	SEG474	SEG473	SEG472	:	:	:	:	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	
Remap, A[1] = 0 & A[2] = 1			SEG3	SEG2	SEG1	SEG0	SEG7	SEG6	SEG5	SEG4	:	:	:	:	SEG475	SEG474	SEG473	SEG472	SEG479	SEG478	SEG477	SEG476	
Normal, A[1] = 1 & A[2] = 1			SEG476	SEG477	SEG478	SEG479	SEG472	SEG473	SEG474	SEG475	:	:	:	:	SEG4	SEG5	SEG6	SEG7	SEG0	SEG1	SEG2	SEG3	SEG476
			0				1				...				76				77				RAM / Column address (HEX)
Normal, A[4] = 0	Remap, A[4] = 1		0				1				...				76				77				
COM0	COM127	0	D1[3:0]	D1[7:4]	D0[3:0]	D0[7:4]	D3[3:0]	D3[7:4]	D2[3:0]	D2[7:4]	:	:	:	:	D237[3:0]	D237[7:4]	D236[3:0]	D236[7:4]	D239[3:0]	D239[7:4]	D238[3:0]	D238[7:4]	
COM1	COM126	1	D241[3:0]	D241[7:4]	D240[3:0]	D240[7:4]	D243[3:0]	D243[7:4]	D242[3:0]	D242[7:4]	:	:	:	:	D477[3:0]	D477[7:4]	D476[3:0]	D476[7:4]	D479[3:0]	D479[7:4]	D478[3:0]	D478[7:4]	
:	:	:																					
COM126	COM1	7E	D30241[3:0]	D30241[7:4]	D30240[3:0]	D30240[7:4]	D30243[3:0]	D30243[7:4]	D30242[3:0]	D30242[7:4]	:	:	:	:	D30477[3:0]	D30477[7:4]	D30476[3:0]	D30476[7:4]	D30479[3:0]	D30479[7:4]	D30478[3:0]	D30478[7:4]	
COM127	COM0	7F	D30481[3:0]	D30481[7:4]	D30480[3:0]	D30480[7:4]	D30483[3:0]	D30483[7:4]	D30482[3:0]	D30482[7:4]	:	:	:	:	D30717[3:0]	D30717[7:4]	D30716[3:0]	D30716[7:4]	D30719[3:0]	D30719[7:4]	D30718[3:0]	D30718[7:4]	
COM Outputs	RAM / Row address (HEX)																						Corresponding to one pixel

- COM scan direction Remap (A[4])**
 This command bit determines the scanning direction of the common for flexible layout of common signals in OLED module either from up to down or vice versa.
 A[1] = 0 (reset): Scan from up to down
 A[1] = 1: Scan from bottom to up
 Details of pin arrangement can be found in Figure 10-5.
- Odd even split of COM pins (A[5])**
 This command bit can set the odd even arrangement of COM pins.
 A[5] = 0 (reset): Disable COM split odd even, pin assignment of common is in sequential as
 COM127 COM126...COM 65 COM64...SEG479...SEG0...COM0 COM1...COM62 COM63
 A[5] = 1: Enable COM split odd even, pin assignment of common is in odd even split as
 COM127 COM125...COM3 COM1...SEG479...SEG0...COM0 COM2...COM124 COM126
 Details of pin arrangement can be found in Figure 10-6.

- Set Dual COM mode (B[4])
 This command bit can set the dual COM mode.
 B[4] = 0 (reset): Disable the dual COM mode, as shown on Figure 10-6
 B[4] = 1: Enable the dual COM mode, details of pin arrangement can be found in Figure 10-7
 Notice that Odd even split of COM pins must be disabled (A[5]=0) and MUX must be set equating to or smaller than 63 (MUX≤63) when dual COM mode is enabled (B[4]=1).

Figure 10-6 : COM Pins Hardware Configuration – 1 (MUX ratio: 128)

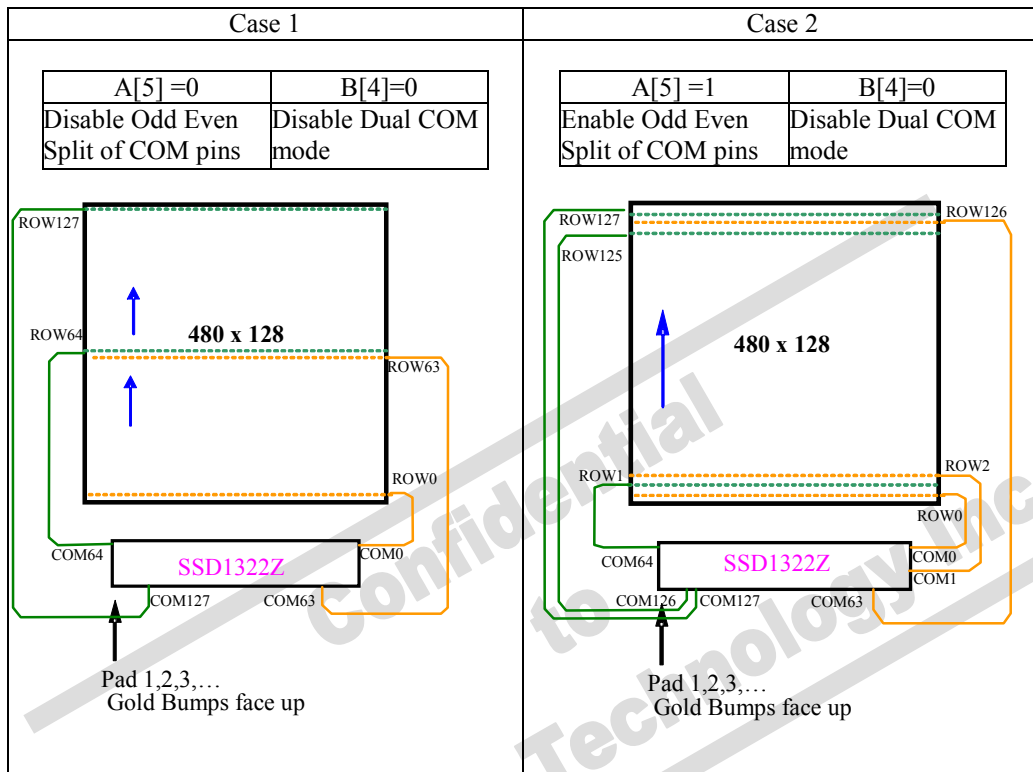
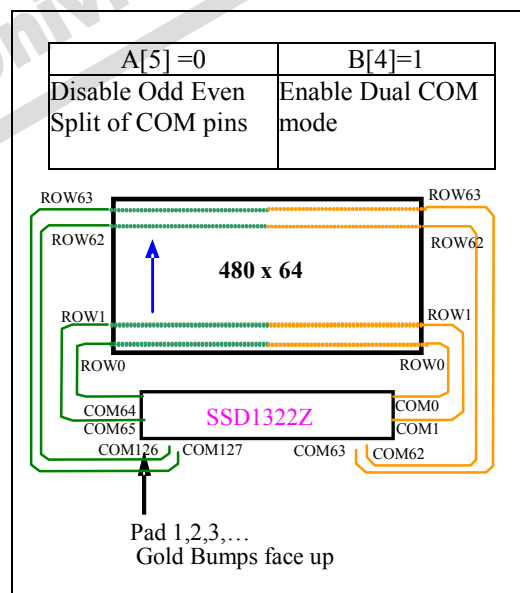






Figure 10-7 : COM Pins Hardware Configuration – 2 (MUX ratio: 64)



10.1.7 Set Display Start Line (A1h)

This command is used to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 127. Figure 10-8 shows an example of using this command when MUX ratio = 128 and MUX ratio = 90 and Display Start Line = 40. In there, “Row” means the graphic display data RAM row.





Figure 10-8 : Example of Set Display Start Line with no Remap

	MUX ratio (CAh) = 128	MUX ratio (CAh) = 128	MUX ratio (CAh) = 90	MUX ratio (CAh) = 90
COM Pin	Display Start Line (A1h) = 0	Display Start Line (A1h) = 40	Display Start Line (A1h) = 0	Display Start Line (A1h) = 40
COM0	ROW0	ROW40	ROW0	ROW40
COM1	ROW1	ROW41	ROW1	ROW41
COM2	ROW2	ROW42	ROW2	ROW42
COM3	ROW3	ROW43	ROW3	ROW43
:	:	:	:	:
:	:	:	:	:
COM48	ROW48	ROW88	ROW48	ROW88
COM49	ROW49	ROW89	ROW49	ROW89
COM50	ROW50	ROW90	ROW50	ROW90
COM51	ROW51	ROW91	ROW51	ROW91
:	:	:	:	:
:	:	:	:	:
COM86	ROW86	ROW126	ROW86	ROW126
COM87	ROW87	ROW127	ROW87	ROW127
COM88	ROW88	ROW0	ROW88	ROW0
COM89	ROW89	ROW1	ROW89	ROW1
COM90	ROW90	ROW2	-	-
COM91	ROW91	ROW3	-	-
:	:	:	:	:
:	:	:	:	:
COM124	ROW124	ROW36	-	-
COM125	ROW125	ROW37	-	-
COM126	ROW126	ROW38	-	-
COM127	ROW127	ROW39	-	-
Display Example				

10.1.8 Set Display Offset (A2h)

This command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0-127. For example, to move the COM39 towards the COM0 direction for 40 lines, the 7-bit data in the second command should be given by 0101000. The figure below shows an example of this command. In there, “Row” means the graphic display data RAM row.

Figure 10-9 : Example of Set Display Offset with no Remap

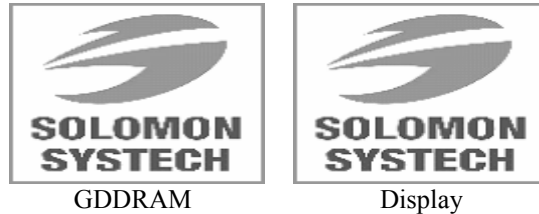
	MUX ratio (CAh) = 128	MUX ratio (CAh) = 128	MUX ratio (CAh) = 90	MUX ratio (CAh) = 90
COM Pin	Display Offset (A2h)=0	Display Offset (A2h)=40	Display Offset (A2h)=0	Display Offset (A2h)=40
COM0	ROW0	ROW40	ROW0	ROW40
COM1	ROW1	ROW41	ROW1	ROW41
COM2	ROW2	ROW42	ROW2	ROW42
COM3	ROW3	ROW43	ROW3	ROW43
.
.
COM48	ROW48	ROW88	ROW48	ROW88
COM49	ROW49	ROW89	ROW49	ROW89
COM50	ROW50	ROW90	ROW50	-
COM51	ROW51	ROW91	ROW51	-
.
.
COM86	ROW86	ROW126	ROW86	-
COM87	ROW87	ROW127	ROW87	-
COM88	ROW88	ROW0	ROW88	ROW0
COM89	ROW89	ROW1	ROW89	ROW1
COM90	ROW90	ROW2	-	ROW2
COM91	ROW91	ROW3	-	ROW3
.
.
COM124	ROW124	ROW36	-	ROW36
COM125	ROW125	ROW37	-	ROW37
COM126	ROW126	ROW38	-	ROW38
COM127	ROW127	ROW39	-	ROW39
Display Example				

10.1.9 Set Display Mode (A4h ~ A7h)

These are single byte command and they are used to set Normal Display, Entire Display ON, Entire Display OFF and Inverse Display.

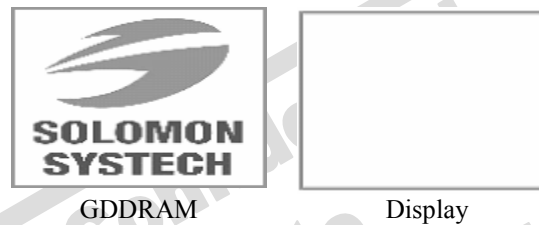
- Normal Display (A4h)
Reset the above effect and turn the data to ON at the corresponding gray level. Figure 10-10 shows an example of Normal Display.

Figure 10-10 : Example of Normal Display



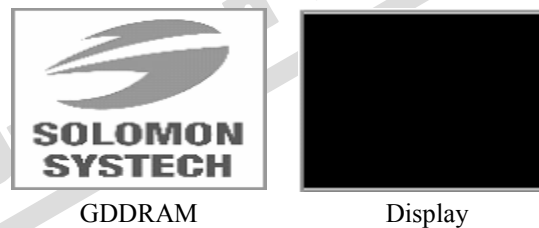
- Set Entire Display ON (A5h)
Force the entire display to be at gray scale “GS15” regardless of the contents of the display data RAM as shown in Figure 10-11.

Figure 10-11 : Example of Entire Display ON



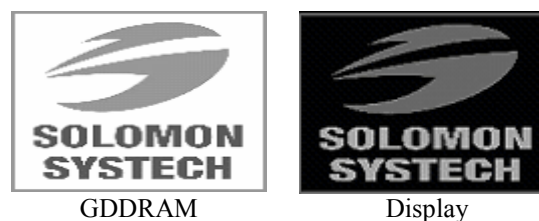
- Set Entire Display OFF (A6h)
Force the entire display to be at gray scale level “GS0” regardless of the contents of the display data RAM as shown in Figure.

Figure 10-12 : Example of Entire Display OFF



- Inverse Display (A7h)
The gray level of display data are swapped such that “GS0” ↔ “GS15”, “GS1” ↔ “GS14”, ... Figure 10-13 shows an example of inverse display.

Figure 10-13 : Example of Inverse Display



10.1.10 Enable Partial Display (A8h)

The partial mode display area is defined this triple byte command. Figure 10-14 shows an example of enabling the partial mode display with start row address A[6:0] = 20h and end start row address B[6:0] = 5Fh at MUX ratio = 128.

Figure 10-14 : Example of Partial Mode Display



10.1.11 Exit Partial Display (A9h)

This single byte command is sent to exit the partial mode display area (command A8h).

10.1.12 Set Function selection (ABh)

This double byte command is used to enable or disable the VDD regulator.

Internal VDD regulator is selected when the bit A[0] is set to 0b, while external VDD is selected when A[0] is set to 1b.

10.1.13 Set Display ON/OFF (AEh / AFh)

These single byte commands are used to turn the OLED panel display ON or OFF.

When the display is ON (command AFh), the selected circuits by Set Master Configuration command will be turned ON. When the display is OFF (command AEh), those circuits will be turned off, the segment is in V_{SS} state and common is in high impedance state.

10.1.14 Set Phase Length (B1h)

This double byte command sets the length of phase 1 and 2 of segment waveform of the driver.

- Phase 1 (A[3:0]): Set the period from 5 to 31 in the unit of 2 DCLKs. A larger capacitance of the OLED pixel may require longer period to discharge the previous data charge completely.
- Phase 2 (A[7:4]): Set the period from 3 to 15 in the unit of DCLKs. A longer period is needed to charge up a larger capacitance of the OLED pixel to the target voltage V_P .

10.1.15 Set Front Clock Divider / Oscillator Frequency (B3h)

This double byte command consists of two functions:

- Front Clock Divide Ratio (A[3:0])
Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 16, with reset value = 1. Please refer to Section 8.5 for the detail relationship of DCLK and CLK.
- Oscillator Frequency (A[7:4])
Program the oscillator frequency F_{osc} which is the source of CLK if CLS pin is pulled HIGH. The 4-bit value results in 16 different frequency settings being available.

10.1.16 Set GPIO (B5h)

This double byte command is used to set the states of GPIO0 and GPIO1 pins. Refer to Table 9-1 for details.

10.1.17 Set Second Pre-charge period (B6h)

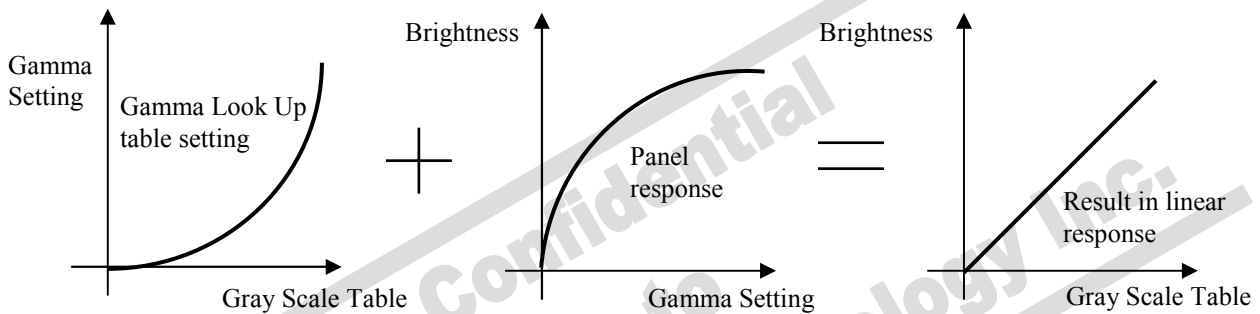
This double byte command is used to set the phase 3 second pre-charge period. The period of phase 3 can be programmed by command B6h and it is ranged from 0 to 15 DCLK's. Please refer to Table 9-1 for the detail information.

10.1.18 Set Gray Scale Table (B8h)

This command is used to set each individual gray scale level for the display. Except gray scale levels GS0 that has no pre-charge and current drive, each gray scale level is programmed in the length of current drive stage pulse width with unit of DCLK. The longer the length of the pulse width, the brighter the OLED pixel when it's turned ON. Following the command B8h, the user has to set the gray scale setting for GS1, GS2, ..., GS14, GS15 one by one in sequence. Refer to Section 8.8 for details.

The setting of gray scale table entry can perform gamma correction on OLED panel display. Since the perception of the brightness scale shall match the image data value in display data RAM, appropriate gray scale table setting like the example shown below (Figure 10-15) can compensate this effect.

Figure 10-15 : Example of Gamma correction by Gamma Look Up table setting



10.1.19 Select Default Linear Gray Scale Table (B9h)

This single byte command reloads the preset linear Gray Scale table as GS0 = Gamma Setting 0, GS1 = Gamma Setting 0, GS2 = Gamma Setting 2, ... GS14 = Gamma Setting 104, GS14 = Gamma Setting 112. Refer to Section 8.8 for details.

10.1.20 Set Pre-charge voltage (BBh)

This double byte command sets the first pre-charge voltage (phase 2) level of segment pins. The level of pre-charge voltage is programmed with reference to V_{CC} . Refer to Table 9-1 for details.

10.1.21 Set V_{COMH} Voltage (BEh)

This double byte command sets the high voltage level of common pins, V_{COMH} . The level of V_{COMH} is programmed with reference to V_{CC} . Refer to Table 9-1 for details.

10.1.22 Set Contrast Current (C1h)

This double byte command is used to set Contrast Setting of the display. The chip has 256 contrast steps from 00h to FFh. The segment output current I_{SEG} increases linearly with the contrast step, which results in brighter display.

10.1.23 Master Current Control (C7h)

This double byte command is to control the segment output current by a scaling factor. The chip has 16 master control steps, with the factor ranges from 1 [0000b] to 16 [1111b – default]. The smaller the master current value, the dimmer the OLED panel display is set.

For example, if original segment output current is 160uA at scale factor = 16, setting scale factor to 8 would reduce the current to 80uA.

10.1.24 Set Multiplex Ratio (CAh)

This double byte command switches default 1:128 multiplex mode to any multiplex mode from 16 to 128. For example, when multiplex ratio is set to 16, only 16 common pins are enabled. The starting and the ending of the enabled common pins are depended on the setting of “Display Offset” register programmed by command A2h. Figure 10-8 and Figure 10-9 show examples of setting the multiplex ratio through command CAh.

10.1.25 Set Command Lock (FDh)

This command is used to lock the OLED driver IC from accepting any command except itself. After entering FDh 16h (A[2]=1b), the OLED driver IC will not respond to any newly-entered command (except FDh 12h A[2]=0b) and there will be no memory access. This is call “Lock” state. That means the OLED driver IC ignore all the commands (except FDh 12h A[2]=0b) during the “Lock” state.

Entering FDh 12h (A[2]=0b) can unlock the OLED driver IC. That means the driver IC resume from the “Lock” state. And the driver IC will then respond to the command and memory access.

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11 MAXIMUM RATINGS

Table 11-1 : Maximum Ratings

(Voltage Reference to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to 2.75	V
V_{CC}		-0.5 to 21.0	V
V_{DDIO}		-0.5 to V_{CI}	V
V_{CI}		-0.3 to 4.0	V
V_{SEG}	SEG output voltage	0 to V_{CC}	V
V_{COM}	COM output voltage	0 to $0.9 \cdot V_{CC}$	V
V_{in}	Input voltage	$V_{SS}-0.3$ to $V_{DDIO}+0.3$	V
T_A	Operating Temperature	-40 to +85	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

*This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

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12 DC CHARACTERISTICS

Conditions (Unless otherwise specified):

Voltage referenced to V_{SS}

V_{DD} = 2.4 to 2.6V

V_{CI} = 2.4 to 3.5V (V_{CI} must be larger than or equal to V_{DD})

T_A = 25°C

Table 12-1 : DC Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	
V _{CC}	Operating Voltage	-	10	-	20	V	
V _{DD}	Logic Supply Voltage	-	2.4	-	2.6	V	
V _{CI}	Low voltage power supply	-	2.4	-	3.5	V	
V _{DDIO}	Power Supply for I/O pins	-	1.65	-	V _{CI}	V	
V _{OH}	High Logic Output Level	I _{out} = 100uA	0.9*V _{DDIO}	-	V _{DDIO}	V	
V _{OL}	Low Logic Output Level	I _{out} = 100uA	0	-	0.1*V _{DDIO}	V	
V _{IH}	High Logic Input Level	-	0.8*V _{DDIO}	-	V _{DDIO}	V	
V _{IL}	Low Logic Input Level	-	0	-	0.2*V _{DDIO}	V	
I _{SLP_VDD}	V _{DD} Sleep mode Current	V _{CI} = V _{DDIO} = 2.8V, V _{CC} = OFF V _{DD} (external) = 2.5V, Display OFF, No panel attached	-	-	10	uA	
I _{SLP_VDDIO}	V _{DDIO} Sleep mode Current	V _{CI} = V _{DDIO} = 2.8V, V _{CC} = OFF Display OFF, No panel attached	External V _{DD} =	-	-	10	uA
			Internal V _{DD}	-	-	10	uA
I _{SLP_VCI}	V _{CI} Sleep mode Current	V _{CI} = V _{DDIO} = 2.8V, V _{CC} = OFF Display OFF, No panel attached	External V _{DD} =	-	-	10	uA
			Enable Internal V _{DD} during Sleep mode	-	-	40	uA
			Disable Internal V _{DD} during Sleep mode	-	-	10	uA
I _{DD}	V _{DD} Supply Current	V _{CI} = 3.3V, V _{CC} = 18V, V _{DDIO} = 2.5V, External V _{DD} = 2.5V, Display ON, No panel attached, contrast = FF	-	TBD	TBD	uA	
I _{DDIO}	V _{DDIO} Supply Current	V _{CI} = 3.3V, V _{CC} = 18V, V _{DDIO} = 2.5V, Display ON, No panel attached, contrast = FF	External V _{DD} = 2.5V	-	TBD	TBD	uA
			Internal V _{DD} = 2.5V	-	TBD	TBD	uA
I _{CI}	V _{CI} Supply Current	V _{CI} = 3.3V, V _{CC} = 18V, V _{DDIO} = 2.5V, Display ON, No panel attached, contrast = FF	External V _{DD} = 2.5V	-	TBD	TBD	uA
			Internal V _{DD} = 2.5V	-	TBD	TBD	uA
I _{CC}	V _{CC} Supply Current	V _{CI} = 3.3V, V _{CC} = 18V, V _{DDIO} = 2.5V, Display ON, No panel attached, contrast = FF	External V _{DD} = 2.5V	-	TBD	TBD	mA
			Internal V _{DD} = 2.5V	-	TBD	TBD	mA
I _{SEG}	Segment Output Current Setting V _{CC} =18V, I _{REF} =10uA	Contrast = FF	-	TBD	TBD	uA	
		Contrast = 7F	-	TBD	TBD	uA	
		Contrast = 3F	-	TBD	TBD	uA	
Dev	Segment output current uniformity	Dev = (I _{SEG} - I _{MID}) / I _{MID} I _{MID} = (I _{MAX} + I _{MIN}) / 2 I _{SEG} = Segment current at contrast FF	-3	-	3	%	
Adj. Dev	Adjacent pin output current uniformity (contrast = FF)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])	-2	-	2	%	

13 AC CHARACTERISTICS

Conditions:

Voltage referenced to V_{SS}

V_{DD} = 2.4 to 2.6V

T_A = 25°C

Table 13-1 : AC Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
F _{OSC} ⁽¹⁾	Oscillation Frequency of Display Timing Generator	V _{DD} = 2.5V	TBD	TBD	TBD	MHz
F _{FRM}	Frame Frequency for 128 MUX Mode	480x128 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F _{OSC} * 1 / (D * K * 128) ⁽²⁾	-	Hz
t _{RES}	Reset low pulse width (RES#)	-	2000	-	-	ns

Note

⁽¹⁾ F_{OSC} stands for the frequency value of the internal oscillator and the value is measured when command B3h A[7:4] is in default value.

⁽²⁾ D: divide ratio

K: Phase 1 period + Phase 2 period + X

X: DCLKs in current drive period.

Default K is 9 + 7 + 122 = 138

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Table 13-2 : 6800-Series MCU Parallel Interface Timing Characteristics

($V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{DDIO} = 1.6V$, $V_{CI} = 3.3V$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read)	120	-	-	ns
	Chip Select Low Pulse Width (write)	60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read)	60	-	-	ns
	Chip Select High Pulse Width (write)	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 13-1 : 6800-series MCU parallel interface characteristics

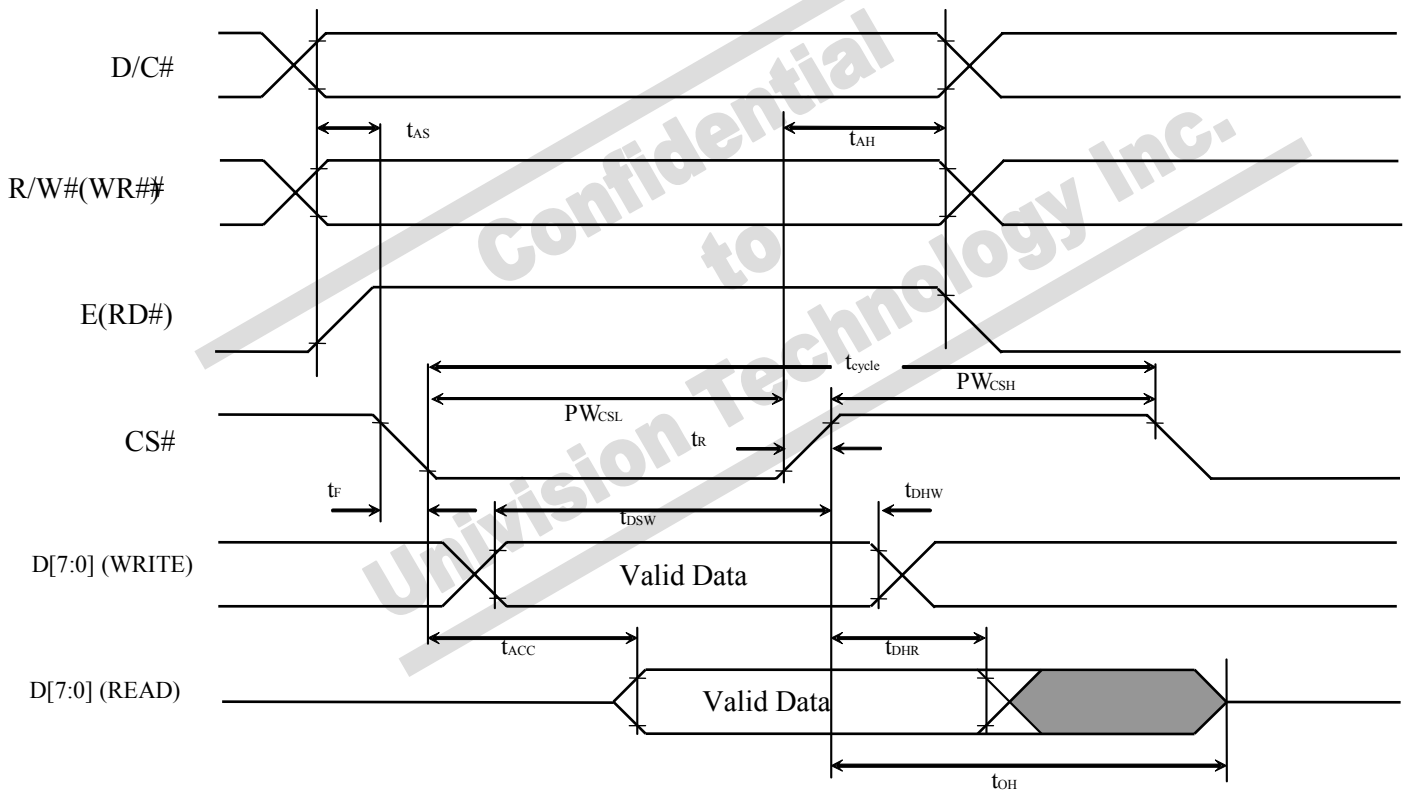


Table 13-3 : 8080-Series MCU Parallel Interface Timing Characteristics

($V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{DDIO} = 1.6V$, $V_{CI} = 3.3V$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 13-2 : 8080-series MCU parallel interface characteristics

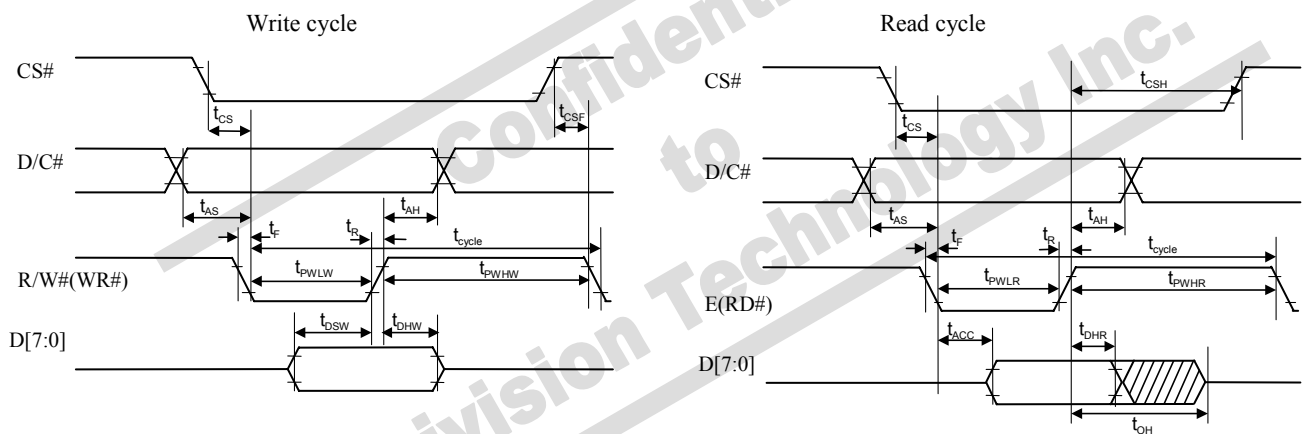


Table 13-4 : Serial Interface Timing Characteristics (4-wire SPI)

($V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{DDIO} = 1.6V$, $V_{CI} = 3.3V$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 13-3 : Serial interface characteristics (4-wire SPI)

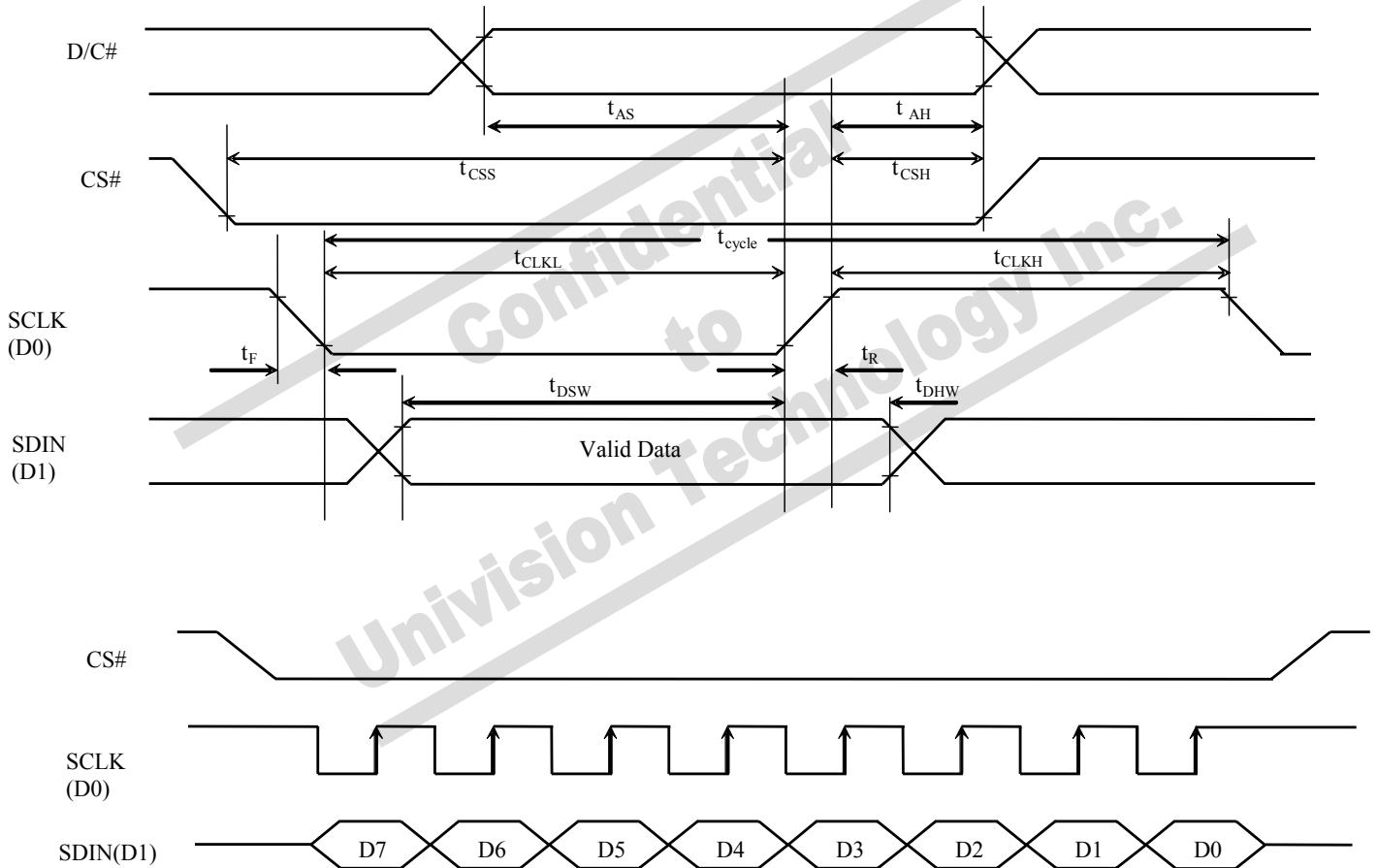
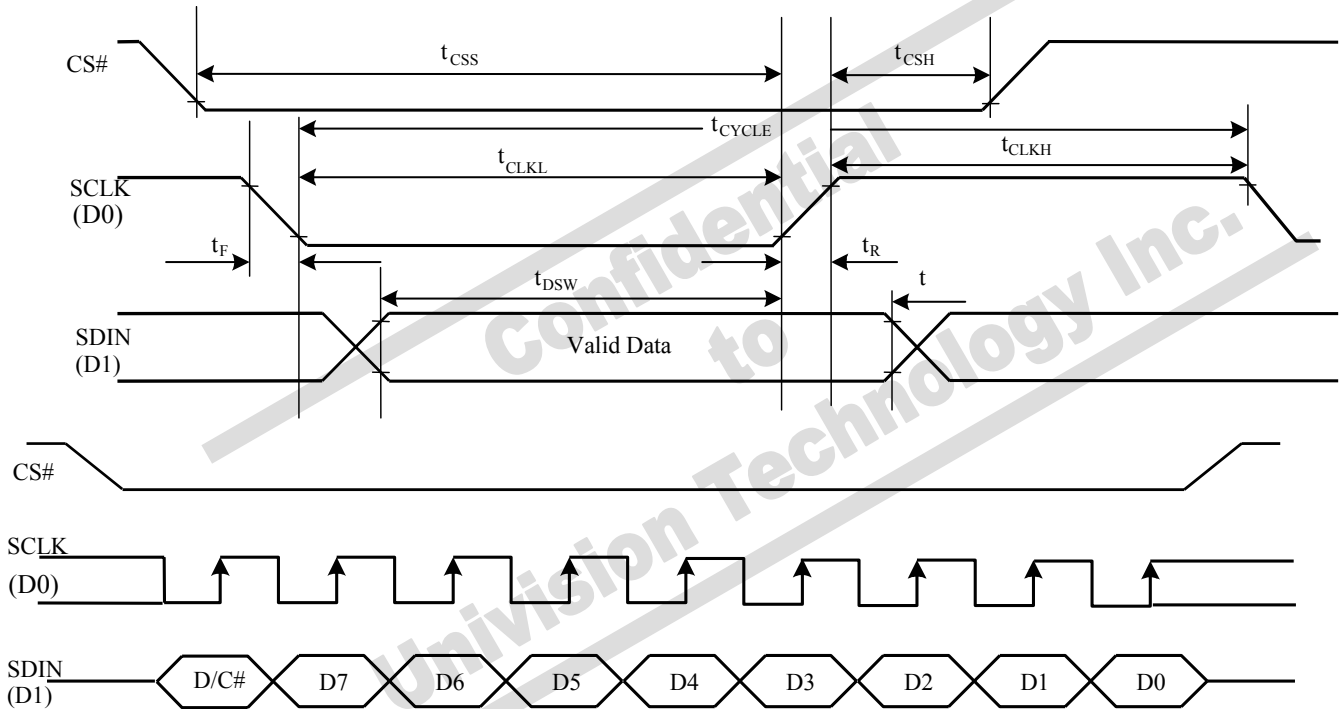


Table 13-5: Serial Interface Timing Characteristics (3-wire SPI)

($V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{DDIO} = 1.6V$, $V_{CI} = 3.3V$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

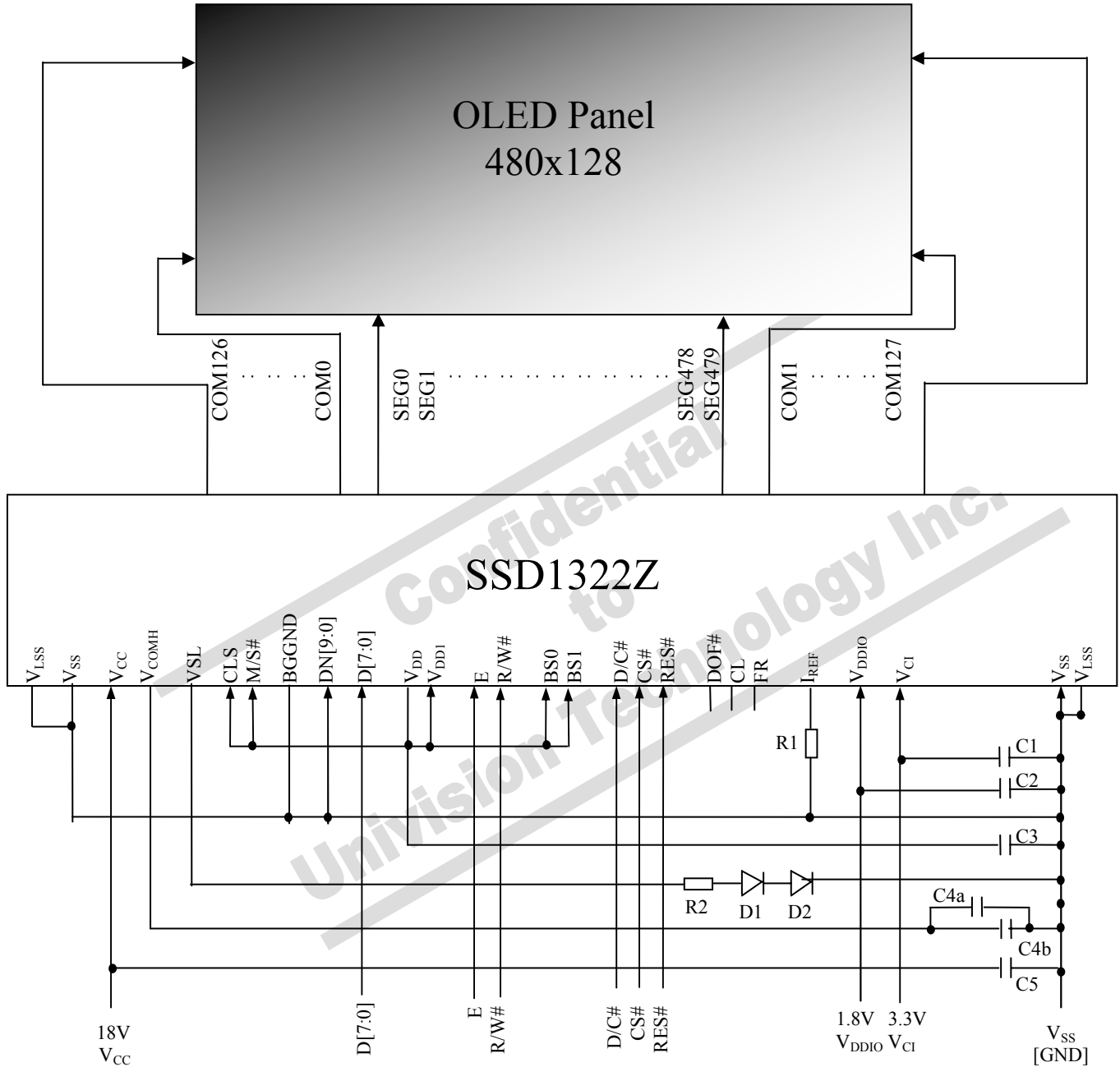
Figure 13-4: Serial interface characteristics (3-wire SPI)



14 APPLICATION EXAMPLES

Figure 14-1 : SSD1322 application example for 8-bit 6800-parallel interface mode (Internal regulated V_{DD})

The configuration for 8-bit 6800-parallel interface mode, externally V_{CC} is shown in the following diagram:
(V_{CI} = 3.3V (V_{CI} must be > 2.6V), Internal regulated V_{DD} = 2.5V, V_{DDIO} = 1.8V, external V_{CC} = 18V, I_{REF} = 10uA)



Voltage at I_{REF} = V_{CC} - 6V. For V_{CC} = 18V, I_{REF} = 10uA:

$$R1 = (\text{Voltage at } I_{REF} - V_{SS}) / I_{REF}$$

$$= (18 - 6) / 10\mu$$

$$= 1.2M\Omega$$

$$R2 = 50\Omega, 1/8W^{(1)}$$

$$D1 - D2 = V_{th} = 0.7V, 1N4148^{(1)}$$

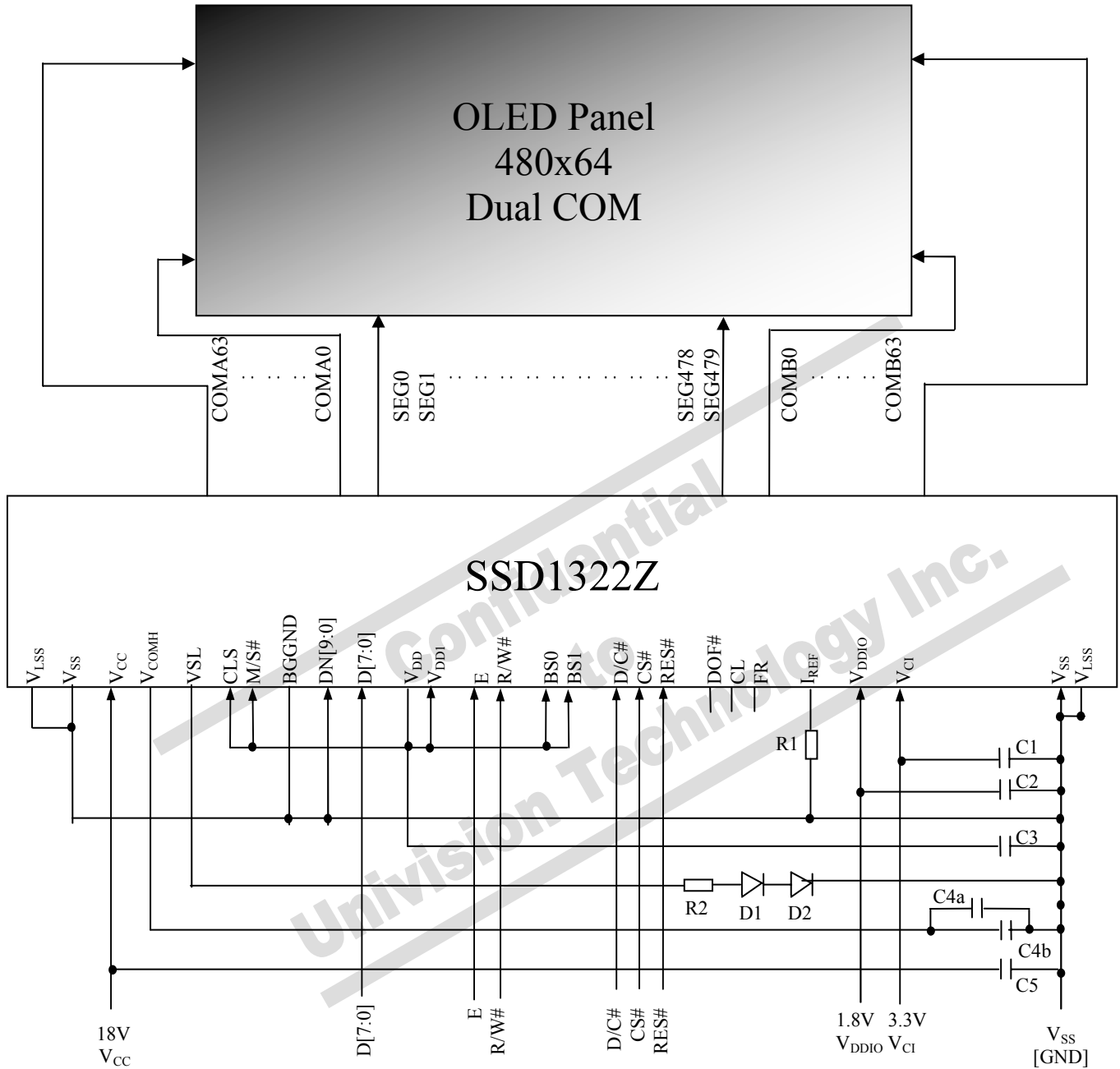
$$C1 \sim C3: 1\mu F, C4a \text{ and } C5: 4.7\mu F, C4b: 0.1\mu F$$

Note

⁽¹⁾ The value is recommended value. Select appropriate value against module application.

Figure 14-2 : SSD1322 application example for 8-bit 6800-parallel interface, dual COM mode (Internal V_{DD})

The configuration for 8-bit 6800-parallel interface mode, externally V_{CC} is shown in the following diagram:
 (V_{CI}=3.3V (V_{CI} must be > 2.6V), Internal regulated V_{DD} = 2.5V, V_{DDIO} = 1.8V, external V_{CC} = 18V, I_{REF} = 10uA)



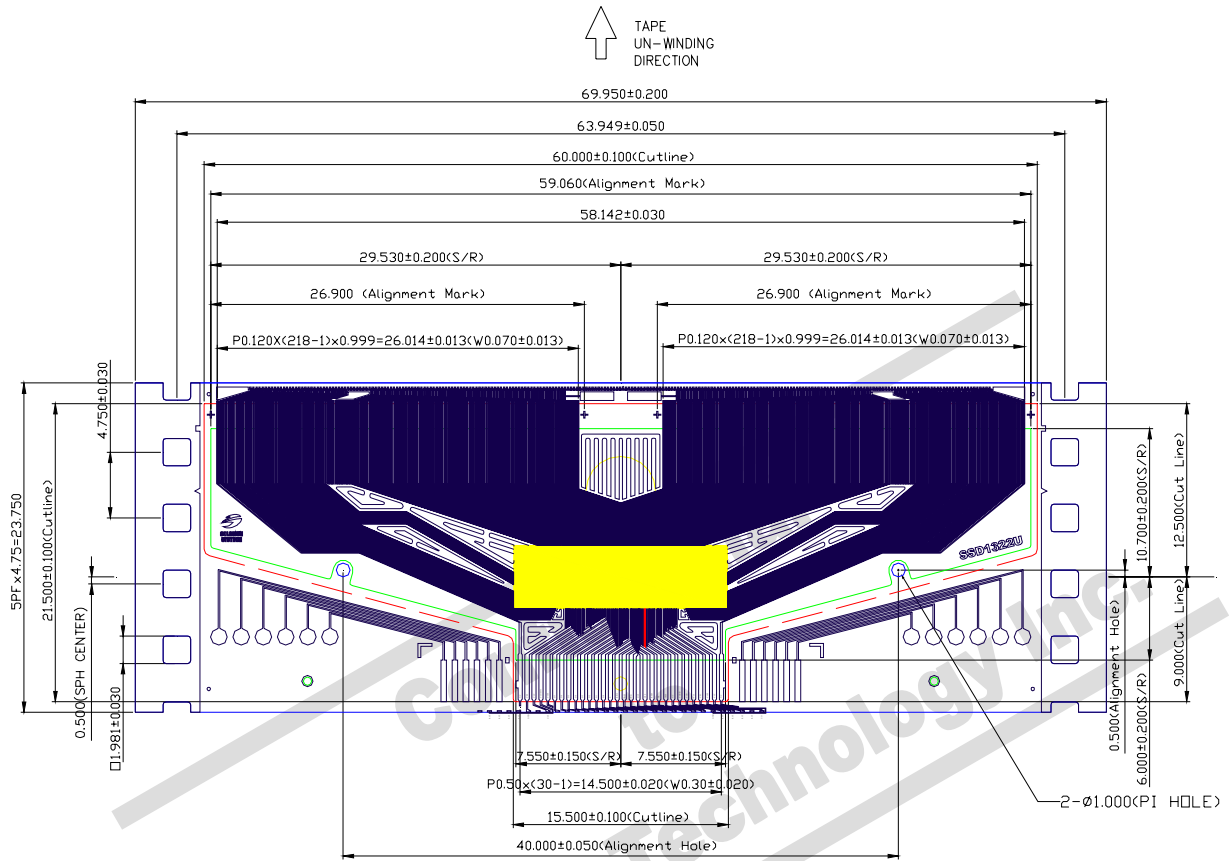
Voltage at I_{REF} = V_{CC} - 6V. For V_{CC} = 18V, I_{REF} = 10uA:
 $R1 = (\text{Voltage at } I_{REF} - V_{SS}) / I_{REF}$
 $= (18 - 6) / 10\mu$
 $= 1.2M\Omega$
 R2 = 50Ω, 1/8W⁽¹⁾
 D1 - D2 = V_{th} = 0.7V, 1N4148⁽¹⁾
 C1 ~ C3: 1uF, C4a and C5: 4.7uF, C4b: 0.1uF

Note
⁽¹⁾The value is recommended value. Select appropriate value against module application.

15 PACKAGE INFORMATION

15.1 SSD1322UR1 detail dimension

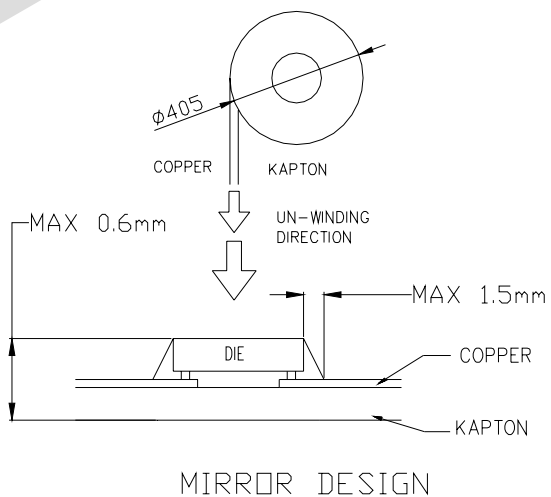
Figure 15-1: SSD1322UR1 Detail Dimension



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NOTE:

1. GENERAL TOLERANCE: ±0.05mm
2. MATERIAL
 - PI: 38±4um
 - CU: 8±2um
 - SR: 15±10um
 - (OTHER TOLERANCE: ±0.200mm)
3. Sn PLATING 0.16±0.050um
4. TAPSITE: 5 SPH, 23.75mm




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