

150-mA Low-Noise LDO Regulator With Error Flag and Discharge Option

FEATURES

- Ultra Low Dropout—130 mV at 150-mA Load
- Low Noise—75 μV_{rms} (10-Hz to 100-kHz Bandwidth)
- Out-of-Regulation Error Flag (power good)
- Shutdown Control
- 110- μA Ground Current at 150-mA Load
- Fast Start-Up (50 μs)
- 1.5% Guaranteed Output Voltage Accuracy (1.2 V, 2%)
- 300-mA Peak Output Current Capability
- Uses Low ESR Ceramic Capacitors
- Fast Line and Load Transient Response ($\leq 30 \mu\text{s}$)
- 1- μA Maximum Shutdown Current
- Output Current Limit
- Reverse Battery Protection
- Built-in Short Circuit and Thermal Protection



- Output—Auto-Discharge In Shutdown Mode
- Fixed 1.2, 1.8, 2.5, 2.6, 2.8, 2.85, 3.0, 3.3, 5.0-V Output Voltage Options
- Thin SOT23-5 Package

APPLICATIONS

- Cellular Phones, Wireless Handsets
- Noise-Sensitive Electronic Systems, Laptop and Palmtop Computers
- PDAs
- Pagers
- Digital Cameras
- MP3 Player
- Wireless Modem

DESCRIPTION

The Si91842 is a 150-mA CMOS LDO (low dropout) voltage regulator. It is the perfect choice for low voltage, low power applications. An ultra low ground current and ultra fast turn-on make this part attractive for battery operated power systems. The Si91842 also offers ultra low dropout voltage to prolong battery life in portable electronics. Systems requiring a quiet voltage source will benefit from the Si91842's low output noise. The Si91842 is designed to maintain regulation while delivering 300-mA peak current, making it ideal for systems that have a high surge current upon turn-on.

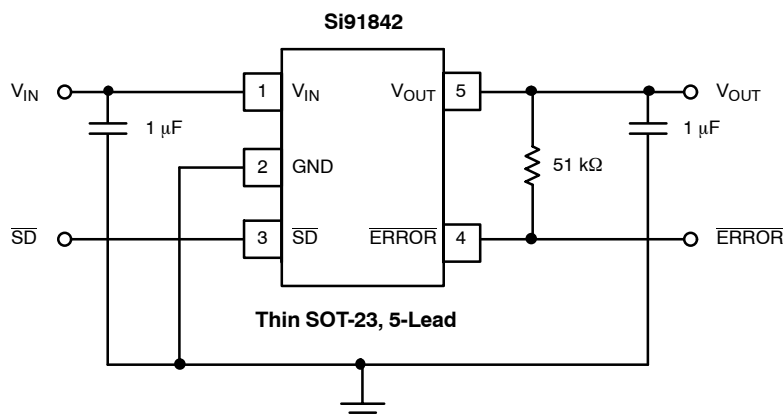
pull-down circuit is built into the Si91842 to clamp the output voltage when it rises beyond normal regulation. The Si91842 automatically discharges the output voltage by connecting the output to ground through a 100- Ω n-channel MOSFET when the device is put in shutdown mode.

The Si91842 features reverse battery protection to limit reverse current flow to approximately 1- μA in the event reversed battery is applied at the input, thus preventing damage to the IC.

For better transient response and regulation, an active

The Si91842 is available in both standard and lead (Pb)-free packages.

TYPICAL APPLICATION CIRCUIT





ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings	
Input Voltage, V_{IN} to GND	-6.0 to 6.5 V
ERROR, V_{SD} (See Detailed Description)	-0.3 V to V_{IN}
Output Current, I_{OUT}	Short Circuit Protected
Output Voltage, V_{OUT}	-0.3 V to $V_{IN} + 0.3$ V
Package Power Dissipation, $(P_d)^b$	440 mW

Package Thermal Resistance, $(\theta_{JA})^a$	180°C/W
Maximum Junction Temperature, $T_{J(max)}$	150°C
Storage Temperature, T_{STG}	-65°C to 150°C

- Notes
- Device mounted with all leads soldered or welded to PC board.
 - Derate 5.5 mW/°C above $T_A = 70^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Input Voltage, V_{IN}	2 V to 6 V
Input Voltage, V_{SD}	0 V to V_{IN}

Operating Ambient Temperature, T_A	-40°C to 85°C
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$C_{IN} = C_{OUT} = 1 \mu\text{F}$ (ceramic)
 Maximum ESR of C_{OUT} : 0.4 Ω

SPECIFICATIONS								
Parameter	Symbol	Test Conditions Unless Specified $T_A = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 1$ V, $I_{OUT} = 1$ mA, $C_{IN} = 1 \mu\text{F}$, $C_{OUT} = 1.0 \mu\text{F}$, $V_{SD} = 1.5$ V		Temp ^a	Limits -40 to 85°C			Unit
					Min ^b	Typ ^c	Max ^b	
Input Voltage Range	V_{IN}			Full	2		6	V
Output Voltage Accuracy		$1 \text{ mA} \leq I_{OUT} \leq 150 \text{ mA}$	$V_{OUT} \geq 1.8 \text{ V}$	Room	-1.5	1	1.5	%
				Full	-2.5	1	2.5	
				Room	-2.0	1	2.0	
				Full	-3.0	1	3.0	
Line Regulation ($V_{OUT} \leq 3$ V)	$\frac{\Delta V_{OUT} \times 100}{\Delta V_{IN} \times V_{OUT(nom)}}$	From $V_{IN} = V_{OUT(nom)} + 1$ V to $V_{OUT(nom)} + 2$ V		Full	-0.06		0.18	%V
Line Regulation (3.0 V < $V_{OUT} \leq 3.6$ V)				Full	0		0.3	
Line Regulation (5-V Version)				Full	0		0.4	
Dropout Voltage ^{d, g} ($V_{OUT(nom)} \geq 2.6$ V)	$V_{IN} - V_{OUT}$	$I_{OUT} = 1$ mA		Room		1		mV
		$I_{OUT} = 50$ mA		Room		45	80	
		$I_{OUT} = 150$ mA		Full		50	90	
		$I_{OUT} = 150$ mA		Room		130	180	
Dropout Voltage ^{d, g} ($V_{OUT(nom)} < 2.6$ V, $V_{IN} \geq 2$ V)	$V_{IN} - V_{OUT}$	$I_{OUT} = 50$ mA		Full			220	
		$I_{OUT} = 50$ mA		Room		65	100	
		$I_{OUT} = 150$ mA		Full			120	
		$I_{OUT} = 150$ mA		Room		190	250	
Ground Pin Current ^{e, g} ($V_{OUT(nom)} \leq 3$ V)	I_{GND}	$I_{OUT} = 0$ mA		Full			300	μA
		$I_{OUT} = 150$ mA		Room		100	150	
		$I_{OUT} = 150$ mA		Full			180	
		$I_{OUT} = 150$ mA		Room		110	200	
Ground Pin Current ^{e, g} ($V_{OUT(nom)} > 3$ V)	I_{GND}	$I_{OUT} = 0$ mA		Full			230	
		$I_{OUT} = 0$ mA		Room		110	170	
		$I_{OUT} = 150$ mA		Full			200	
		$I_{OUT} = 150$ mA		Room		120	200	
Peak Output current	$I_{O(peak)}$	$V_{OUT} \geq 0.95 \times V_{OUT(nom)}$, $t_{PW} = 2$ ms		Full	300			mA
Output Noise Voltage	e_N	$V_{OUT} = 2.6$ V, BW = 10 Hz to 100 kHz, 0 mA < I_{OUT} < 150 mA		Room		75		$\mu\text{V(rms)}$

SPECIFICATIONS								
Parameter	Symbol	Test Conditions Unless Specified $T_A = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT} = 1.0\ \mu\text{F}$, $V_{SD} = 1.5\text{ V}$	Temp ^a	Limits -40 to 85°C			Unit	
				Min ^b	Typ ^c	Max ^b		
Ripple Rejection	$\Delta V_{OUT}/\Delta V_{IN}$	$I_{OUT} = 150\text{ mA}$	f = 1 kHz Room		60		dB	
			f = 10 kHz Room		40			
			f = 100 kHz Room		30			
Dynamic Line Regulation	$\Delta V_{O(\text{line})}$	$V_{IN} : V_{OUT(nom)} + 1\text{ V to } V_{OUT(nom)} + 2\text{ V}$ $t_r/t_f = 2\ \mu\text{s}$, $I_{OUT} = 150\text{ mA}$	Room		20		mV	
Dynamic Load Regulation	$\Delta V_{O(\text{load})}$	$I_{OUT} : 1\text{ mA to } 150\text{ mA}$, $t_r/t_f = 2\ \mu\text{s}$	Room		25			
Thermal Shutdown Junction Temperature	$T_{J(S/D)}$		Room		150		°C	
Thermal Hysteresis	T_{HYST}		Room		20			
Reverse current	I_R	$V_{IN} = -6.0\text{ V}$	Room		1		μA	
Short Circuit Current	I_{SC}	$V_{OUT} = 0\text{ V}$	Room		700		mA	
Shutdown								
Shutdown Supply Current	$I_{CC(\text{off})}$	$V_{SD} = 0\text{ V}$	Room		0.1	1	μA	
SD Pin Input Voltage	V_{SD}	High = Regulator ON (Rising)	Full	1.5		V_{IN}	V	
		Low = Regulator OFF (Falling)	Full			0.4		
Auto Discharge Resistance	R_{DIS}	Si91842 Only	Room		100		Ω	
SD Pin Input Current ^f	$I_{IN(SD)}$	$V_{SD} = 1.5\text{ V}$, $V_{IN} = 6\text{ V}$	Room		0.7		μA	
SD Hysteresis	$V_{HYST(SD)}$		Full		150		mV	
V_{OUT} Turn-On Time	t_{ON}	V_{SD} (See Figure 1), $I_{LOAD} = 100\text{ mA}$	Room		50		μS	
ERROR Output								
ERROR High Leakage	I_{OFF}	ERROR ≤ V_{IN} , V_{OUT} in Regulation	Full			1	μA	
ERROR Low Voltage	V_{OL}	$I_{SINK} = 0.5\text{ mA}$	Full			0.4	V	
ERROR Voltage Threshold	V_{ERROR}	V_{OUT} Below $V_{OUT(nom)}^g$, $V_{IN} \geq 2\text{ V}$ V_{OUT} Falling, $I_{OUT} = 1\text{ mA}$, $V_{OUT(nom)} \geq 2\text{ V}$	Full	-2	-4	-6	%	
		$V_{OUT(nom)}^g < 2\text{ V}$, $V_{IN} > 2\text{ V}$	Full		-4			
ERROR Voltage Threshold Hysteresis	$V_{HYST(ERROR)}$		Room		1.5			

Notes

- Room = 25°C, Full = -40 to 85°C.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Dropout voltage is defined as the input to output differential voltage at which the output voltage drops 2% below the output voltage measured with a 1-V differential, provided that V_{IN} does not drop below 2.0 V.
- Ground current is specified for normal operation as well as “drop-out” operation.
- The device’s shutdown pin includes a typical 2-MΩ internal pull-down resistor connected to ground.
- $V_{OUT(nom)}$ is V_{OUT} when measured with a 1-V differential to V_{IN} .

TIMING WAVEFORMS

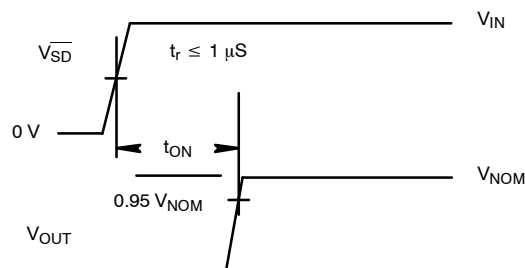
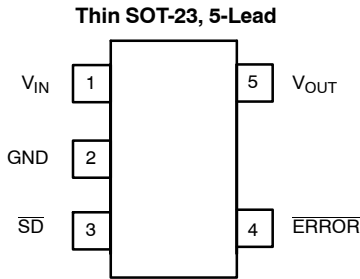


FIGURE 1. Timing Diagram for Power-Up

PIN CONFIGURATION



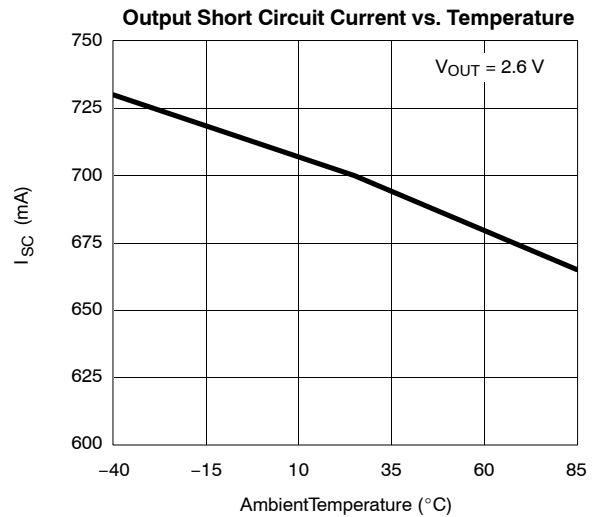
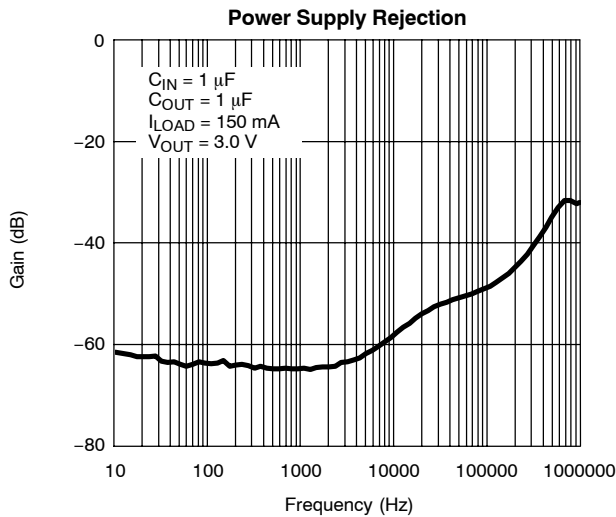
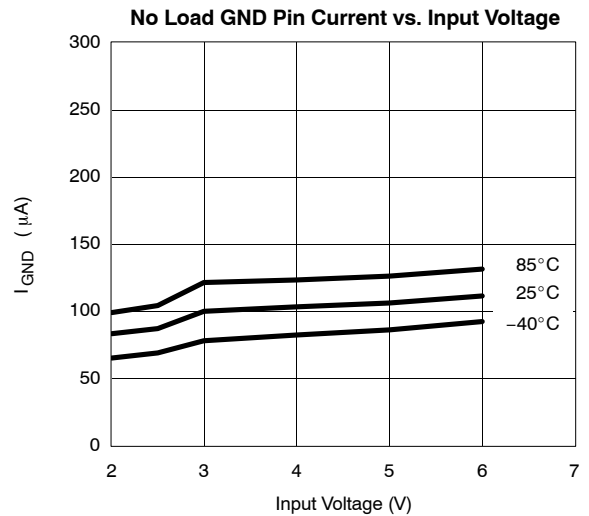
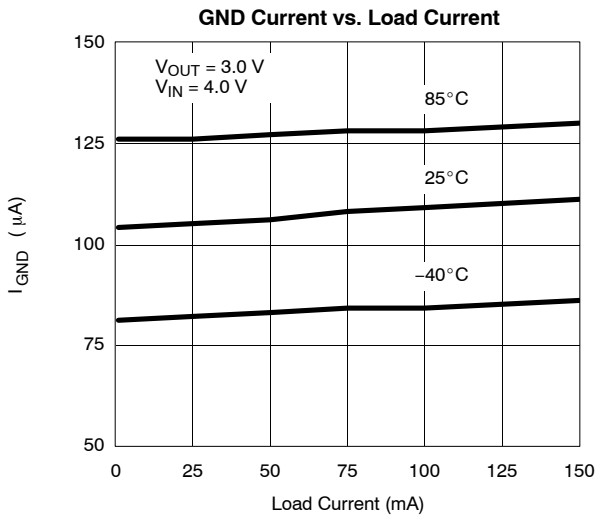
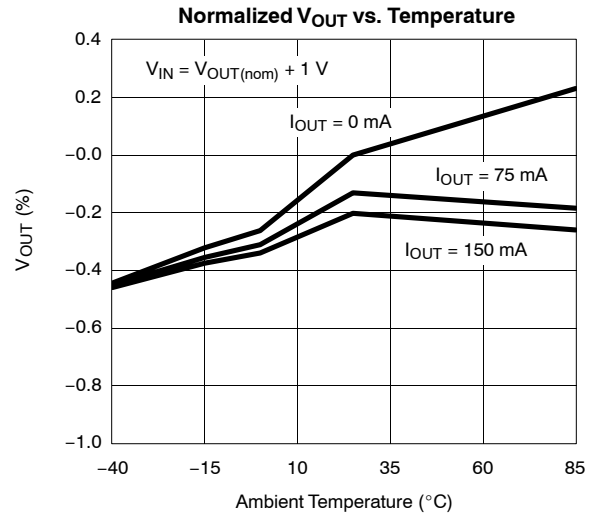
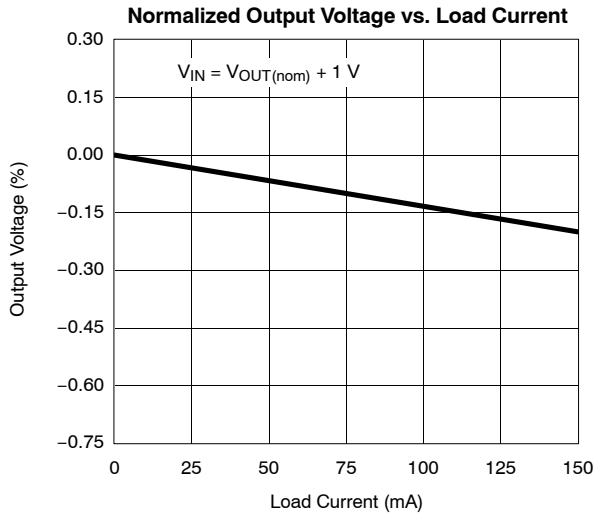
PIN DESCRIPTION		
Pin No.	Name	Function
1	V_{IN}	Input supply pin. Bypass this pin with a 1- μ F ceramic or tantalum capacitor to ground
2	GND	Ground pin. For better thermal capability, directly connected to large ground plane
3	\overline{SD}	By applying less than 0.4 V to this pin, the device will be turned off. Connect this pin to V_{IN} if unused
4	\overline{ERROR}	The open drain output is an error flag output which goes low when V_{OUT} drops 4% below its nominal voltage.
5	V_{OUT}	Output voltage. Connect C_{OUT} between this pin and ground.

ORDERING INFORMATION—Si91842

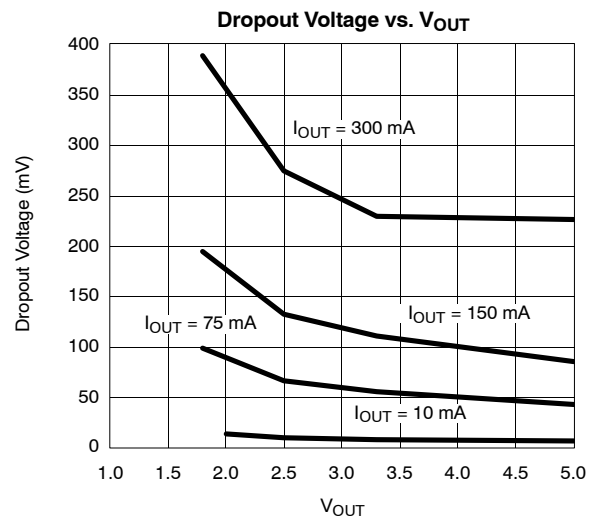
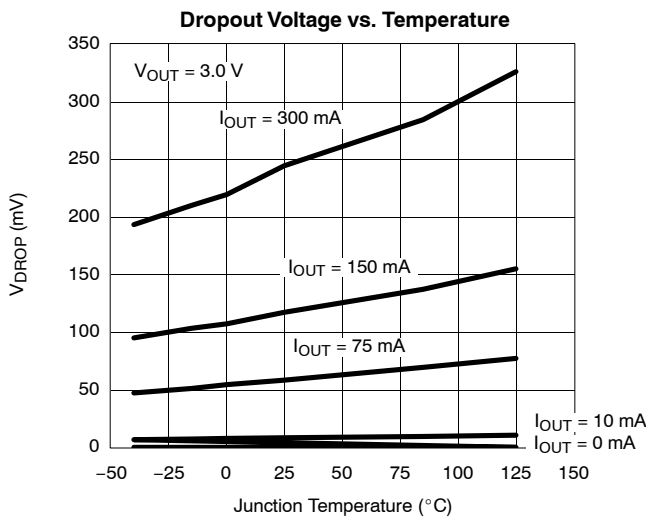
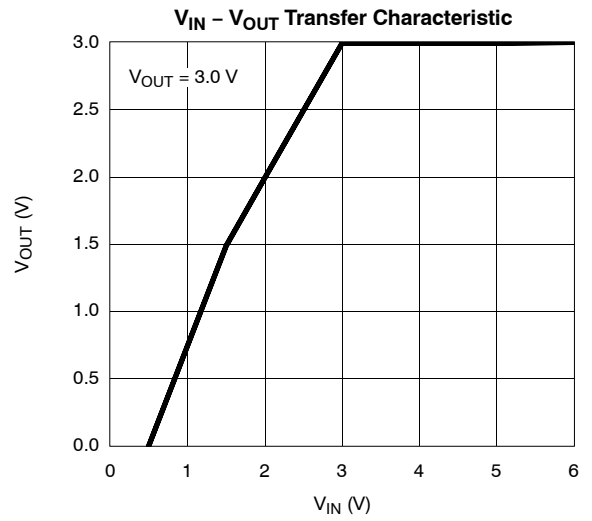
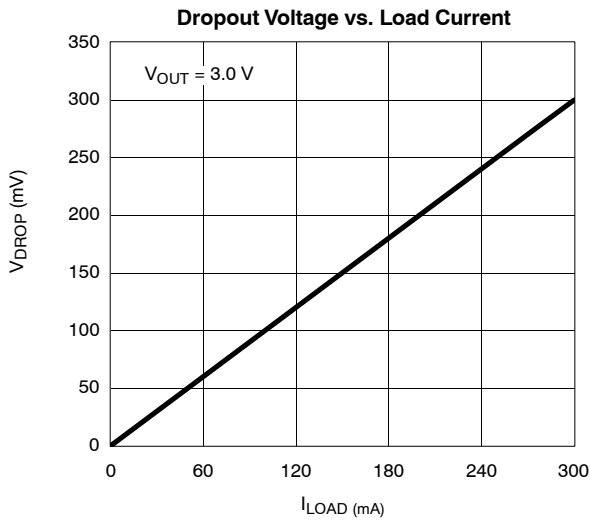
Part Number	Lead (Pb)-Free Part Number	Marking	Voltage	Temperature Range	Package
Si91842DT-12-T1	Si91842DT-12-T1—E3	J8LLL	1.2	-40 to 85°C	ThinSOT23-5
Si91842DT-18-T1	Si91842DT-18-T1—E3	C8LLL	1.8		
Si91842DT-25-T1	Si91842DT-25-T1—E3	D1LLL	2.5		
Si91842DT-26-T1	Si91842DT-26-T1—E3	D2LLL	2.6		
Si91842DT-28-T1	Si91842DT-28-T1—E3	D4LLL	2.8		
Si91842DT-285-T1	Si91842DT-285—E3	D5LLL	2.85		
Si91842DT-29-T1	Si91842DT-29-T1—E3	D6LLL	2.9		
Si91842DT-30-T1	Si91842DT-30-T1—E3	D7LLL	3.0		
Si91842DT-33-T1	Si91842DT-33-T1—E3	D8LLL	3.3		
Si91842DT-50-T1	Si91842DT-50-T1—E3	E1LLL	5.0		

LLL = Lot Code

TYPICAL CHARACTERISTICS (INTERNALLY REGULATED, 25°C UNLESS NOTED)

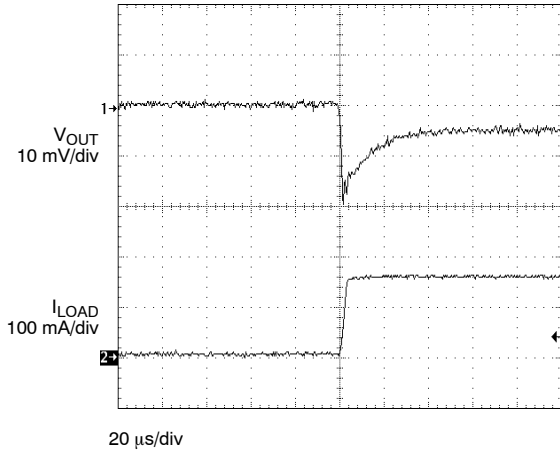


TYPICAL CHARACTERISTICS (INTERNALLY REGULATED, 25°C UNLESS NOTED)



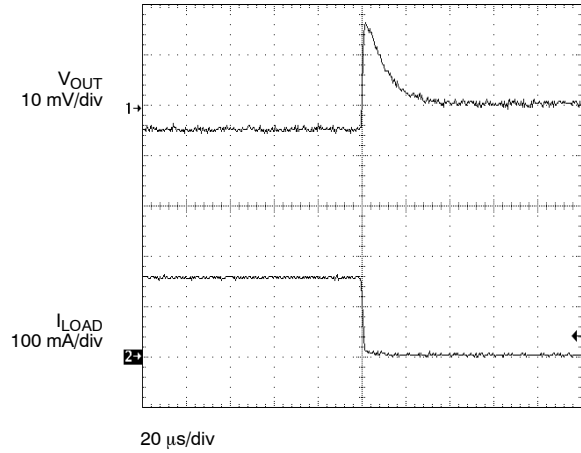
TYPICAL WAVEFORMS

Load Transient Response-1



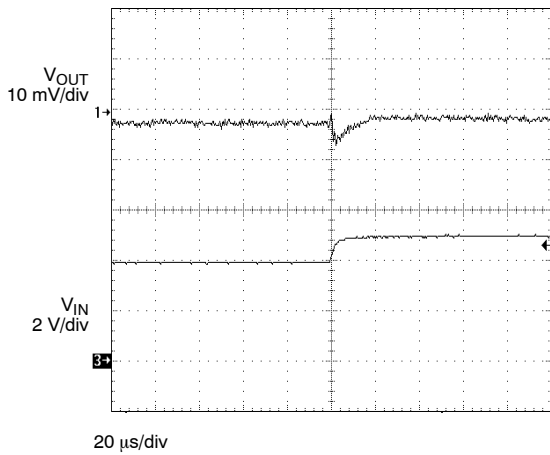
$V_{OUT} = 3.0\text{ V}$
 $C_{OUT} = 1\ \mu\text{F}$
 $I_{LOAD} = 1\ \text{to}\ 150\ \text{mA}$
 $t_{rise} = 2\ \mu\text{sec}$

Load Transient Response-2



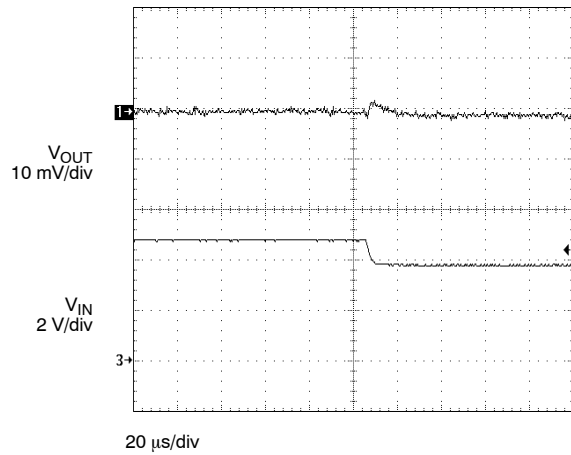
$V_{OUT} = 3.0\text{ V}$
 $C_{OUT} = 1\ \mu\text{F}$
 $I_{LOAD} = 150\ \text{to}\ 1\ \text{mA}$
 $t_{fall} = 2\ \mu\text{sec}$

Line Transient Response-1



$V_{INSTEP} = 4\ \text{to}\ 5\ \text{V}$
 $V_{OUT} = 3\ \text{V}$
 $C_{OUT} = 1\ \mu\text{F}$
 $C_{IN} = 1\ \mu\text{F}$
 $I_{LOAD} = 150\ \text{mA}$
 $t_{rise} = 5\ \mu\text{sec}$

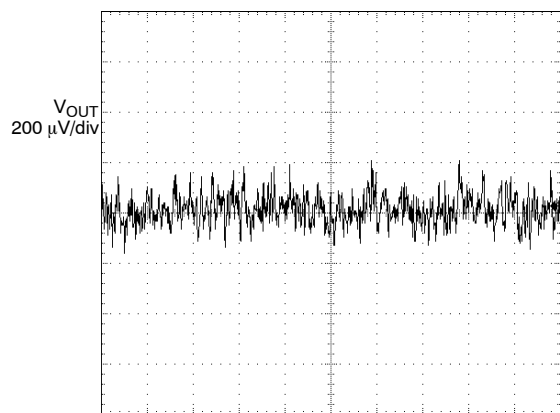
Line Transient Response-2



$V_{INSTEP} = 5\ \text{to}\ 4\ \text{V}$
 $V_{OUT} = 3\ \text{V}$
 $C_{OUT} = 1\ \mu\text{F}$
 $C_{IN} = 1\ \mu\text{F}$
 $I_{LOAD} = 150\ \text{mA}$
 $t_{fall} = 5\ \mu\text{sec}$

TYPICAL WAVEFORMS

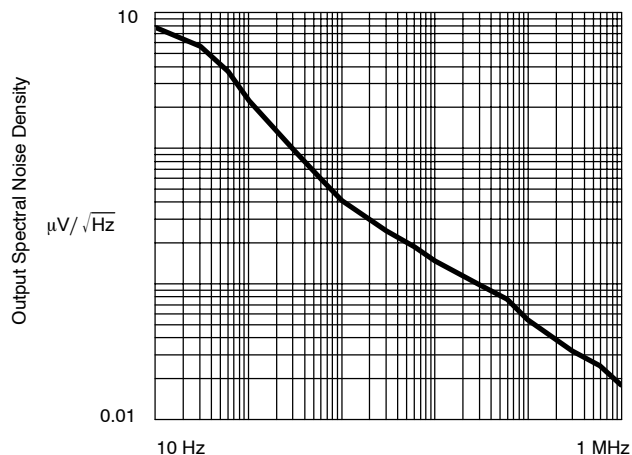
Output Noise



4 ms/div

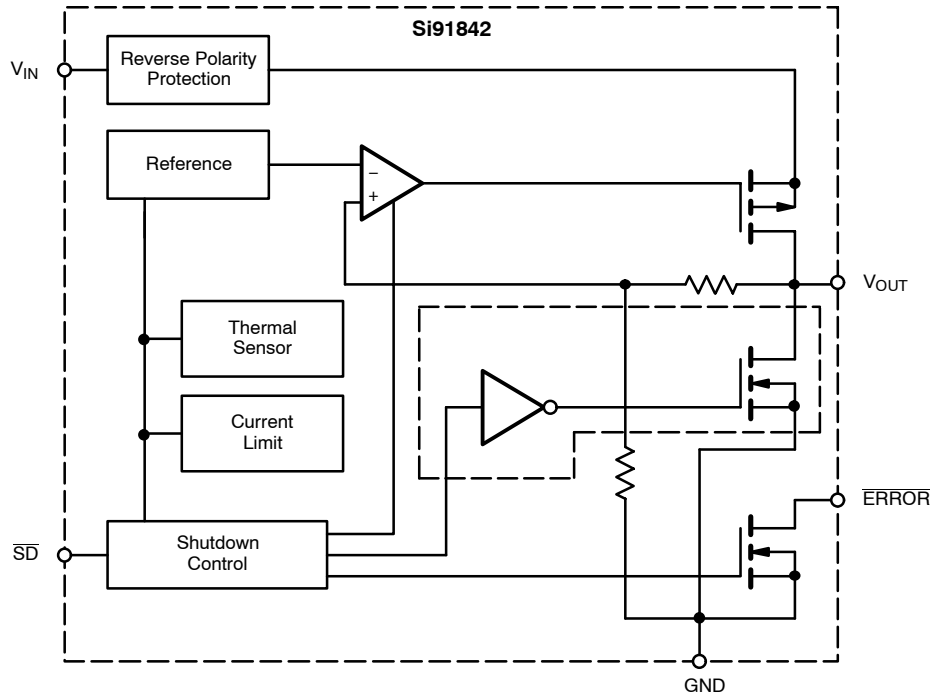
$V_{IN} = 4\text{ V}$
 $V_{OUT} = 3\text{ V}$
 $I_{OUT} = 150\text{ mA}$
BW = 10 Hz to 100 kHz

Noise Spectrum



$V_{IN} = 4\text{ V}$
 $V_{OUT} = 3\text{ V}$
 $I_{LOAD} = 150\text{ mA}$

BLOCK DIAGRAM



DETAILED DESCRIPTION

The Si91842 is a low-noise, low drop-out and low quiescent current linear voltage regulator, packaged in a small footprint Thin SOT23-5 package. The Si91842 can supply loads up to 150 mA. As shown in the block diagram, the circuit consists of a bandgap reference, error amplifier, p-channel pass transistor and feedback resistor string. Additional blocks, not shown in the block diagram, include a precise current limiter, reverse battery and current protection, and thermal sensor.

Thermal Overload Protection

The thermal overload protection limits the total power dissipation and protects the device from being damaged. When the junction temperature exceeds 150°, the device turns the p-channel pass transistor off.

Reverse Battery Protection

The Si91842 has a battery reverse protection circuitry that disconnects the internal circuitry when V_{IN} drops below the GND voltage. There is no current drawn in such an event. When the \overline{SD} pin is hardwired to V_{IN} , the user must connect the \overline{SD} pin to V_{IN} via a 100-k Ω resistor if reverse battery

protection is desired. Hardwiring the \overline{SD} pin directly to the V_{IN} pin is allowed when reverse battery protection is not desired.

ERROR

\overline{ERROR} is an open drain output that goes low when V_{OUT} is less than 4% of its normal value. To obtain a logic level output, connect a pull-up resistor from \overline{ERROR} to V_{OUT} or any other voltage equal to or less than V_{IN} . \overline{ERROR} pin is high impedance (off) when \overline{SD} pin is low.

Auto-Discharge/No-Discharge

V_{OUT} has an internal 100- Ω (typ.) discharge path to ground when \overline{SD} pin is low for the Si91842. The Si91844 does not have a discharge path when the \overline{SD} pin is low.

Stability

The circuit is stable with only a small output capacitor equal to 6 nF/mA (= 1 μ F @ 150 mA). Since the bandwidth of the error amplifier is around 1–3 MHz and the dominant pole is at the output node, the capacitor should be capacitive in this range, i.e., for 150-mA load current, an ESR <0.4 Ω is necessary. Parasitic inductance of about 10 nH can be tolerated.

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