

Dual P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^{a, e}	Q _g (Typ.)
- 20	0.058 at V _{GS} = - 4.5 V	- 4	8
	0.094 at V _{GS} = - 2.5 V	- 4	

FEATURES

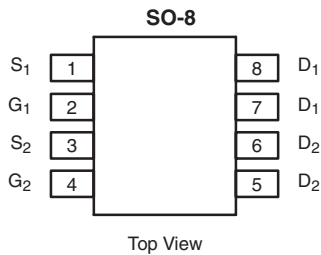
- Halogen-free Option Available
- TrenchFET[®] Power MOSFET
- 100 % R_g and UIS Tested



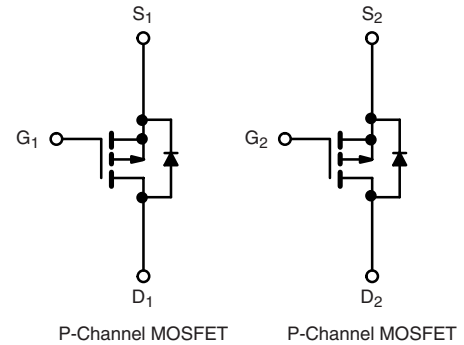
RoHS
COMPLIANT

APPLICATIONS

- Load Switch
- DC/DC Converter



Ordering Information: Si9933CDY-T1-E3 (Lead (Pb)-free)
Si9933CDY-T1-GE3 (Lead (Pb)-free and Halogen-free)



ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	- 20	V	
Gate-Source Voltage	V _{GS}	± 12		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	- 4 ^e	
		T _C = 70 °C	- 4 ^e	
		T _A = 25 °C	- 4 ^{b, c, e}	
		T _A = 70 °C	- 3.8 ^{b, c}	
Pulsed Drain Current (10 μs Pulse Width)	I _{DM}	- 20	A	
Source-Drain Current Diode Current	I _S	T _C = 25 °C		- 2.5
		T _A = 25 °C		- 1.7 ^{b, c}
Single Pulse Avalanche Current	I _{AS}	- 6	mJ	
Single-Pulse Avalanche Energy	E _{AS}	1.8		
Maximum Power Dissipation	P _D	T _C = 25 °C	3.1	
		T _C = 70 °C	2	
		T _A = 25 °C	2 ^{b, c}	
		T _A = 70 °C	1.28 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 50 to 150	°C	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit		Unit
		Typical	Maximum	
Maximum Junction-to-Ambient ^{b, d}	R _{thJA}	52	62.5	°C/W
Maximum Junction-to-Foot (Drain)	R _{thJF}	32	40	

Notes:

- Based on T_C = 25 °C.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under Steady State conditions is 110 °C/W.
- Package Limited.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	- 20			V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		- 19		mV/ $^\circ\text{C}$	
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			3.1			
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	- 0.6		- 1.4	V	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			- 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$			- 1	μA	
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			- 10		
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = \leq -5\text{ V}, V_{GS} = -10\text{ V}$	- 20			A	
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -4.8\text{ A}$		0.048	0.058	Ω	
		$V_{GS} = -2.5\text{ V}, I_D = -1\text{ A}$		0.075	0.094		
Forward Transconductance ^b	g_{fs}	$V_{DS} = -10\text{ V}, I_D = -4.8\text{ A}$		11		S	
Dynamic^a							
Input Capacitance	C_{iss}	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		665		pF	
Output Capacitance	C_{oss}			140			
Reverse Transfer Capacitance	C_{rss}			115			
Total Gate Charge	Q_g	$V_{DS} = -10\text{ V}, V_{GS} = -10\text{ V}, I_D = -4.8\text{ A}$		17	26	nC	
		$V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -4.8\text{ A}$		8	12		
Q_{gs}			2				
Q_{gd}			3				
Gate Resistance	R_g	$f = 1\text{ MHz}$	1.2	6	12	Ω	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 2.6\text{ }\Omega$ $I_D \cong -3.8\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		6	12	ns	
Rise Time	t_r			15	23		
Turn-Off Delay Time	$t_{d(off)}$			26	39		
Fall Time	t_f			9	18		
Turn-On Delay Time	$t_{d(on)}$		$V_{DD} = -10\text{ V}, R_L = 2.6\text{ }\Omega$ $I_D \cong -3.8\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		21		32
Rise Time	t_r				50		75
Turn-Off Delay Time	$t_{d(off)}$			29	44		
Fall Time	t_f			13	20		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			- 2.5		A
Pulse Diode Forward Current ^a	I_{SM}				- 20		
Body Diode Voltage	V_{SD}	$I_S = -3.8\text{ A}$		- 0.77	- 1.2	V	
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -3.8\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		30	45	ns	
Body Diode Reverse Recovery Charge	Q_{rr}				17	26	nC
Reverse Recovery Fall Time	t_a				16		ns
Reverse Recovery Rise Time	t_b				14		

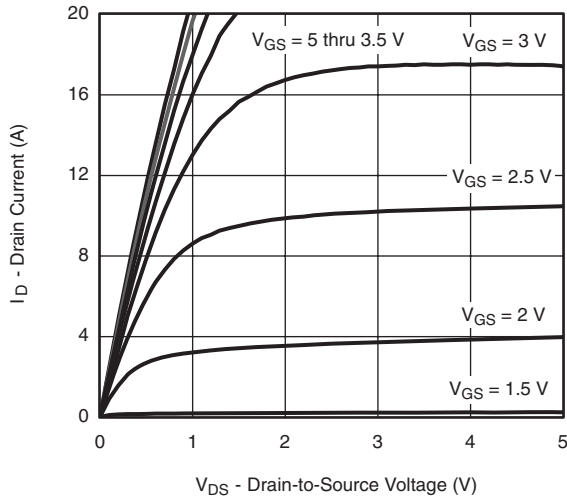
Notes:

a. Guaranteed by design, not subject to production testing.

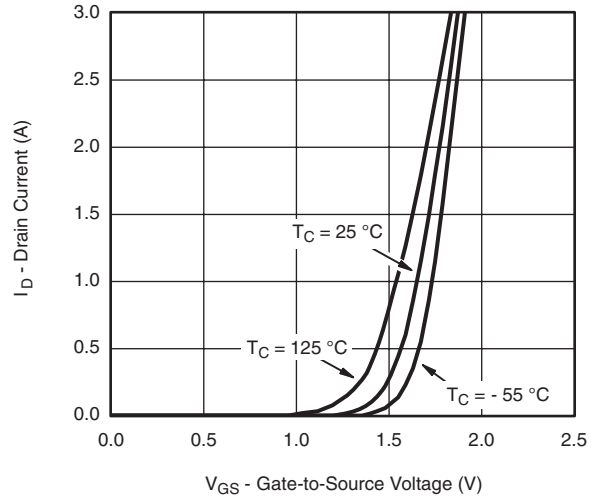
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

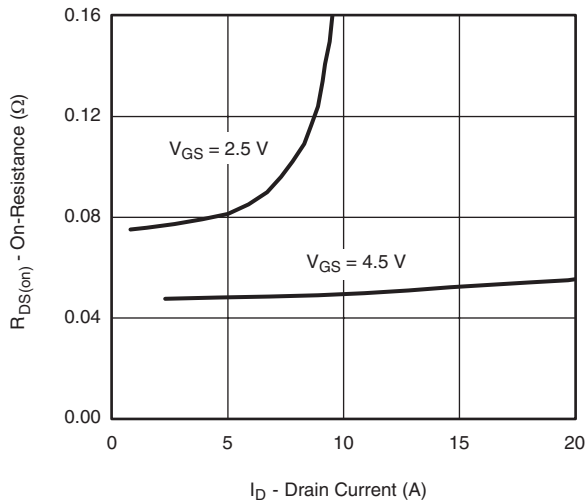
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



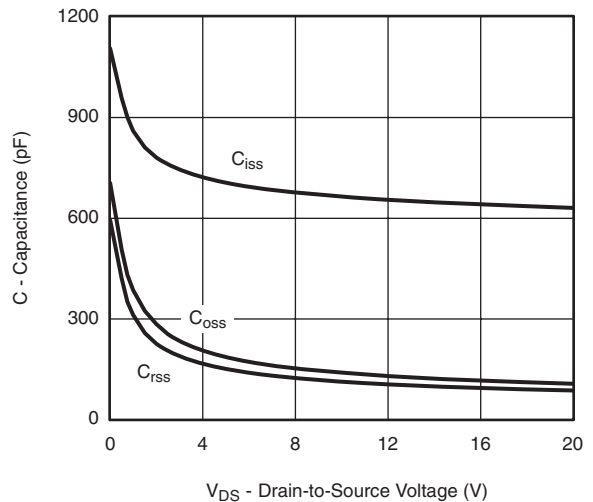
Output Characteristics



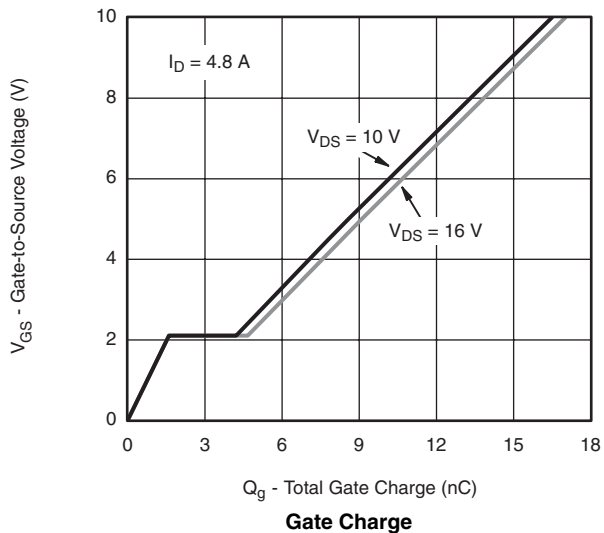
Transfer Characteristics



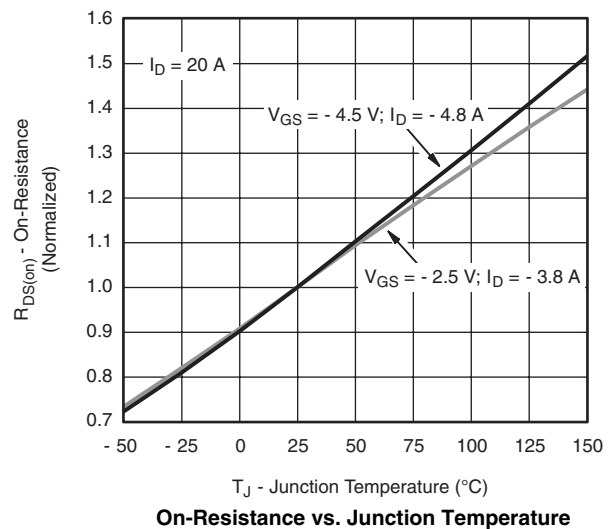
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



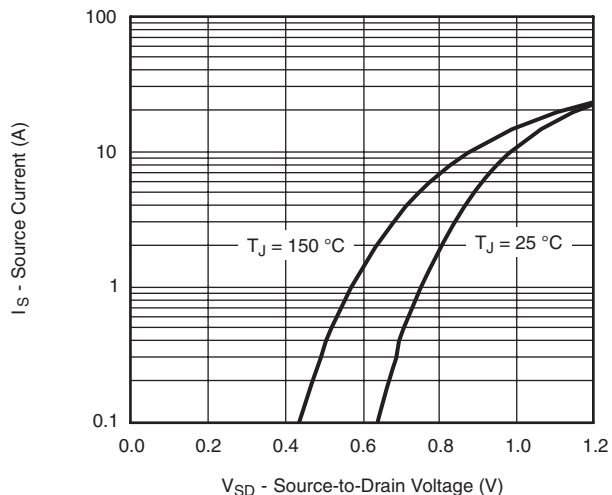
Gate Charge



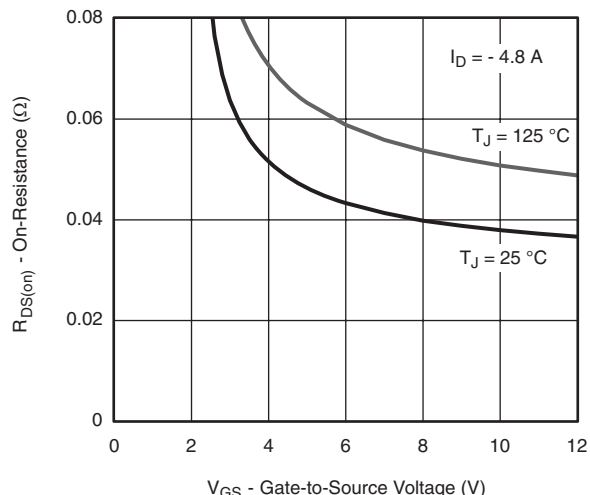
On-Resistance vs. Junction Temperature



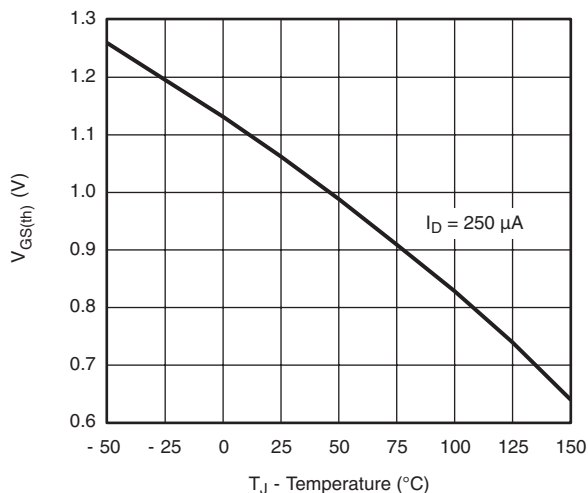
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



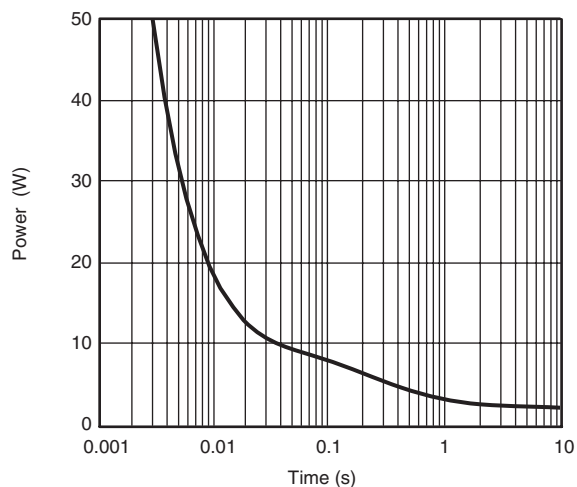
Source-Drain Diode Forward Voltage



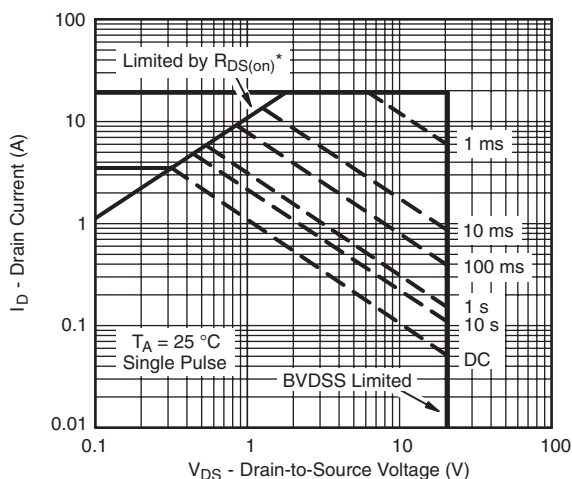
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

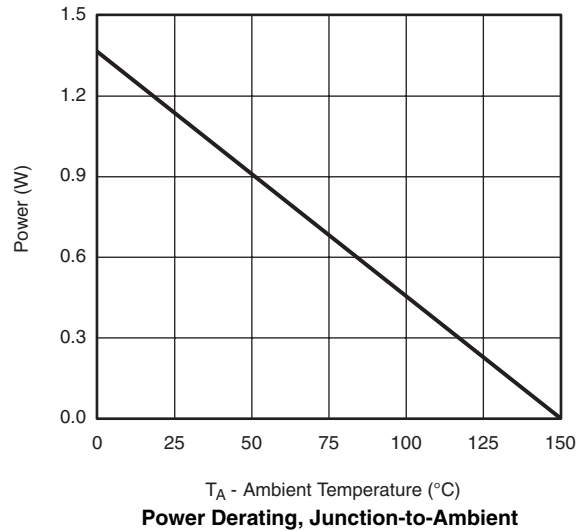
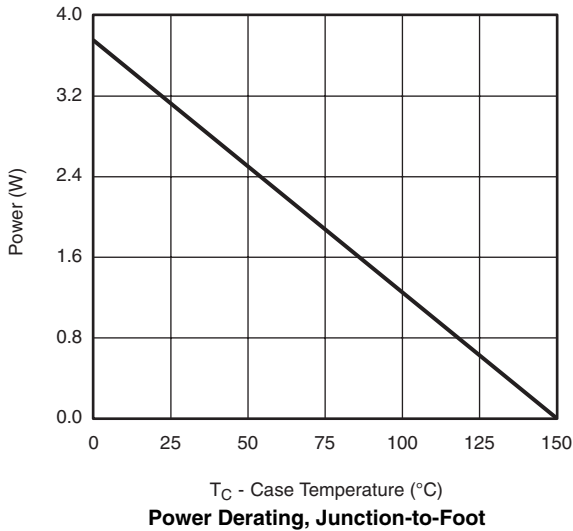
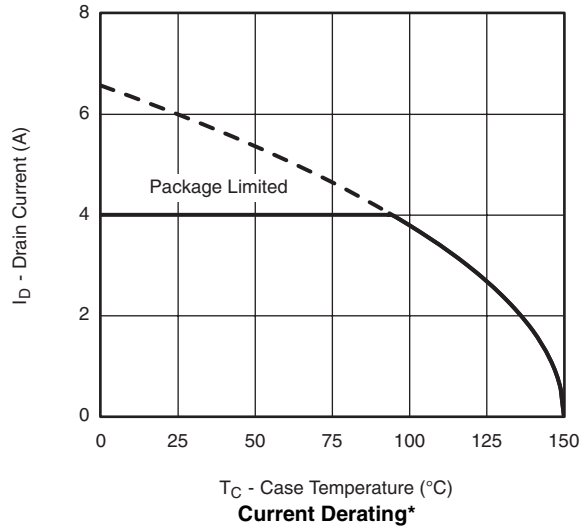


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient



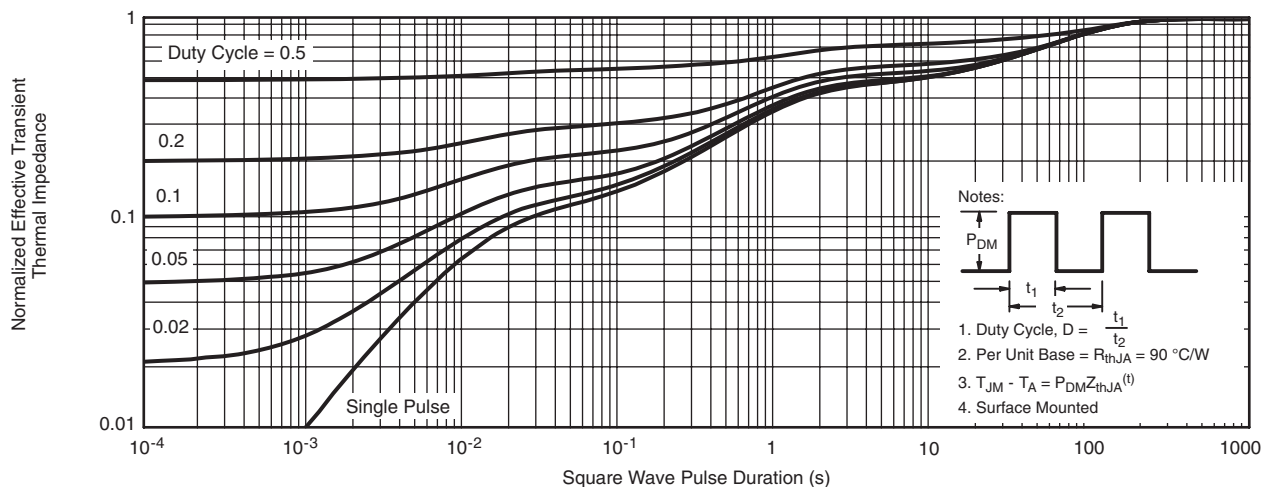
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



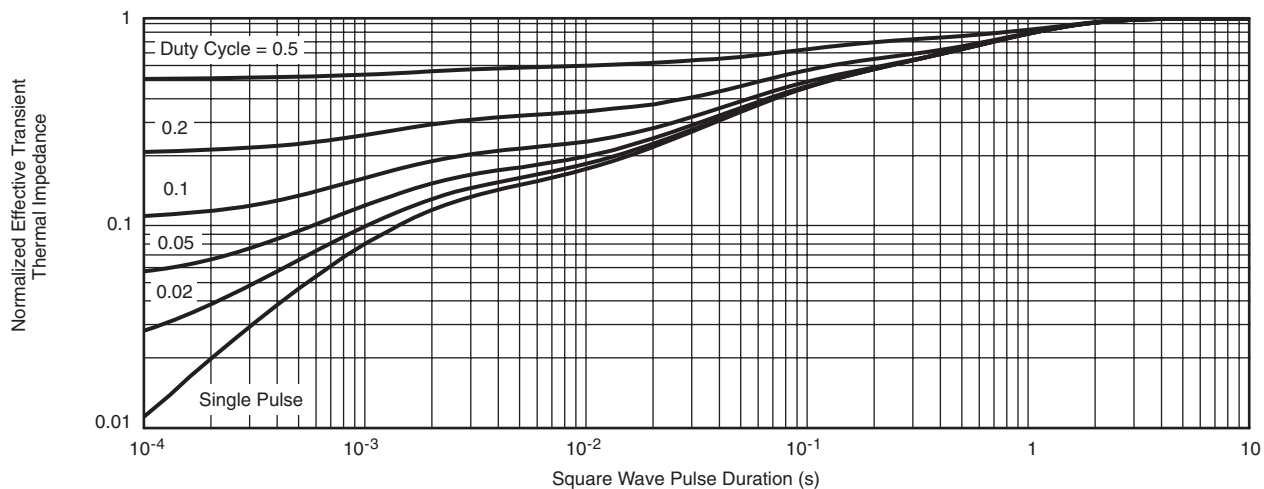
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?68791>.



Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.