TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

# SSM6P16FE

High Speed Switching Applications Analog Switch Applications

· Small package

Low on-resistance

 $: R_{on} = 8 \Omega \text{ (max) } (@V_{GS} = -4 \text{ V})$ 

:  $R_{on} = 12 \Omega \text{ (max) } (@V_{GS} = -2.5 \text{ V})$ 

 $: R_{on} = 45 \Omega \text{ (max) } (@V_{GS} = -1.5 \text{ V})$ 

# Absolute Maximum Ratings (Ta = 25°C) (Q1, Q2 Common)

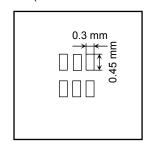
Characteristics		Symbol	Rating	Unit	
Drain-Source voltage		$V_{DS}$	-20	V	
Gate-Source voltage		$V_{GSS}$	±10	V	
Drain current	DC	ID	-100	mA	
	Pulse	I <sub>DP</sub>	-200		
Drain power dissipation (Ta = 25°C)		P <sub>D</sub> (Note 1)	150	mW	
Channel temperature		T <sub>ch</sub>	150	°C	
Storage temperature range		T <sub>stg</sub>	-55~150	°C	

Note:

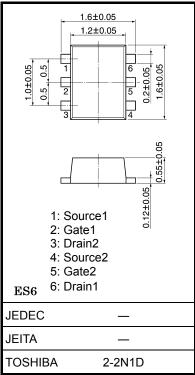
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

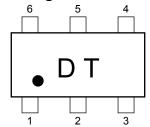
Note 1: Total rating, mounted on FR4 board (25.4 mm  $\times$  25.4 mm  $\times$  1.6 t, Cu Pad: 0.135 mm $^2 \times$  6)



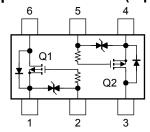
# Unit: mm



## Marking



# **Equivalent Circuit (top view)**



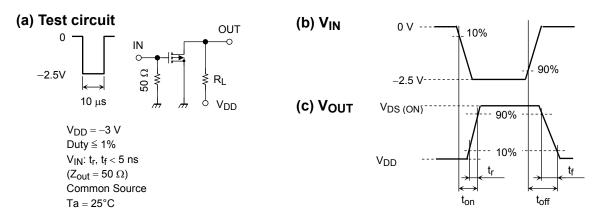
#### **Handling Precaution**

When handling individual devices (which are not yet mounted on a circuit board), ensure that the environment is protected against static electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

# Electrical Characteristics (Ta = 25°C) (Q1, Q2 common)

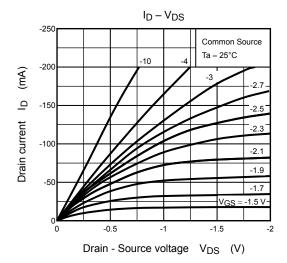
Characteristic		Symbol	Test Condition	MIN.	TYP.	MAX.	UNIT	
Gate leakage current		I <sub>GSS</sub>	$V_{GS} = \pm 10 \text{ V}, V_{DS} = 0$	_	_	±1	μА	
Drain-Source breakdown voltage		V (BR) DSS	$I_D = -0.1 \text{ mA}, V_{GS} = 0$	-20	_	_	V	
Drain cut-off current		I <sub>DSS</sub>	$V_{DS} = -20 \text{ V}, V_{GS} = 0$	_	_	-1	μА	
Gate threshold voltage		V <sub>th</sub>	$V_{DS} = -3 \text{ V}, I_D = -0.1 \text{ mA}$	-0.6	_	-1.1	V	
Forward transfer admittance		Y <sub>fs</sub>	$V_{DS} = -3 \text{ V}, I_D = -10 \text{ mA}$	25	_	_	mS	
Drain-Source on-resistance		R <sub>DS</sub> (ON)	$I_D = -10 \text{ mA}, V_{GS} = -4 \text{ V}$	_	6	8	Ω	
			$I_D = -10 \text{ mA}, V_{GS} = -2.5 \text{ V}$	_	8	12		
			$I_D = -1 \text{ mA}, V_{GS} = -1.5 \text{ V}$	_	18	45		
Input capacitance		C <sub>iss</sub>		_	11	_	pF	
Reverse transfer capacitance		C <sub>rss</sub>	$V_{DS} = -3 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	_	3.7	_	pF	
Output capacitance		C <sub>oss</sub>		_	10	_	pF	
Switching time	Turn-on time	t <sub>on</sub>	$V_{DD} = -3 \text{ V}, I_D = -10 \text{ mA},$	_	130	_	ns	
	Turn-off time	t <sub>off</sub>	$V_{GS} = 0 \sim -2.5 \text{ V}$	_	190	_		

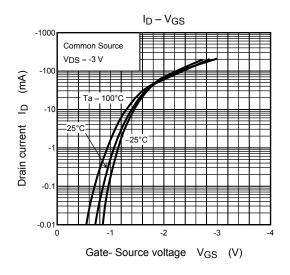
# **Switching Time Test Circuit**

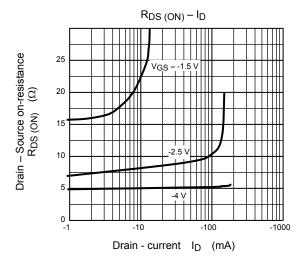


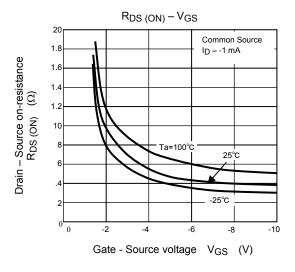
### **Precaution**

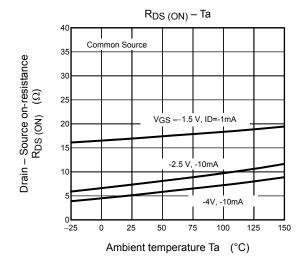
 $V_{th}$  can be expressed as the voltage between the gate and source when the low operating current value is ID =  $100~\mu A$  for this product. For normal switching operation,  $V_{GS}$  (on) requires a higher voltage than  $V_{th}$  and  $V_{GS}$  (off) requires a lower voltage than  $V_{th}$ . (The relationship can be established as follows:  $V_{GS}$  (off)  $< V_{th} < V_{GS}$  (on).) Be sure to take this into consideration when using the device.

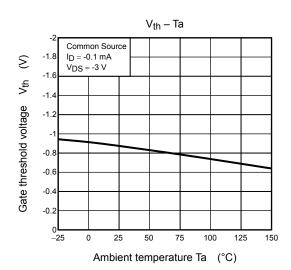


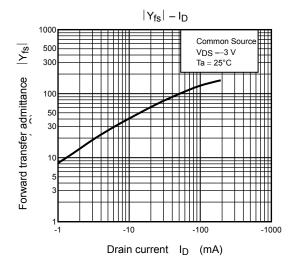


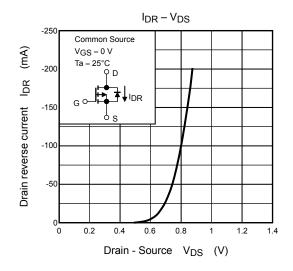


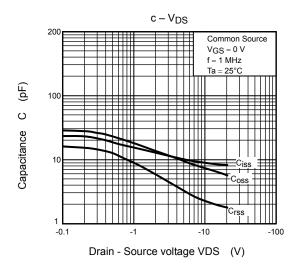


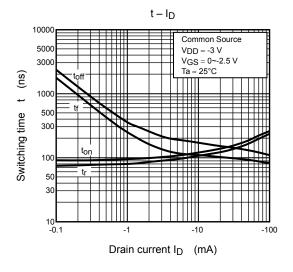


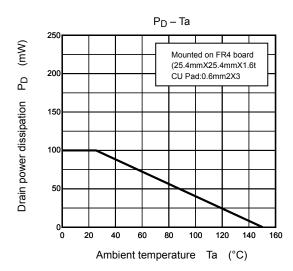












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