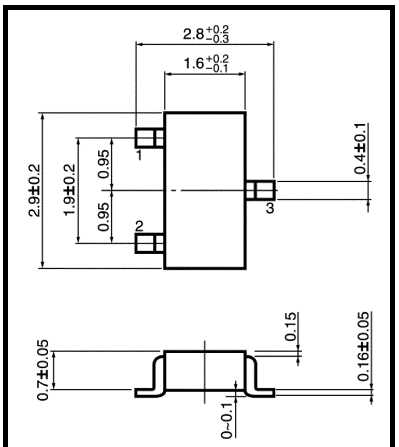
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM3K02T

High Speed Switching Applications

Unit: mm

- Small package
- Low on resistance: R_{on} = 200 mΩ (max) (V_{GS} = 4 V)
  : R_{on} = 250 mΩ (max) (V_{GS} = 2.5 V)
- Low gate threshold voltage: V_{th} = 0.6~1.1 V (V_{DS} = 3 V, I_D = 0.1 mA)



1. GATE
2. SOURCE
3. DRAIN

TSM

JEDEC	—
JEITA	—
TOSHIBA	2-3S1A

Weight: 0.01 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

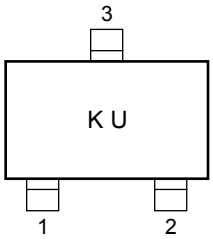
Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DS}	30	V
Gate-source voltage		V_{GSS}	±10	V
Drain current	DC	I_D	2.5	A
	Pulse	I_{DP}	5.0	
Drain power dissipation (Ta = 25°C)		P_D (Note 1)	1250	mW
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

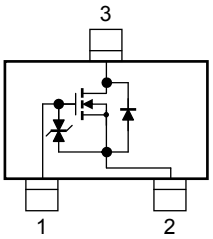
Note 1: Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 t, Cu pad: 645 mm^2, t = 10 s)

Note 2: The pulse width limited by max channel temperature.

Marking



Equivalent Circuit



Handling Precaution

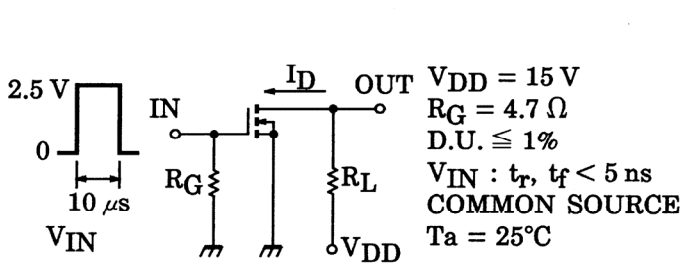
When handling individual devices (which are not yet mounted on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

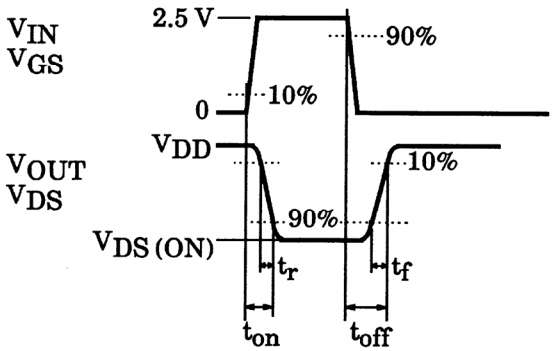
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	—	±5	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 1 mA, V_{GS} = 0	30	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = 30 V, V_{GS} = 0	—	—	1	μA
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 0.1 mA	0.6	—	1.1	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 1.25 A (Note)	2.2	—	—	S
Drain-source ON resistance		$R_{DS\ (ON)}$	I_D = 1.25 A, V_{GS} = 4 V (Note)	—	140	200	mΩ
			I_D = 1.25 A, V_{GS} = 2.5 V (Note)	—	180	250	
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	—	115	—	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	—	24	—	pF
Output capacitance		C_{oss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	—	60	—	pF
Switching time	Turn-on time	t_{on}	V_{DD} = 15 V, I_D = 0.5 A, V_{GS} = 0~2.5 V, R_G = 4.7 Ω	—	52	—	ns
	Turn-off time	t_{off}		—	80	—	

Note: Pulse test

Switching Time Test Circuit





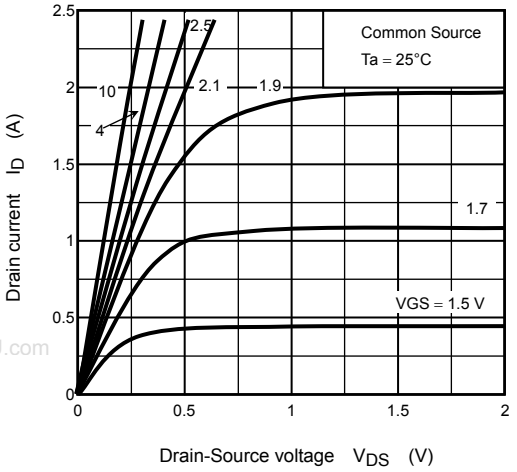
Precaution

V_{th} can be expressed as voltage between gate and source when low operating current value is I_D = 100 μA for this product. For normal switching operation, $V_{GS\ (ON)}$ requires higher voltage than V_{th} and $V_{GS\ (off)}$ requires lower voltage than V_{th}.

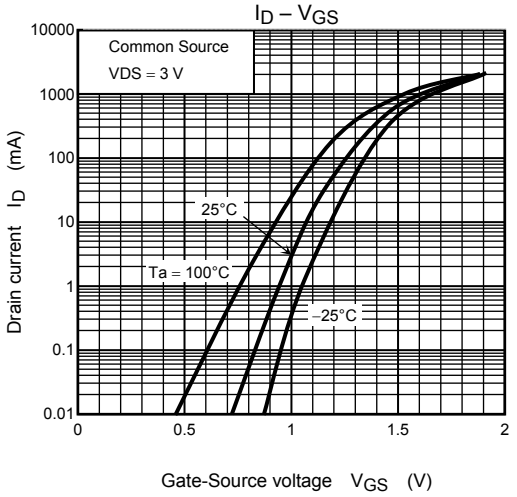
(Relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (ON)}$)

Please take this into consideration for using the device.

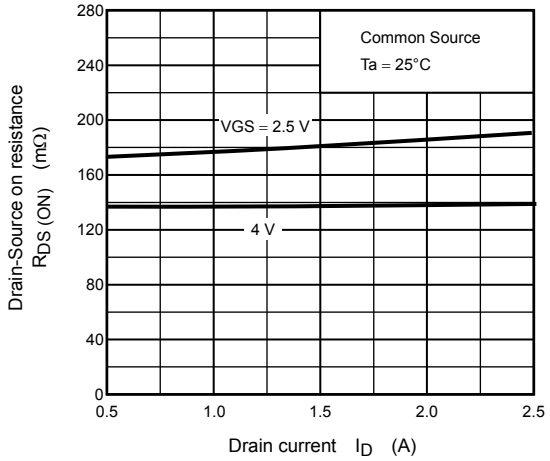
$I_D - V_{DS}$



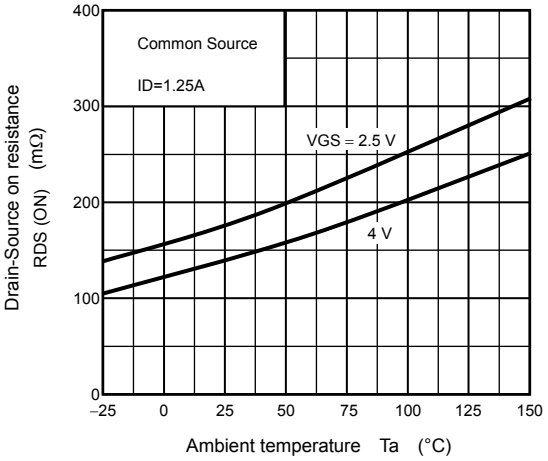
$I_D - V_{GS}$



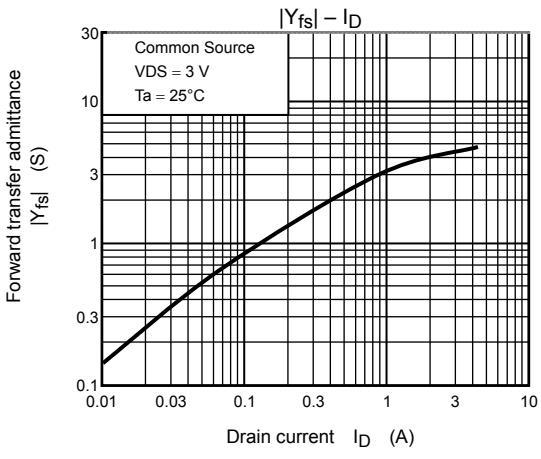
$R_{DS\ (ON)} - I_D$



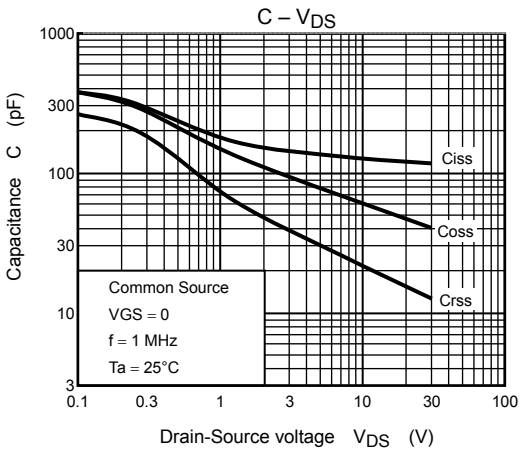
$R_{DS\ (ON)} - Ta$



$|Y_{fs}| - I_D$



$C - V_{DS}$



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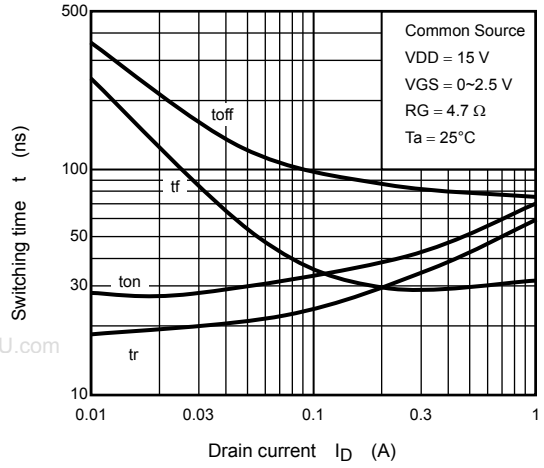
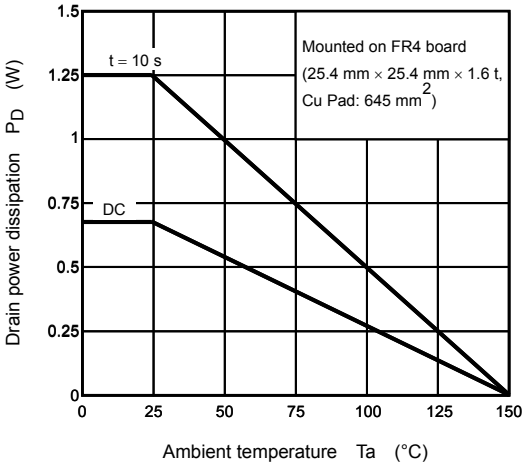
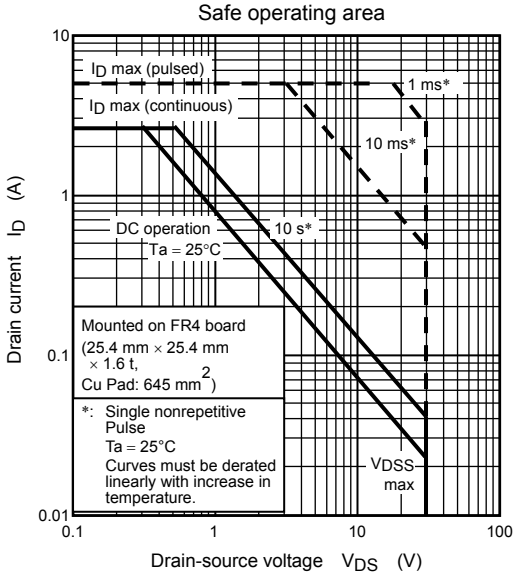
$t - I_D$



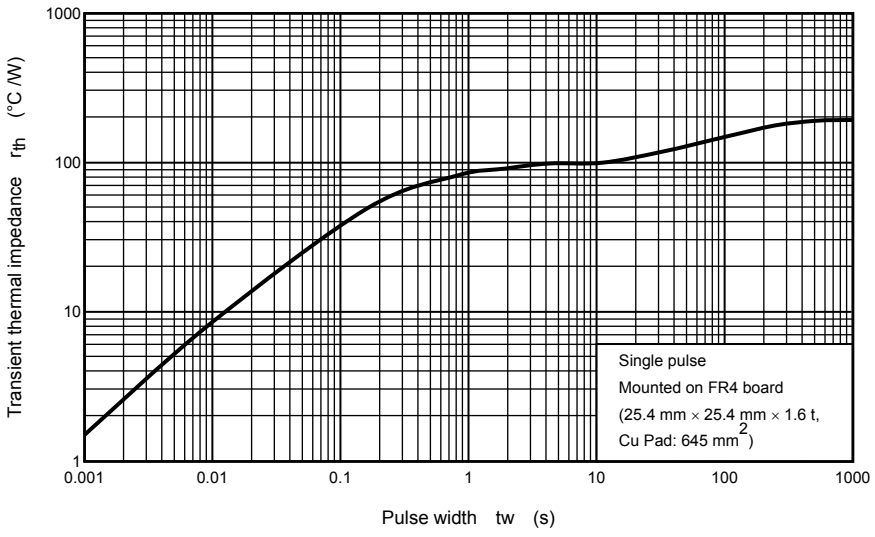
$P_D - Ta$



Safe operating area



$r_{th} - tw$



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20070701-EN GENERAL

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