



# STS1HNC60

N-CHANNEL 600V - 7Ω - 0.4A SO-8

PowerMesh™II MOSFET

PRELIMINARY DATA

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STS1HNC60	600 V	< 8 Ω	0.36 A

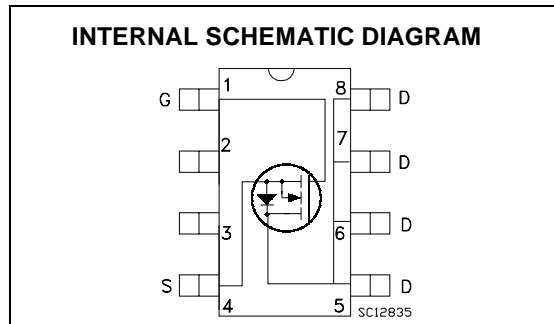
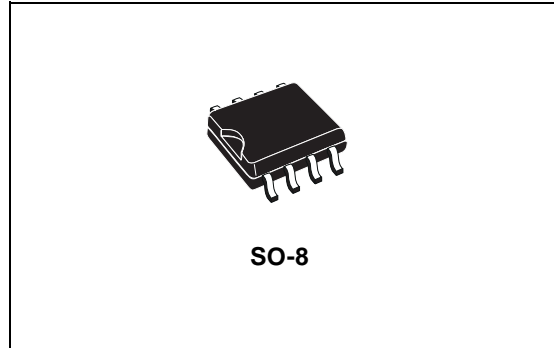
- TYPICAL R<sub>DS(on)</sub> = 7 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- NEW HIGH VOLTAGE BENCHMARK
- GATE CHARGE MINIMIZED

## DESCRIPTION

Using the latest high voltage MESH OVERLAY™II process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest R<sub>DS(on)</sub> per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

## APPLICATIONS

- SWITCH MODE LOW POWER SUPPLIES (SMPS)
- CFL



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	600	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	600	V
V <sub>GS</sub>	Gate- source Voltage	± 30	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	0.36	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	0.22	A
I <sub>DM</sub> (●)	Drain Current (pulsed)	1.44	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	2.5	W
	Derating Factor	0.028	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	3.5	V/ns
T <sub>stg</sub>	Storage Temperature	-65 to 150	°C
T <sub>j</sub>	Max. Operating Junction Temperature	150	°C

(●)Pulse width limited by safe operating area

(1)<sub>ISD</sub> ≤ 0.36 A, di/dt ≤ 100A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>.

## STS1HNC60

### THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	35.7	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max (Surface Mounted)	60	°C/W
T <sub>l</sub>	Maximum Lead Temperature For Soldering Purpose	300	°C

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	0.4	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	100	mJ

### ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	600			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			1 50	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2	3	4	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 0.3 A		7	8	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> , I <sub>D</sub> = 0.3 A		1.25		S
C <sub>iSS</sub>	Input Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		160		pF
C <sub>oSS</sub>	Output Capacitance			26		pF
C <sub>rSS</sub>	Reverse Transfer Capacitance			3.8		pF

**ELECTRICAL CHARACTERISTICS (CONTINUED)**

**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 300V, I_D = 0.7 A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		8		ns
$t_r$	Rise Time			8		ns
$Q_g$	Total Gate Charge	$V_{DD} = 480V, I_D = 1.4 A,$ $V_{GS} = 10V, R_G = 4.7\Omega$		8.5	11.5	nC
$Q_{gs}$	Gate-Source Charge			2.8		nC
$Q_{gd}$	Gate-Drain Charge			2.8		nC

**SWITCHING OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 480 V, I_D = 1.4 A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 5)		25		ns
$t_f$	Fall Time			9		ns
$t_c$	Cross-over Time			34		ns

**SOURCE DRAIN DIODE**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				0.4	A
$I_{SDM} (2)$	Source-drain Current (pulsed)				1.6	A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 0.4 A, V_{GS} = 0$			1.6	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 1.4 A, di/dt = 100A/\mu s,$ $V_{DD} = 100V, T_j = 150^\circ C$ (see test circuit, Figure 5)		500		ns
$Q_{rr}$	Reverse Recovery Charge			950		$\mu C$
$I_{RRM}$	Reverse Recovery Current			3.8		A

Note: 1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.  
2. Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

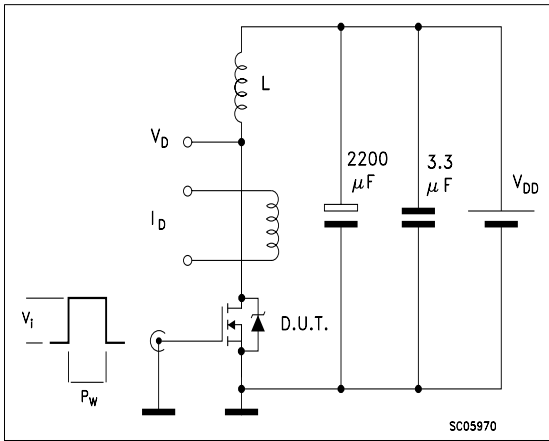


Fig. 2: Unclamped Inductive Waveform

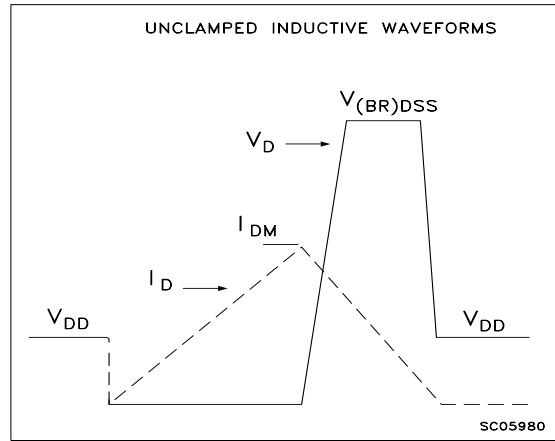


Fig. 3: Switching Times Test Circuit For Resistive Load

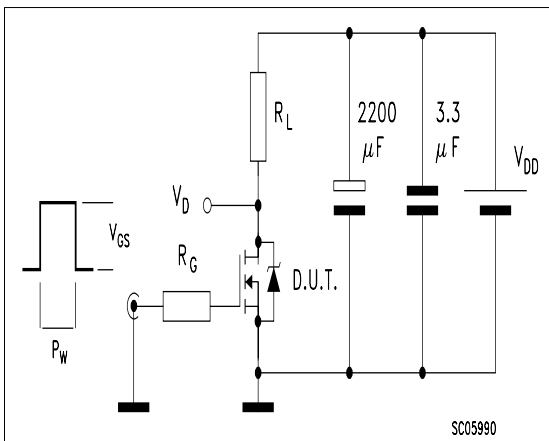


Fig. 4: Gate Charge test Circuit

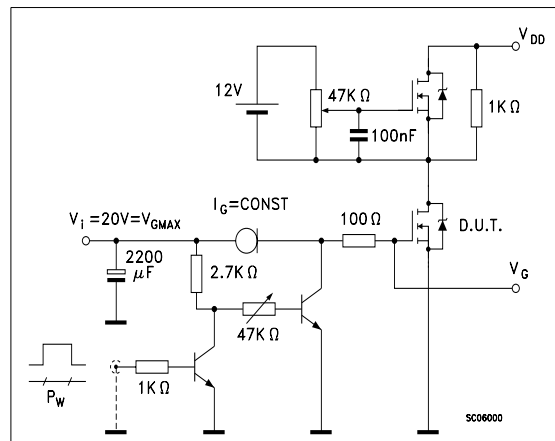
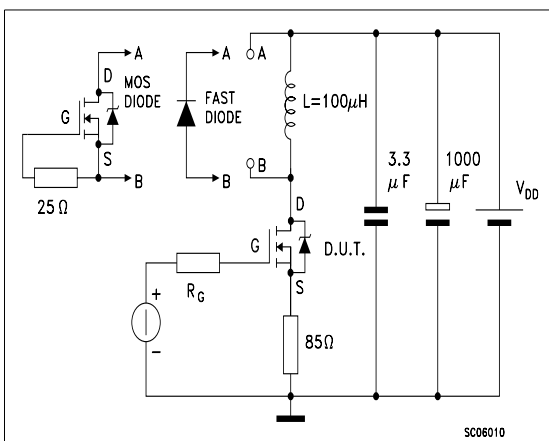
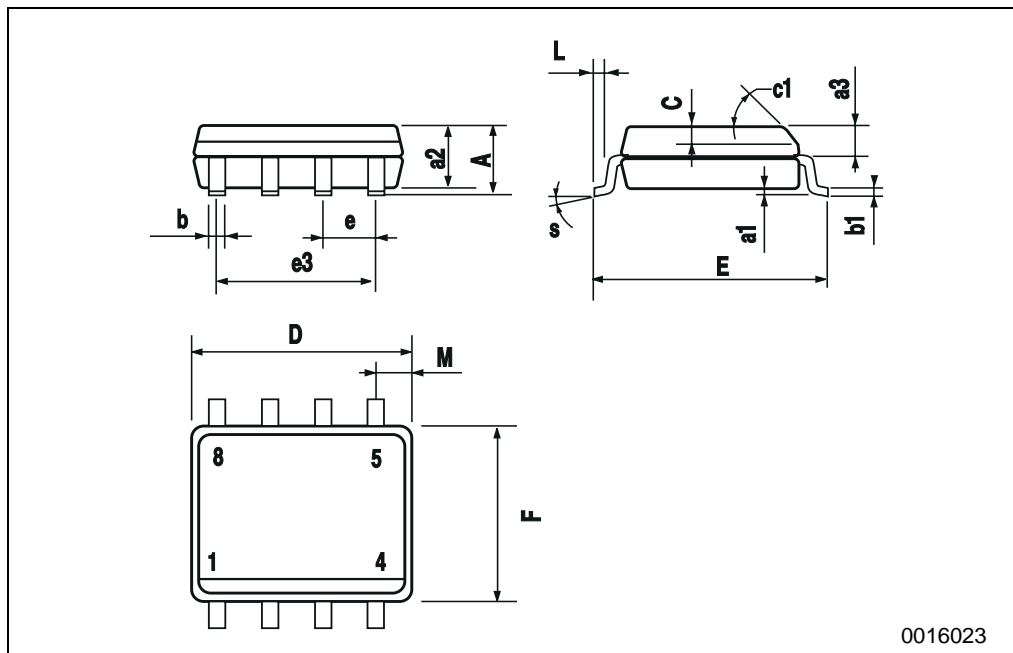


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



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