TSH110-111-112-113-114

WIDE BAND, LOW NOISE OPERATIONAL AMPLIFIERS

- **LOW NOISE: 3nV/√Hz**
- **LOW SUPPLY CURRENT: 3.2mA**
- **47mA OUTPUT CURRENT**
- **BANDWIDTH: 100MHz**
- **5V to 12V SUPPLY VOLTAGE**
- **SLEW-RATE: 450V/µs**
- **SPECIFIED FOR 100Ω Load**
- **VERY LOW DISTORTION**
- **TINY: SOT23-5, TSSOP and SO PACKAGES**

DESCRIPTION

The singles TSH110 and TSH111, the dual TSH112, the triple TSH113 and the quad TSH114 are current feedback operational amplifiers featuring a very high slew rate of 450V/µs and a large bandwidth of 100MHz, with only a 3.2mA quiescent supply current. The TSH111 and TSH113 feature a Standby function for each operator. This function is a power down mode with a high output impedance.

These devices operate from ±2.5V to ±6V dual supply voltage or from 5V to 12V single supply voltage. They are able to drive a 100Ω load with a swing of 9V minimum (for a 12V power supply).

The harmonic and intermodulation distortions of these devices are very low, making this circuit a good choice for applications requiring wide bandwidth with multiple carriers.

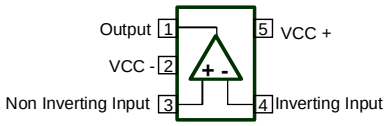
For board space and weight saving, the TSH110 comes in miniature SOT23-5 package, the TSH111 comes in SO8 and TSSOP8 packages, the TSH112 comes in SO8 and TSSOP8 packages, the TSH113 and TSH114 comes in SO14 and TSSOP14 packages.

APPLICATIONS

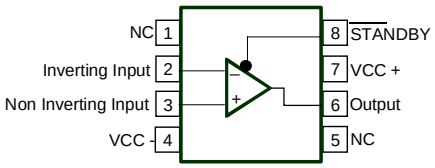
- High End Video Drivers
- Receiver for xDSL
- A/D Converter Driver
- High End Audio Applications

PIN CONNECTIONS (top view)

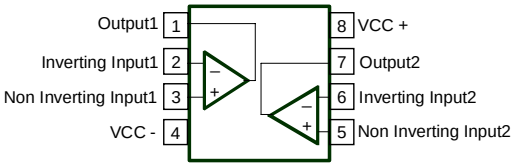
TSH110 : SOT23-5



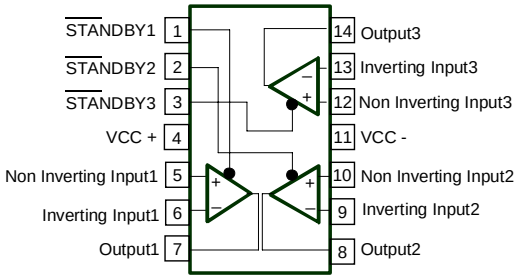
TSH111 : SO8/TSSOP8



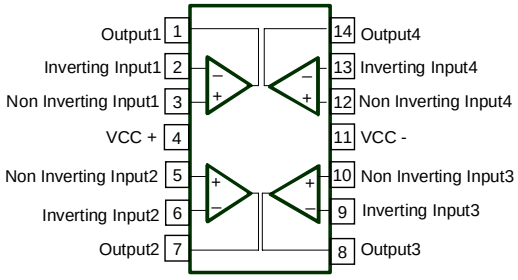
TSH112 : SO8/TSSOP8



TSH113 : SO14/TSSOP14



TSH114 : SO14/TSSOP14



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage [1]	14	V
V_{id}	Differential Input Voltage [2]	±1	V
V_i	Input Voltage [3]	±6	V
T_{oper}	Operating Free Air Temperature Range	-40 to +85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thjc}	Thermal resistance junction to case		°C/W
	SOT23-5	80	
	SO8	28	
	SO14	22	
	TSSOP8	37	
	TSSOP14	32	
R_{thja}	Thermal resistance junction to ambiante area		°C/W
	SOT23-5	250	
	SO8	157	
	SO14	125	
	TSSOP8	130	
	TSSOP14	110	
ESD	Human Body Model	2.0	kV
	Machine Model	0.2	
	Charged Device Model	1.5	
	ouput short circuit duration [4]		

1. All voltages values, except differential voltage are with respect to network ground terminal
2. Differential voltages are non-inverting input terminal with respect to the inverting terminal
3. The magnitude of input and output must never exceed V_{CC} +0.3V
4. Short-circuits can cause excessive heating. Destructive dissipation can result.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	5 to 12	V
Vicm	Common Mode Input Voltage Range	V_{CC-}+1.5 to V_{CC+}-1.5	V

ORDER CODES

Type	Temperature	Package
TSH110ILT (code K302)	-40° to +85°C	SOT23-5
TSH111ID		SO8
TSH111IDT		SO8
TSH111IPT		TSSOP8
TSH112ID		SO8
TSH112IDT		SO8
TSH112IPT		TSSOP8
TSH113ID		SO14
TSH113IDT		SO14
TSH113IPT		TSSOP14
TSH114ID		SO14
TSH114IDT		SO14
TSH114IPT		TSSOP14

D = Small Outline Package (SO) - also available in Tape & Reel (DT)
P = Thin Shrink Small Outline Package (TSSOP) - only available in Tape & Reel (PT)
L = Tiny Package (SOT23-5) - only available in Tape & Reel (LT)

ELECTRICAL CHARACTERISTICS (pages 3 and 4)

Dual Supply Voltage, V_{CC}= ±2.5Volts, R^*_{fb} = 680Ω, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DC PERFORMANCE						
V_{io}	Input Offset Voltage	T_{amb}	-1.5	0.3	2.0	mV
		$T_{min.} < T_{amb} < T_{max.}$		1		mV
ΔV_{io}	Input Offset Voltage Drift vs. Temperature	$T_{min.} < T_{amb} < T_{max.}$		5		µV/°C
I_{ib+}	Non Inverting Input Bias Current	T_{amb}	-10	1.4	13	µA
		$T_{min.} < T_{amb} < T_{max.}$		2.5		µA
I_{ib-}	Inverting Input Bias Current	T_{amb}	-3	1.9	7	µA
		$T_{min.} < T_{amb} < T_{max.}$		2.5		µA
R_{OL}	Transimpedance	R_L=100Ω	500	750		kΩ
I_{CC}	Supply Current per Operator	T_{amb}		3.2	4	mA
		$T_{min.} < T_{amb} < T_{max.}$		3.5		mA
CMR	Common Mode Rejection Ratio (ΔVic/ΔVio)		56	60		dB
SVR	Supply Voltage Rejection Ratio (ΔVCC/ΔVio)		70	80		dB
PSR	Power Supply Rejection Ratio (ΔVCC/ΔVout)	Gain=1, Rload=3.9kΩ		48		dB
DYNAMIC PERFORMANCE and OUTPUT CHARACTERISTICS						
V_{oh}	High Level Output Voltage	T_{amb} R_L = 100Ω	1.4	2		V
		$T_{min.} < T_{amb} < T_{max.}$ R_L = 100Ω GND		1.9		V
V_{ol}	Low Level Output Voltage	T_{amb} R_L = 100Ω		-1.8	-1.3	V
		$T_{min.} < T_{amb} < T_{max.}$ R_L = 100Ω		-1.7		V
$\mid I_{sink} \mid$	Output Sink current	$T_{min.} < T_{amb} < T_{max.}$		20		mA
I_{source}	Output Source current	$T_{min.} < T_{amb} < T_{max.}$		18		mA
BW	-3dB Bandwidth	Vout=1Vpk, Rfb*=820Ω//2pF Load=100Ω				
		A_{VCL}=+2		81		MHz
SR	Slew Rate	A_{VCL}=+2, 2V step Load=100Ω	160	230		V/µs
Tr	Rise Time	for 200mV step A_{VCL}=+2, Rfb*=820Ω//2pF Load=100Ω		9		ns
Tf	Fall Time			9		ns
Ov	Overshoot			16		%
St	Settling Time @ 0.05%			60		ns
ΔG	Differential gain	A_{VCL}=+2, R_L=100Ω F=4.5MHz, V_{out}=1Vpeak		0.05		%
Δϕ	Differential phase			0.05		°

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
NOISE AND HARMONIC PERFORMANCE						
en	Equivalent Input Voltage Noise	Frequency : 1MHz		3		nV/√Hz
in	Equivalent Input Current Noise			8.5		pA/√Hz
THD	Total Harmonic Distortion	A_{VCL}=+2, F=2MHz R_L=100Ω V_{out}=2Vpeak		64.4		dB
IM3	Third order inter modulation product	A_{VCL}=+2, V_{out}=2Vpp R_L=100Ω F1=1MHz, F2=1.1MHz				dBc
		@900kHz		90		
		@1.2MHz		90		
		@3.1MHz		86		
		@3.2MHz		83		
MATCHING CHARACTERISTICS						
Gf	Gain Flatness	F=(DC) to 6MHz A_{VCL}=+2, V_{out}=2Vpp		0.1		dB
Vo1/Vo2	Channel Separation	F=1MHz to 10MHz		65		dB

(*) R_{fb} is the feedback resistance between the output and the inverting input of the amplifier.

ELECTRICAL CHARACTERISTICS (pages 5 and 6)

Dual Supply Voltage, V_{CC}=±6Volts, R^*_{fb} = 680Ω, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	TestCondition	Min.	Typ.	Max.	Unit
DC PERFORMANCE						
V_{io}	Input Offset Voltage	T_{amb}	-1.0	0.9	3.0	mV
		$T_{min.} < T_{amb} < T_{max.}$		1.3		mV
ΔV_{io}	Input Offset Voltage Drift vs Temperature	$T_{min.} < T_{amb} < T_{max.}$		5		µV/°C
I_{ib+}	Non Inverting Input Bias Current	T_{amb}	-12	1	14	µA
		$T_{min.} < T_{amb} < T_{max.}$		1.7		µA
I_{ib-}	Inverting Input Bias Current	T_{amb}	-4	3	10	µA
		$T_{min.} < T_{amb} < T_{max.}$		3.4		µA
R_{OL}	Transimpedance	R_L=100Ω	600	900		kΩ
I_{CC}	Supply Current per Operator	T_{amb}		4	5	mA
		$T_{min.} < T_{amb} < T_{max.}$		4.1		mA
CMR	Common Mode Rejection Ratio (ΔVic/ΔVio)		58	63		dB
SVR	Supply Voltage Rejection Ratio (ΔVcc/ΔVio)		72	80		dB
PSR	Power Supply Rejection Ratio (ΔVcc/ΔVout)	Gain=1, Rload=3.9kΩ		49		dB
DYNAMIC PERFORMANCE and OUTPUT CHARACTERISTICS						
V_{oh}	High Level Output Voltage	T_{amb} R_L = 100Ω	4.5	4.7		V
		$T_{min.} < T_{amb} < T_{max.}$ R_L = 100Ω		4.6		V
V_{ol}	Low Level Output Voltage	T_{amb} R_L = 100Ω		-4.7	-4.3	V
		$T_{min.} < T_{amb} < T_{max.}$ R_L = 100Ω		-4.6		V
$\lvert I_{sink} \rvert$	Output Sink current	$T_{min.} < T_{amb} < T_{max.}$		47		mA
I_{source}	Output Source current	$T_{min.} < T_{amb} < T_{max.}$		46		mA
Bw	-3dB Bandwidth	Vout=1Vpk, Rfb*=680Ω//2pF Load=100Ω				
		A_{VCL}=+2		100		MHz
SR	Slew Rate	A_{VCL}=+2, 6V step Load=100Ω	240	450		V/µs
Tr	Rise Time	for 200mV step A_{VCL}=+2, Rfb*=680Ω//2pF Load=100Ω		10.4		ns
Tf	Fall Time			12.2		ns
Ov	Overshoot			17		%
St	Settling Time @ 0.05%			40		ns
ΔG	Differential gain	A_{VCL}=+2, R_L=100Ω F=4.5MHz, V_{out}=2Vpeak		0.05		%
Δϕ	Differential phase			0.05		°

Symbol	Parameter	TestCondition	Min.	Typ.	Max.	Unit
NOISE AND HARMONIC PERFORMANCE						
en	Equivalent Input Voltage Noise	Frequency : 1MHz		3		nV/√Hz
in	Equivalent Input Current Noise			8.6		pA/√Hz
THD	Total Harmonic Distortion	A_{VCL}=+2, F=2MHz R_L=100Ω V_{out}=4Vpp		67.7		dB
IM3	Third order inter modulation product	A_{VCL}=+2, V_{out}=4Vpp R_L=100Ω F1=1MHz, F2=1.1MHz				dBc
		@900kHz		82		
		@1.2MHz		84		
		@3.1MHz		77		
		@3.2MHz		73		
MATCHING CHARACTERISTICS						
Gf	Gain Flatness	F=(DC) to 6MHz A_{VCL}=+2, V_{out}=4Vpp		0.1		dB
Vo1/Vo2	Channel Separation	F=1MHz to 10MHz		65		dB

(*) R_{fb} is the feedback resistance between the output and the inverting input of the amplifier.

STANDBY MODE

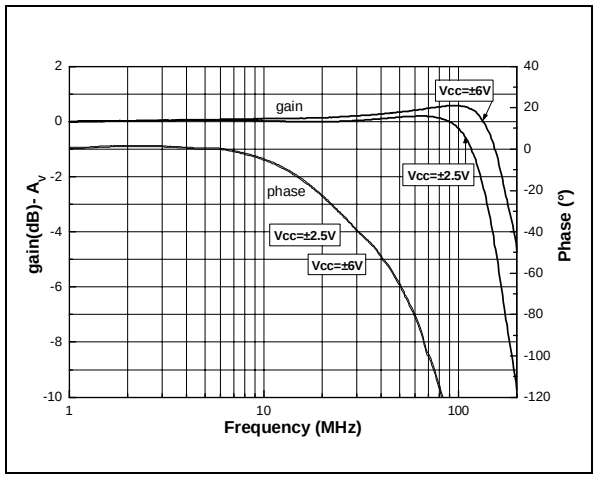
T_{amb} = 25°C (unless otherwise specified), V_{CC}=±6Volts

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Vl_{ow}	Standby Low Level		V_{CC}^-		(V_{CC}^- +0.8)	V
V_{high}	Standby High Level		(V_{CC}^- +2)		(V_{CC}^+)	V
$I_{CC\ SBY}$	Current Consumption per Operator in Standby mode			26	40	µA
I_{sol}	Input/Output Isolation	F=1MHz		-90		dB
Z_{out}	Output Impedance (Rout // Cout)	R_{out} C_{out}		31 25		MΩ pF
T_{on}	Time from Standby Mode to Active Mode			2		µs
T_{off}	Time from Active Mode to Standby Mode	Down to $I_{CC\ SBY}$ = 40µA		13		µs

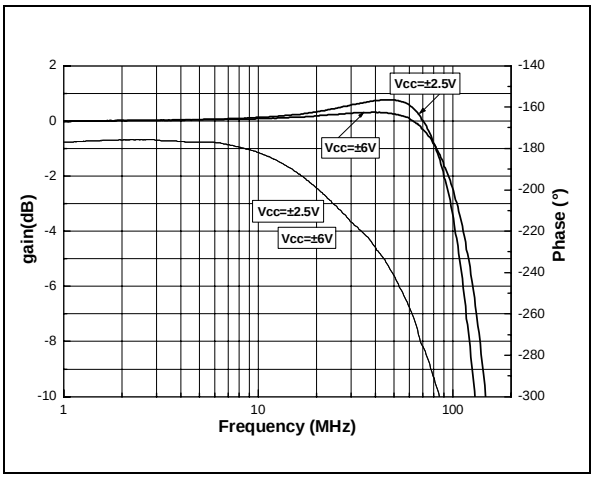
TSH111 STANDBY CONTROL pin 8 ($\overline{SBY}$)	OPERATOR STATUS
V_{low}	Standby
V_{high}	Active

TSH113 STANDBY CONTROL			OPERATOR STATUS		
pin 1 ($\overline{SBY}$ OP1)	pin 2 ($\overline{SBY}$ OP2)	pin 3 ($\overline{SBY}$ OP)	OP1	OP1	OP3
V_{low}	x	x	Standby	x	x
V_{high}	x	x	Active	x	x
x	V_{low}	x	x	Standby	x
x	V_{high}		x	Active	x
x	x	V_{low}	x	x	Standby
x	x	V_{high}	x	x	Active

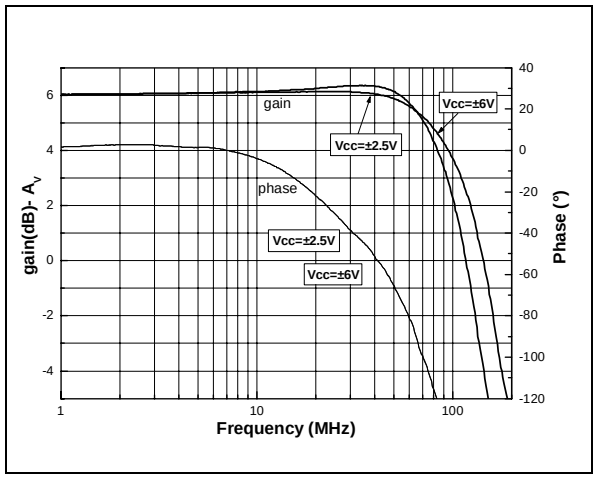
(fig.1) Closed Loop Gain vs. Frequency
A_V=+1, R_{fb}=2.2kΩ, C_{fb}=2pF, R_L=100Ω, V_{in}=100mVp



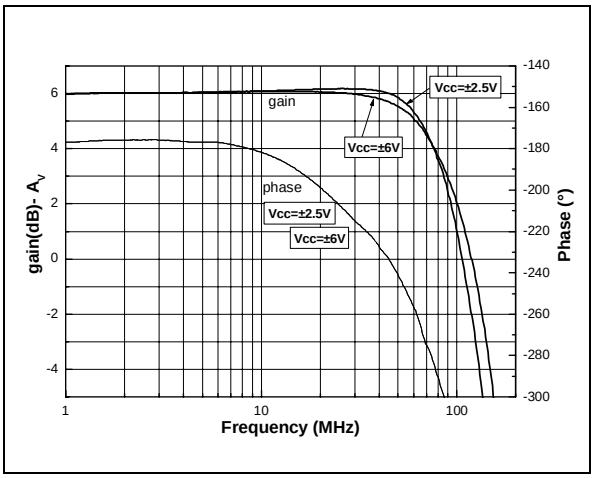
(fig.2) Closed Loop Gain vs. Frequency
A_V=-1, R_{fb}=2.2kΩ, C_{fb}=2pF, R_L=100Ω, V_{in}=100mVp



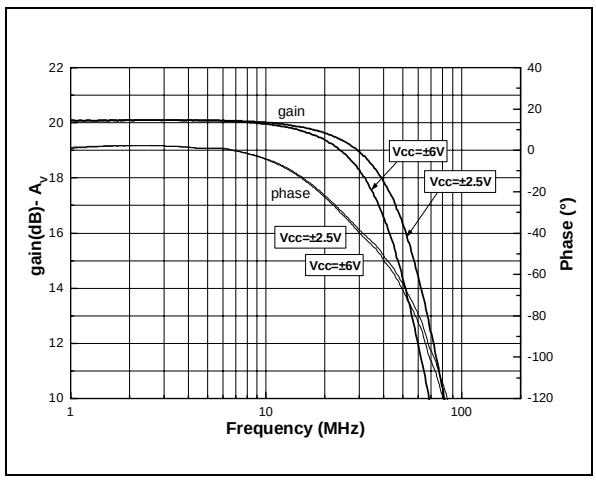
(fig.3) Closed Loop Gain vs. Frequency
A_V=+2, R_{fb}=680Ω, C_{fb}=2pF, R_L=100Ω, V_{in}=100mVp



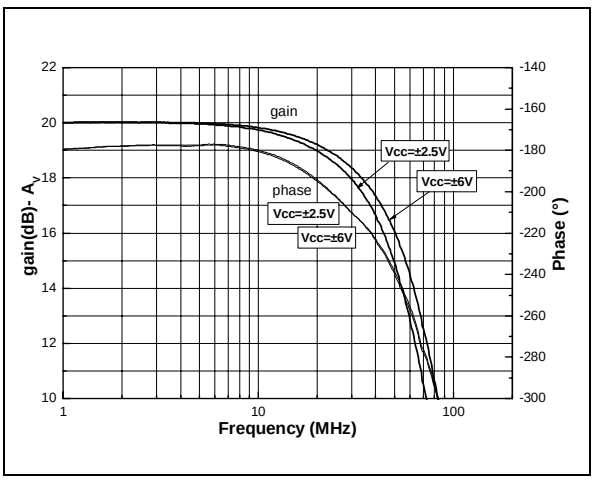
(fig.4) Closed Loop Gain vs. Frequency
A_V=-2, R_{fb}=680kΩ, C_{fb}=2pF, R_L=100Ω, V_{in}=100mVp



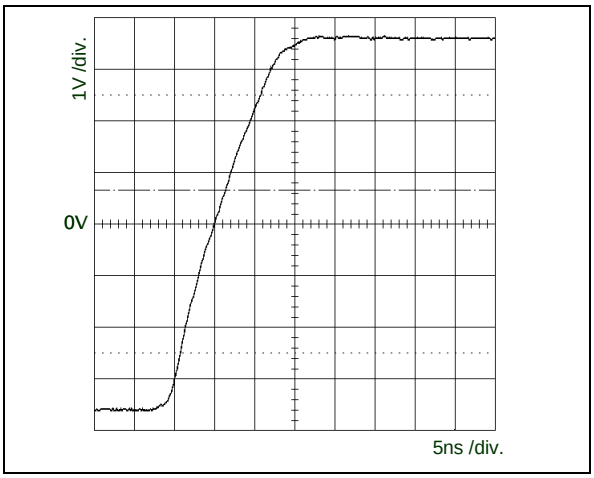
(fig.5) Closed Loop Gain vs. Frequency
A_V=+10, R_{fb}=510Ω, R_L=100Ω, V_{in}=30mVp



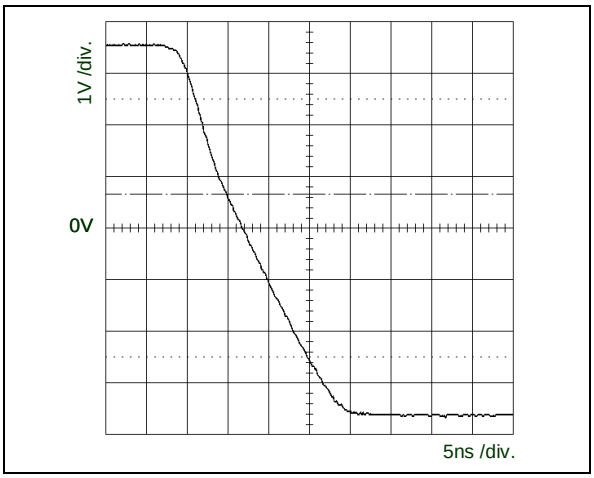
(fig.6) Closed Loop Gain vs. Frequency
A_V=-10, R_{fb}=510Ω, R_L=100Ω, V_{in}=30mVp



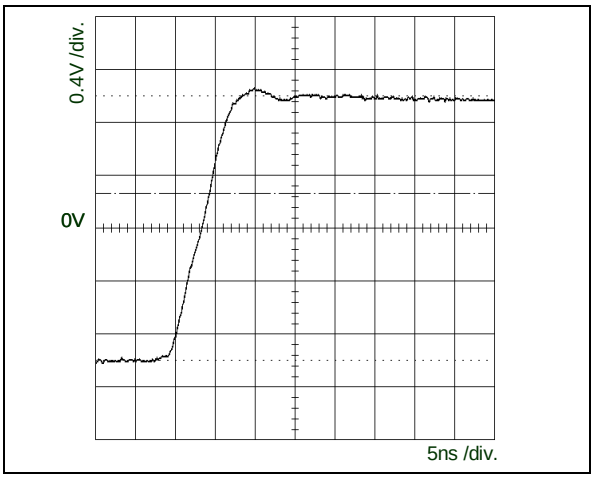
(fig.7): Positive Slew Rate
A_V=+2, R_{fb}=680Ω, C_{fb}=2pF, R_L=100Ω, Vcc=±6V



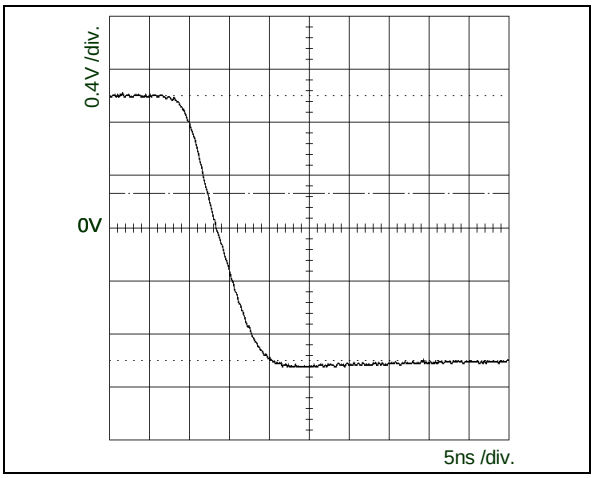
(fig.8): Negative Slew Rate
A_V=+2, R_{fb}=680Ω, C_{fb}=2pF, R_L=100Ω, Vcc=±6V



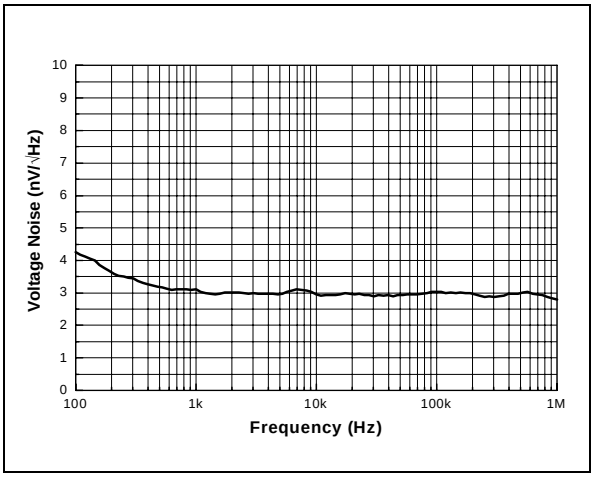
(fig.9): Positive Slew Rate
A_V=+2, R_{fb}=680Ω, C_{fb}=2pF, R_L=100Ω, Vcc=±2.5V



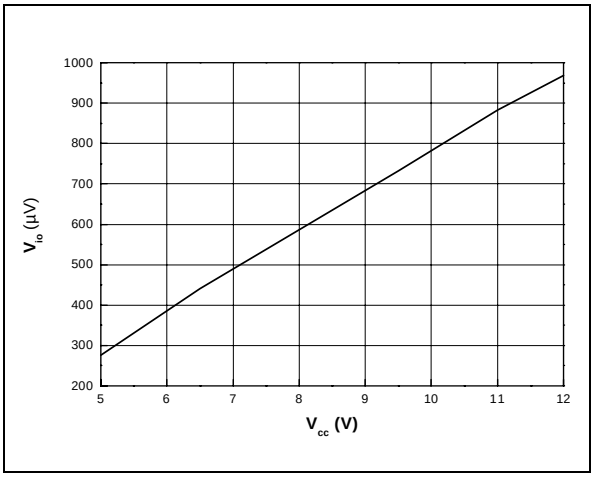
(fig.10): Negative Slew Rate
A_V=+2, R_{fb}=680Ω, C_{fb}=2pF, R_L=100Ω, Vcc=±2.5V



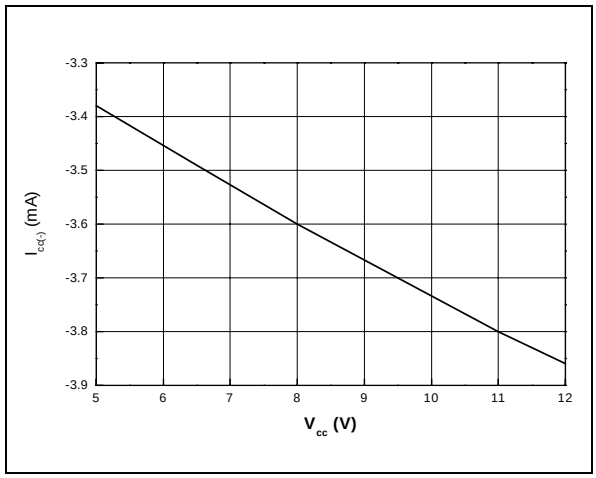
(fig.11): Input Voltage Noise Level
A_V=+100, R_{fb}=1kΩ, Input+ connected to Gnd via 10Ω



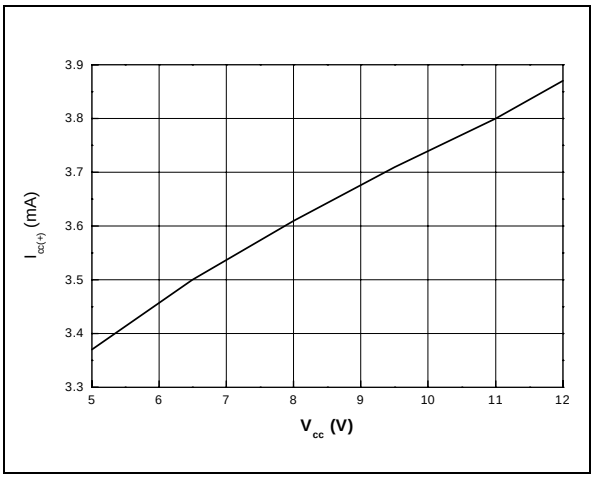
(fig.12): V_{io} vs. Power Supply
Open loop, no load



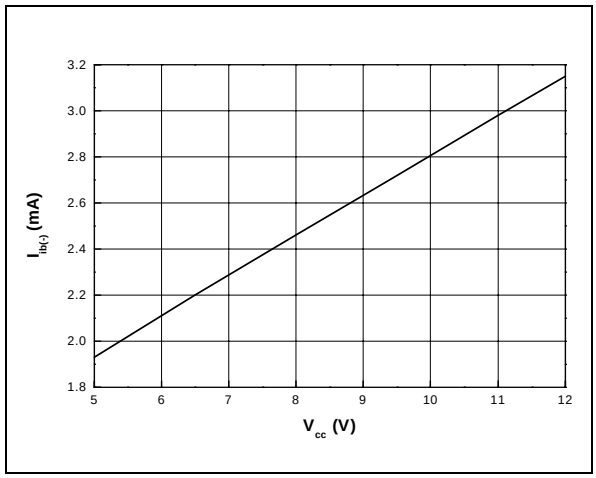
(fig.13): $I_{cc(-)}$ vs. Power Supply
Open loop, no load



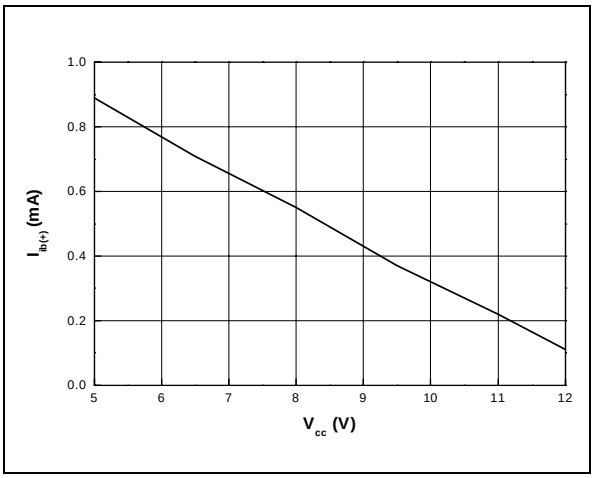
(fig.14): $I_{cc(+)}$ vs. Power Supply
Open loop, no load



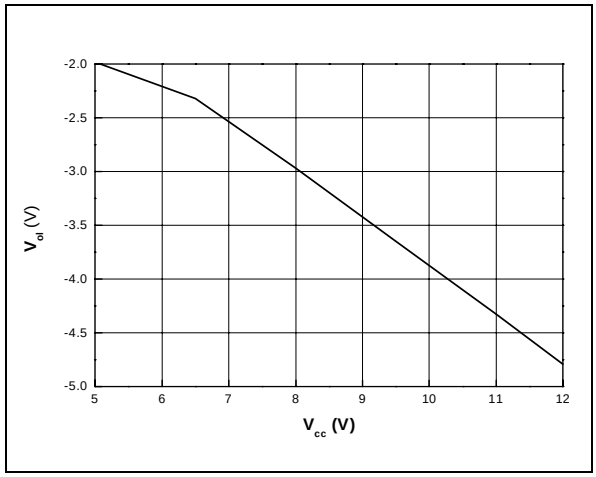
(fig.15): $I_{ib(-)}$ vs. Power Supply
Open loop, no load



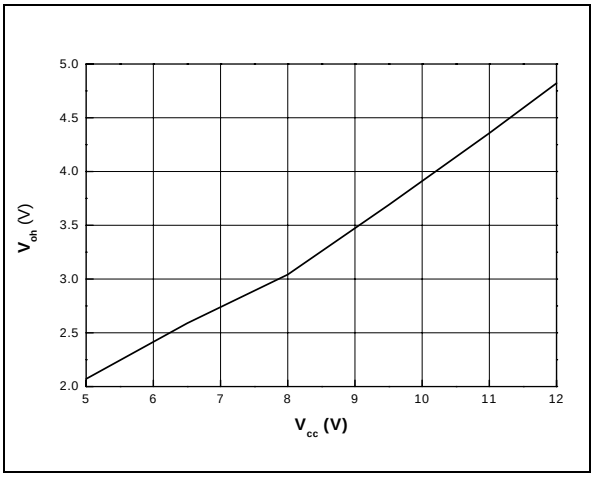
(fig.16): $I_{ib(+)}$ vs. Power Supply
Open loop, no load



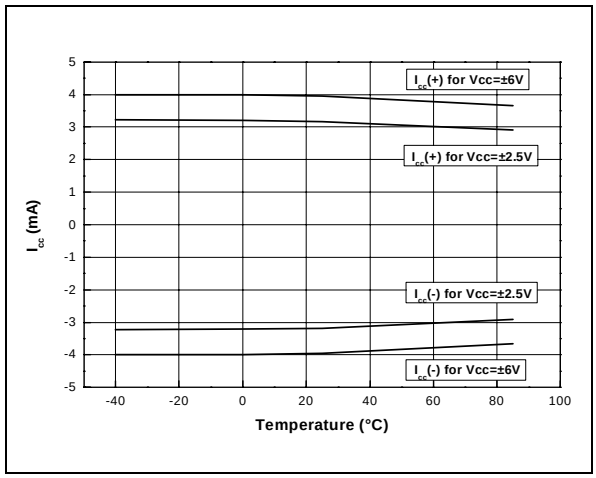
(fig.17): V_{ol} vs. Power Supply
Open loop, R_L=100Ω



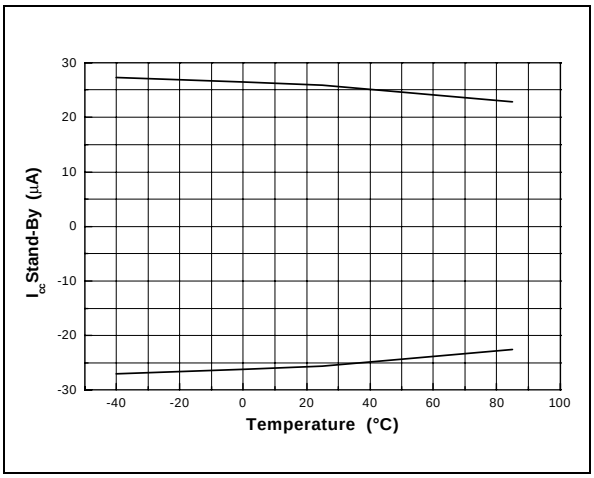
(fig.18): V_{oh} vs. Power Supply
Open loop, R_L=100Ω



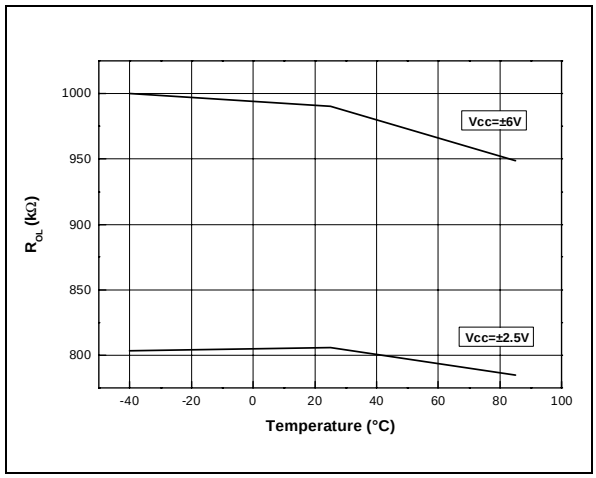
(fig.19): I_{CC} vs. Temperature
Open loop, no load



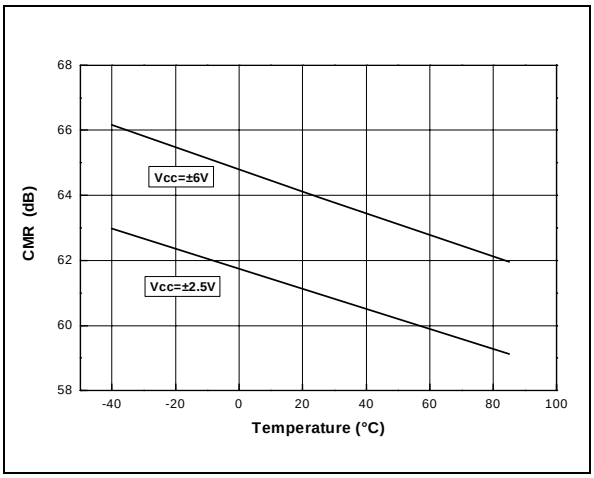
(fig.20): I_{CC} (Standby) vs. Temperaure
Open loop, no load



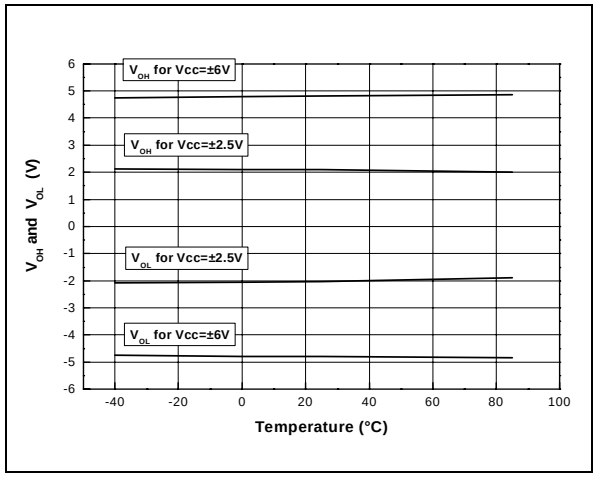
(fig.21): R_{OL} vs. Temperature
Open loop, no load



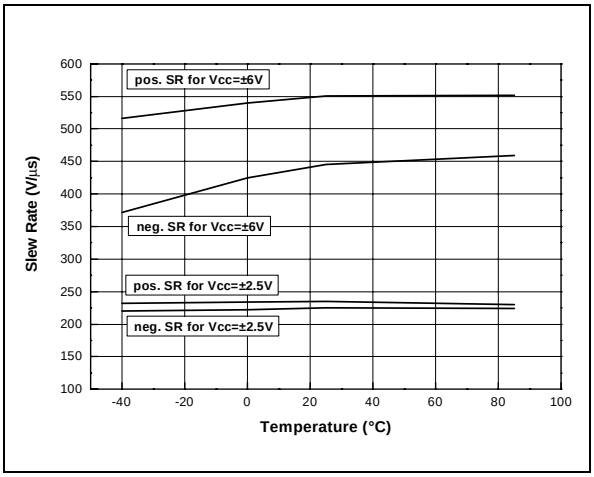
(fig.22): CMR vs. Temperature
Open loop, no load



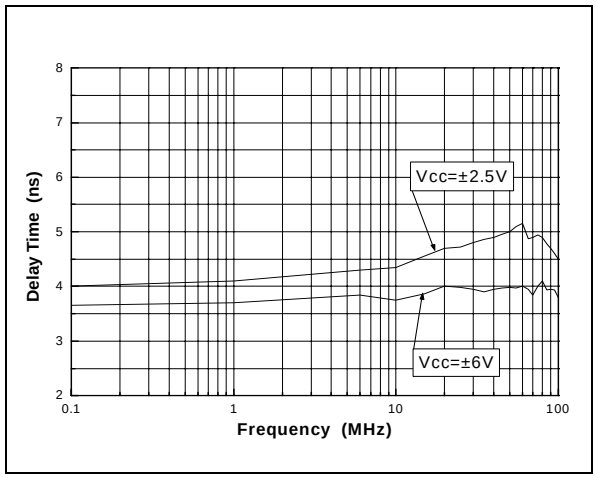
(fig.23): V_{OH} & V_{OL} vs. Temperature
Open loop, R_L=100Ω



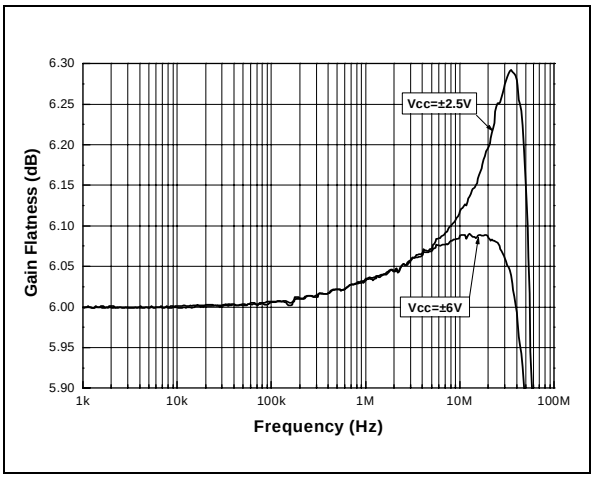
(fig.24): Slew Rate vs. Temperature
A_V=+2, R_L=100Ω



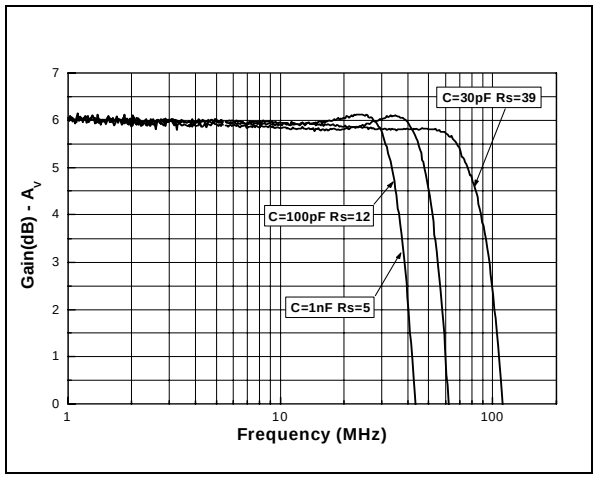
(fig.25): Group Delay
A_V=+2, R_{fb}=680Ω, C_{fb}=2pF, R_L=100Ω



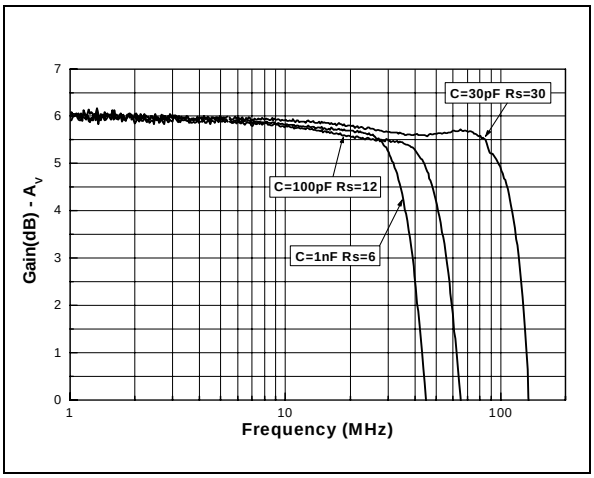
(fig.26): Gain Flatness
A_V=+2, R_{fb}=680Ω, C_{fb}=2pF, R_L=100Ω



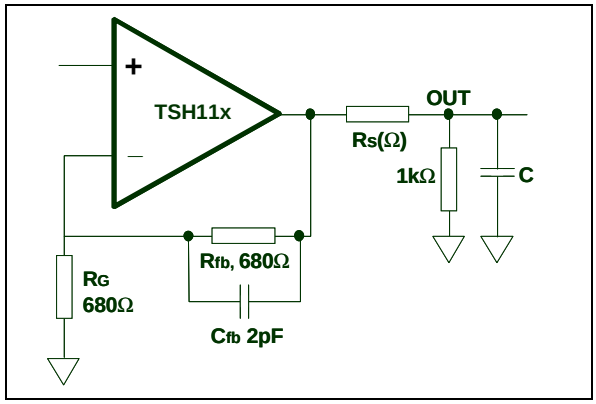
(fig.27): Frequency Response vs. Load
A_V=+2, R_{fb}=680Ω, C_{fb}=2pF, V_{CC}=±2.5V, (fig.29)



(fig.28): Frequency Response vs. Load
A_V=+2, R_{fb}=680Ω, C_{fb}=2pF, V_{CC}=±6V, (fig.29)



(fig.29): *Capacitive Load Schematic. measurements on (fig.27) and (fig.28)*



Intermodulation Distortion

A non-ideal output of the amplifier can be described by the following development :

$V_{out}=C_0+C_1(V_{in})+C_2(V_{in})^2+C_3(V_{in})^3+...+C_n(V_{in})^n$

due to a non-linearity in the input-output amplitude transfert. In the case of $V_{in}=A\sin\omega t$, C_O is the DC component, $C_1(V_{in})$ is the fundamental, C_nA^n is the amplitude of the harmonics.

A one-frequency or one-tone input signal contributes to a harmonic distortion. A two-tones input signal contributes to a harmonic distortion and intermodulation product.

This intermodulation product or intermodulation distortion of a two-tones input signal is the first step of the amplifier study for driving capability in the case of a multitone signal.

In this case $V_{in}=A\sin\omega_1 t+B\sin\omega_2 t$, and :

$V_{out}=$
$C_O+C_1(A\sin\omega_1 t+B\sin\omega_2 t)$
$+$
$C_2(A\sin\omega_1 t+B\sin\omega_2 t)^2+C_3(A\sin\omega_1 t+B\sin\omega_2 t)^3$
$+$
$...C_n(V_{in})^n$

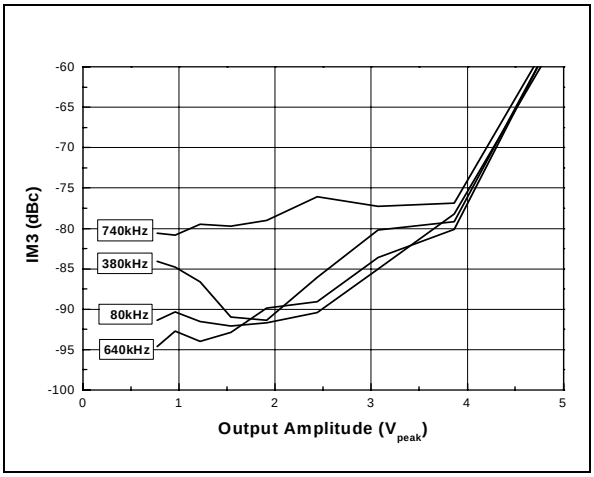
$V_{out}=$
$C_O+C_1(A\sin\omega_1 t+B\sin\omega_2 t)$
$+$
$C_2(A^2+B^2)/2-(C_2/2)(A^2\cos2\omega_1 t+B^2\cos2\omega_2 t)$
$+$
$2C_2AB(\cos(\omega_1-\omega_2)t-\cos(\omega_1+\omega_2)t)$
$+$
$(3C_3/4)$
$(A^3\sin\omega_1 t+B^3\sin\omega_2 t+2A^2B\sin\omega_2 t+2B^2A\sin\omega_1 t)$
$+$
$(C_3A^3\sin3\omega_1 t+B^3\sin3\omega_2 t)$
$+$
$(3C_3A^2B/2)(\sin(2\omega_1-\omega_2)t-1/2\sin(2\omega_1+\omega_2)t)$
$+$
$(3C_3B^2A/2)(\sin(-\omega_1+2\omega_2)t-1/2\sin(\omega_1+2\omega_2)t)$
$+$
$...C_n(V_{in})^n$

In this expression, we can recognize the second order intermodulation IM2 by the frequencies $(\omega_1-\omega_2)$ and $(\omega_1+\omega_2)$ and the third order intermodulation IM3 by the frequencies $(2\omega_1-\omega_2)$, $(2\omega_1+\omega_2)$, $(-\omega_1+2\omega_2)$ and $(\omega_1+2\omega_2)$.

The following graphs show the IM3 of the amplifier in two cases as a function of the output amplitude. The two-tones input signal is achieved by the multisource generator Marconi 2026. Each tone has the same amplitude. The measurement is achieved by the spectrum analyser HP 3585A. Both instruments are phase locked to enhance measurement precision.

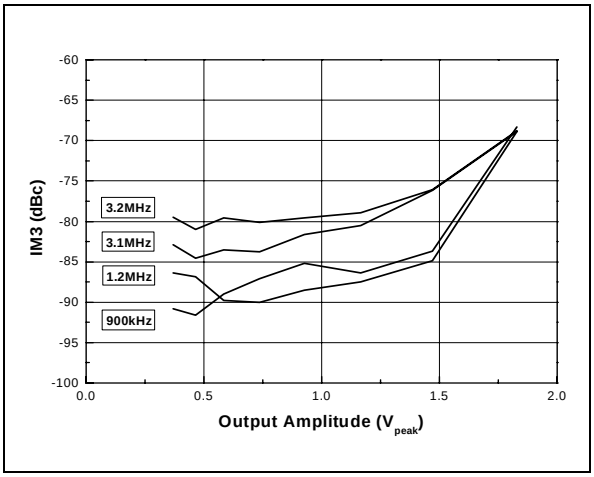
(fig.30): 3rd Order Intermodulation (180kHz & 280kHz)

$A_V=+4$, $R_{fb}=680\Omega$, no C_{fb}, $R_L=100\Omega$, Vcc=±6V



(fig.31): 3rd Order Intermodulation (1MHz & 1.1MHz)

$A_V=+2$, $R_{fb}=680\Omega$, $C_{fb}=2pF$, $R_L=100\Omega$, Vcc=±2.5V



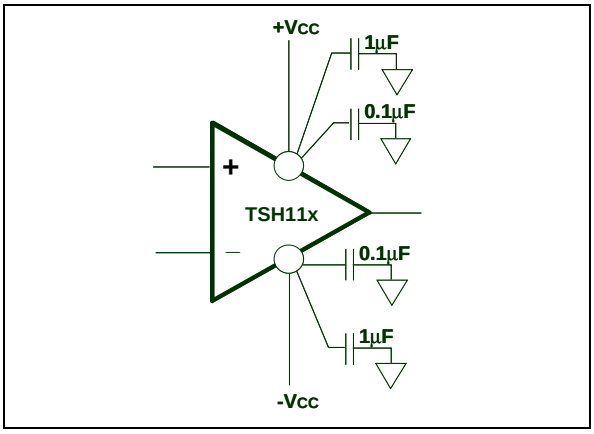
Printed Circuit Board Layout Considerations

In this range of frequency, printed circuit board parasitics can affect the closed-loop performance. The implementation of a proper ground plane in both sides of the PCB is mandatory to provide low inductance and low resistance common return. Most important for controlling the gain flatness and the bandwidth are stray capacitances at the output and inverting input. For minimizing the coupling, the space between signal lines and ground plane will be increased. Connections of the feedback components must be as short as possible on order to decrease the associated inductance which affect high frequency gain errors. It is very important to choose external components as small as possible such as surface mounted devices, SMD, in order to minimize the size of all the dc and ac connections.

Power Supply Bypassing

A proper power supply bypassing comes very important for optimizing the performance in high frequency range. Bypass capacitors must be placed as close as possible to the IC pins to improve high frequency bypassing. A capacitor greater than 1µF is necessary to minimize the distortion. For a better quality bypassing a capacitor of 0.1µF will be added following the same condition of implementation. These bypass capacitors must be incorporated for the negative and the positive supplies.

(fig.32): *Circuit for power supply bypassing.*



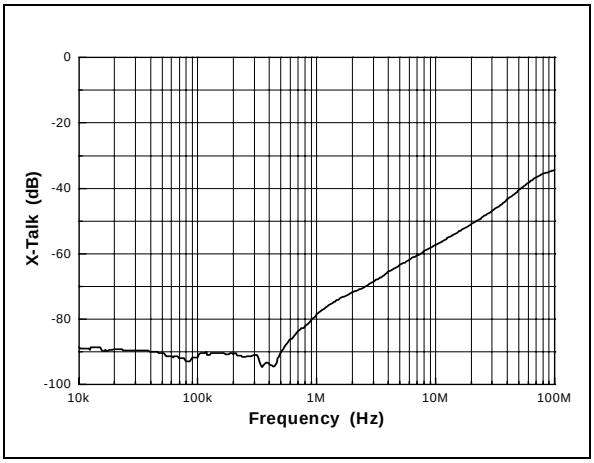
Channel Separation or Crosstalk

The following figure show the crosstalk from an amplifier to a second amplifier. This phenomenon, accented in high frequencies, is unavoidable and intrinsic of the circuit.

Nevertheless, the PCB layout has also an effect on the crosstalk level. Capacitive coupling between signal wires, distance between critical signal nodes, power supply bypassing, are the most significant points.

(fig.33): *Crosstalk vs. Frequency.*

A_V=+2, R_{fb}=680Ω, C_{fb}=2pF, R_L=100Ω, Vcc=±6V, ±2.5V

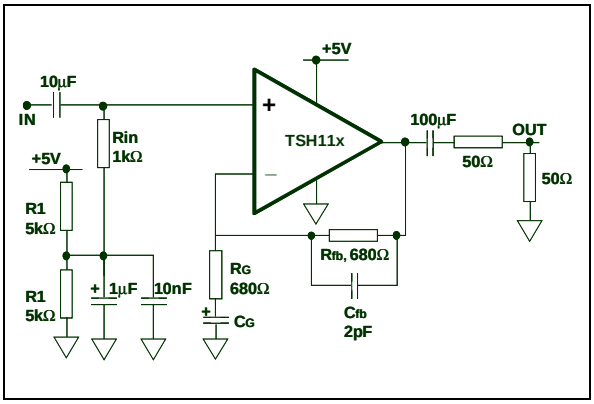


Single Power Supply

The TSH11x operates from 12V down to 5V power supplies. This is achieved with a dual power supply of ±6V and ±2.5V or a single power supply of 12V and 5V referenced to the ground. In the case of this asymmetrical supplying, a biasing is necessary to assume a positive output dynamic range between 0V and +Vcc supply rails. Considering the values of VOH and VOL, the amplifier will provide an ouput dynamic from +1.35V to 10.75V for a 12V supplying, from 0.6V to 4.5V for a 5V supplying.

The following figure show the case of a 5V single power supply configuration.

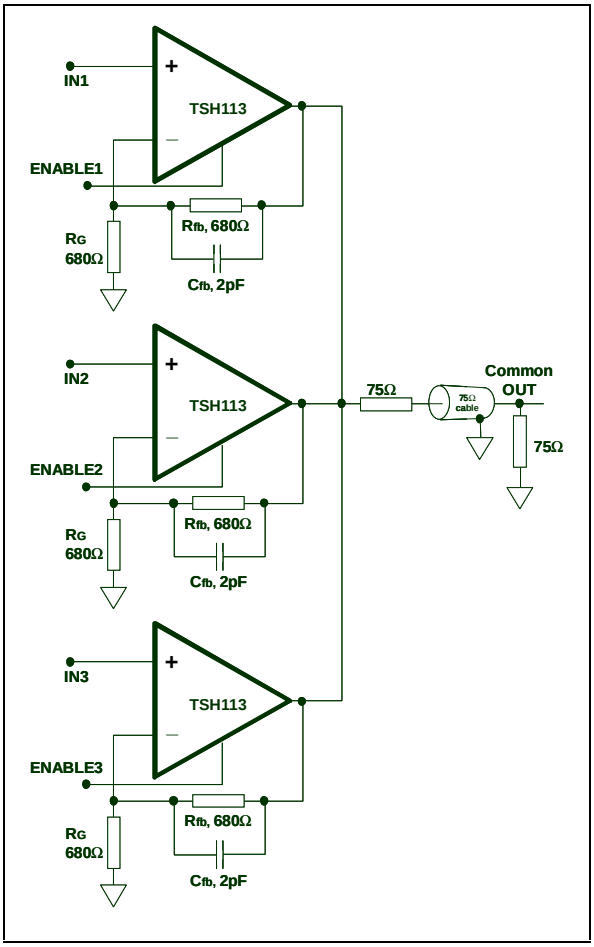
(fig.34): *Circuit for +5V single supply.*



The amplifier must be biased with a mid supply (nominaly +Vcc/2), in order to maintain the DC component of the signal at this value. Several options are possible to provide this bias supply (such as a virtual ground using an operational amplifier), or a two-resistance divider which is the cheapest solution. A high resistance value is required to limit the current consumption. On the other hand, the current must be high enough to bias the non-inverting input of the amplifier. If we consider this bias current (5µA) as the 1% of the current through the resistance divider (500µA) to keep a stable mid supply, two 5kΩ resistances can be used.
The input provides a high pass filter with a break frequency below 10Hz which is necessary to remove the original 0 volt DC component of the input signal, and to hold it at 2.5V.

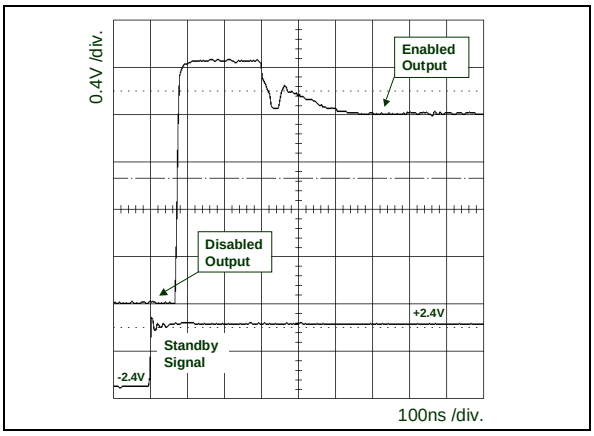
Video Multiplexing using the TSH113

(fig.35): *Circuit for switching 3 video signals with the triple TSH113.*

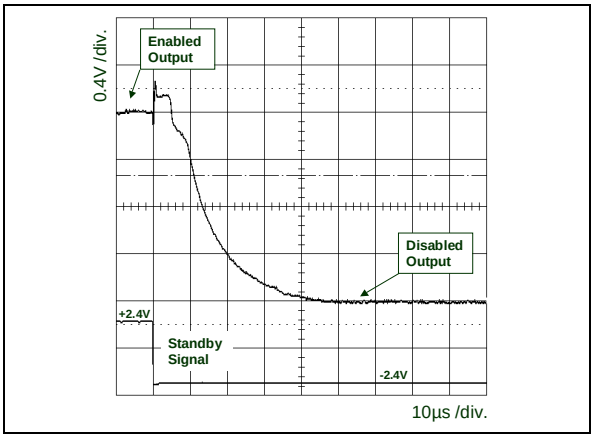


Assuming a low level active onto the disable pins (1,2,3) as described on page 7 of the datasheet, any operator can be disable/enable independently. The two disabled operators will be in standby mode featuring a high ouput impedance with a high input/output isolation and a low quiescent current.

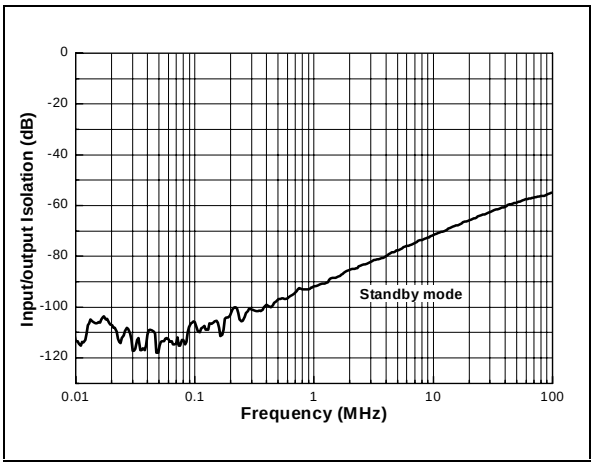
(fig.36): *Typical output response in standby mode on/off*



(fig.37): *Typical output response in standby mode off/on*



(fig.38): *Input / Output Isolation vs. Frequency..*



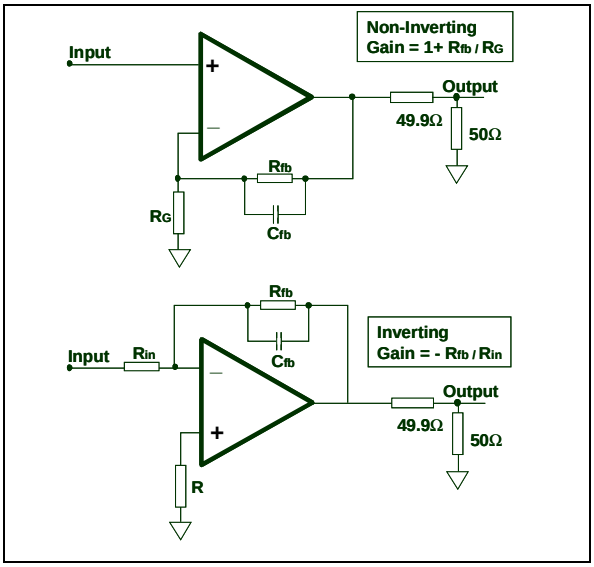
Choice of the Feedback Circuit

The TSH11x is a serie of current feedback amplifiers. For a current feedback structure the bandwidth depends on the value of the feedback components and the value of supply voltage.

A good choice of these components is necessary to achieve the gain flatness and the stability.

The following table shows the typical -3dB bandwidth and 0.1dB bandwidth assuming different gains and power supply on 100Ω load. Please see also the Closed Loop Gain vs. Frequency curves on page 8 of the datasheet.

(fig.39): *Non-inverting and Inverting Implementation..*



(tab.1): *Closed-loop Gain and Feedback Components.*

V_{CC} (V)	Gain	R_{fb} (Ω)	C_{fb} (pF)	-3dB Bw (MHz)	0.1dB Bw (MHz)
±6	+10	510	-	46	14
	-10	510	-	42	13
	+2	680	2	105	50
	-2	680	2	90	40
	+1	2.2k	2	170	30
	-1	2.2k	2	110	20
±2.5	+10	510	-	37	13
	-10	510	-	36	12
	+2	680	2	93	25
	-2	680	2	86	30
	+1	2.2k	2	130	50
	-1	2.2k	2	100	18

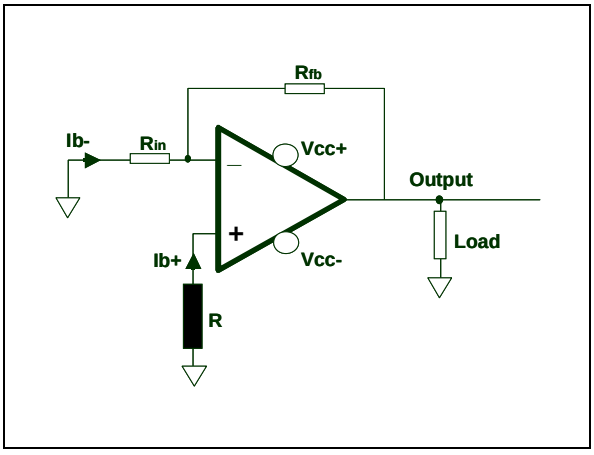
Inverting Amplifier Biasing

In this case a resistance (R on fig.40) is necessary to achieve a good input biasing.

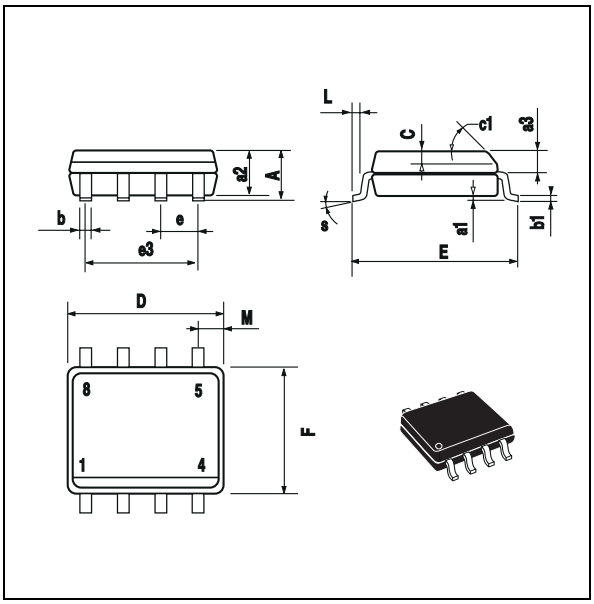
This resistance is calculated by assuming the negative and positive input bias current. The aim is to make the compensation of the offset bias current which could affect the input offset voltage and the output DC component.

Assuming Ib-, Ib+, R_{in}, R_{fb} and a zero volt output, the resistance R comes : $R = R_{in} // R_{fb}$.

(fig.40): *Compensation of the Input Bias Current..*

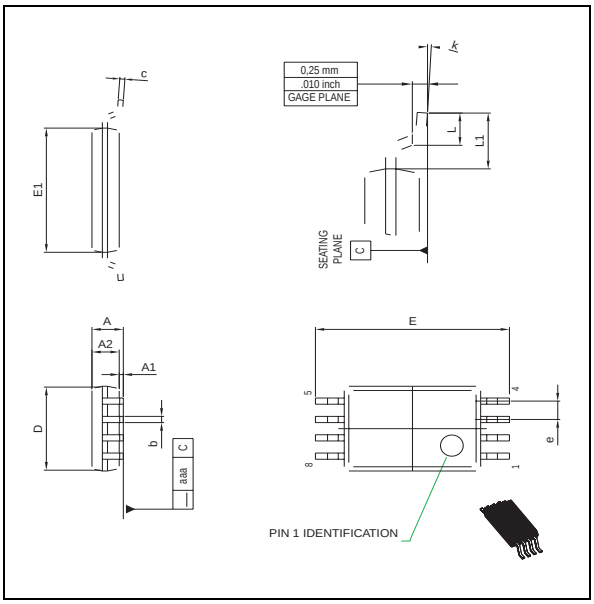


PACKAGE MECHANICAL DATA
8 PINS - PLASTIC MICROPACKAGE (SO)



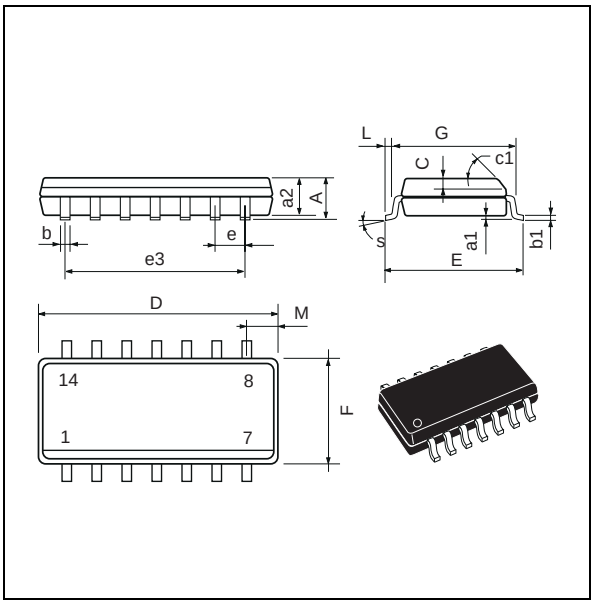
Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

PACKAGE MECHANICAL DATA
8 PINS - THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.05
A1	0.05		0.15	0.01		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.15
c	0.09		0.20	0.003		0.012
D	2.90	3.00	3.10	0.114	0.118	0.122
E		6.40			0.252	
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.025	
k	0°		8°	0°		8°
l	0.50	0.60	0.75	0.09	0.0236	0.030

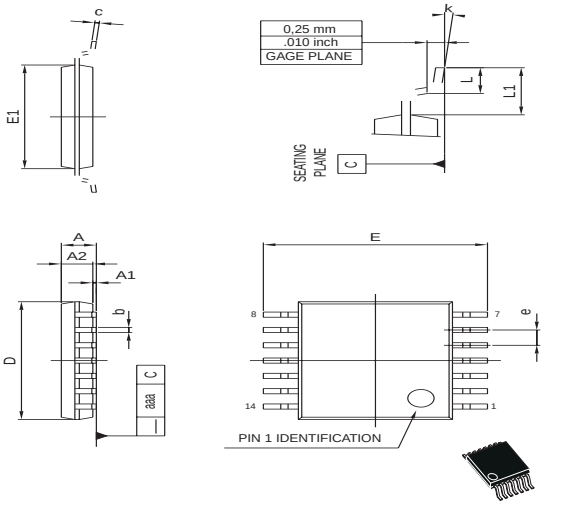
PACKAGE MECHANICAL DATA
14 PINS - PLASTIC MICROPACKAGE (SO)



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.2	0.004		0.008
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D (1)	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F (1)	3.8		4.0	0.150		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.020		0.050
M			0.68			0.027
S	8° (max.)					

Note : (1) D and F do not include mold flash or protrusions - Mold flash or protrusions shall not exceed 0.15mm (.066 inc) ONLY FOR DATA BOOK.

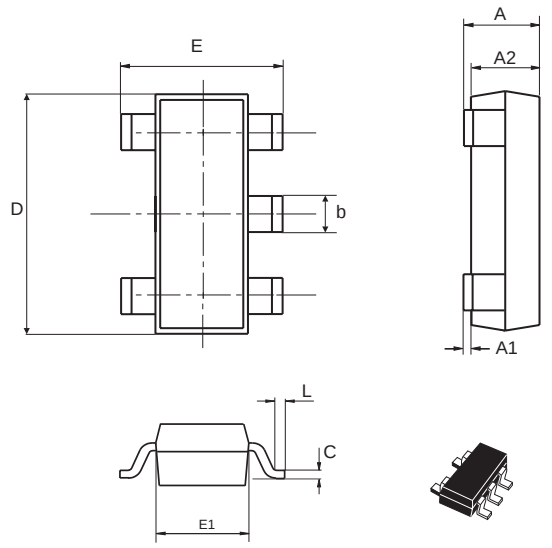
PACKAGE MECHANICAL DATA
14 PINS - THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.05
A1	0.05		0.15	0.01		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.15
c	0.09		0.20	0.003		0.012
D	4.90	5.00	5.10	0.192	0.196	0.20
E		6.40			0.252	
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.025	
k	0°		8°	0°		8°
l	0.50	0.60	0.75	0.09	0.0236	0.030

PACKAGE MECHANICAL DATA 2

5 PINS - TINY PACKAGE (SOT23)



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1	0		0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.014	0.016	0.020
C	0.09	0.15	0.20	0.004	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.0118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.5	0.60	0.004	0.014	0.024
K	0d		10d	0d		10d