

SP8902 (MP)

5GHZ ÷2 Fixed Modulus Divider

March 2007

Data Sheet

The SP8902 is one of a range of very high speed low power prescalers for professional applications. The dividing elements are static D type flip flops and therefore allow operation down to DC if the drive signal is a pulse waveform with fast risetime. The output stage has a differential current output and provides a direct drive into a 50 ohm load.

Features

- Very High Operating Speed
- Operation down to DC with Square Wave Input
- Silicon Technology for Low Phase Noise (Typically better than -140dBc/Hz at 1KHz)
- 5V Single Supply Operation
- Low Power Dissipation: 335mW (Typ.)
- Surface Mount Plastic Package

Ordering Information

SP8902/KG/MP1S (tubes) SP8902/KG/MP1T (tape and reel)

Absolute Maximum Ratings

Supply voltage, V _{CC}	6·5V
Storage temperature	-65°C to +150°C
Maximum junction temperatu	re +150°C
Prescaler input voltage	2·5Vp-p
Operating temperature	KG-40°C to +85°C T _{CASE}

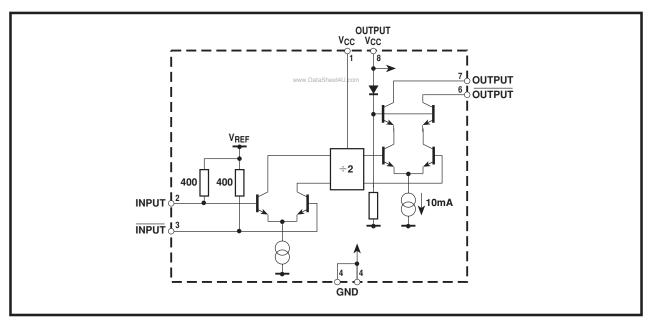


Figure 1 block diagram

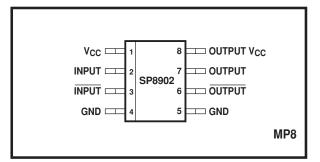


Figure 2 Pin connections - top view

Electrical Characteristics

These characteristics are guaranteed by either production test or design over the following range of operating conditions unless otherwise stated: $T_{AMB} = -40^{\circ}$ C to $+85^{\circ}$ C, $V_{CC} = 4.75$ V to 5.25V

		Value						
Characteristic	Pin	Min.	Тур.	Max.	Units	Conditions		
Supply current	1, 8	-	67	92	mA			
Input frequency	2, 3	1.0	-	5.0	GHz	RMS sinewave		
Input sensitivity	2, 3	-	-	180	mVrms	$f_{IN} = 1 GHz$ and 4.2GHz		
Input sensitivity	2, 3	-	-	570	mVrms	f _{IN} = 5GHz		
Input overload	2, 3	440	-	-	mVrms	f _{IN} = 1GHz and 3GHz		
Input overload	2, 3	700	-	-	mVrms	f _{IN} = 5.0GHz and 3.8GHz		
Output voltage	6, 7	-	0.2	-	Vp-р	Into 50 Ω pullup resistor		
Output power	6, 7	<i>−</i> 15·0	+12	+2.0	dBm	$f_{IN} = 1GHz$ and 5GHz (see note 1)		

NOTE

1. Measured into 50Ω measuring instrument in parallel with 50Ω pullup resistor. See Figure 5.

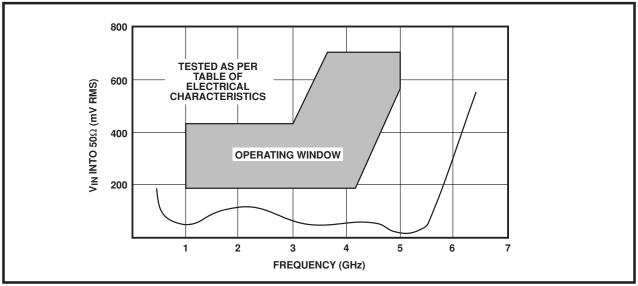


Figure3 Typical input sensitiviy (sinewave drive)

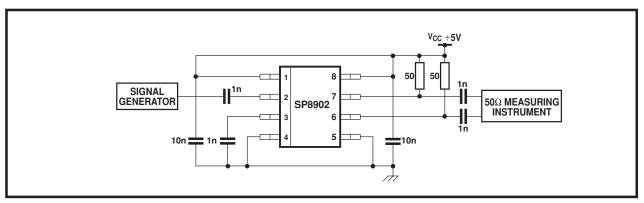


Figure 4 Typical application and test circuit

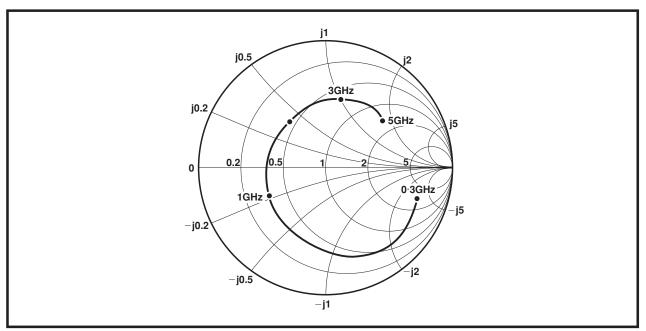


Figure 5 Typical input impedance

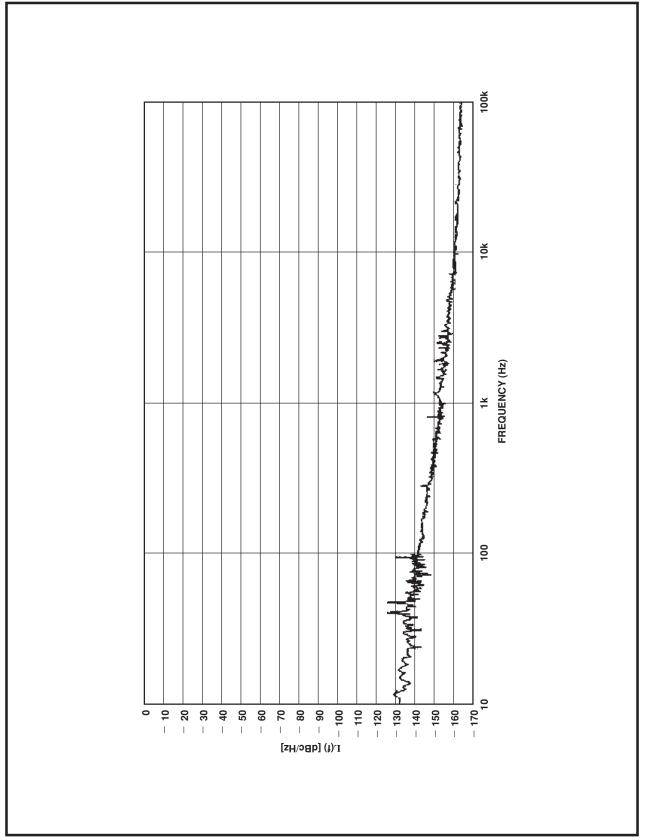
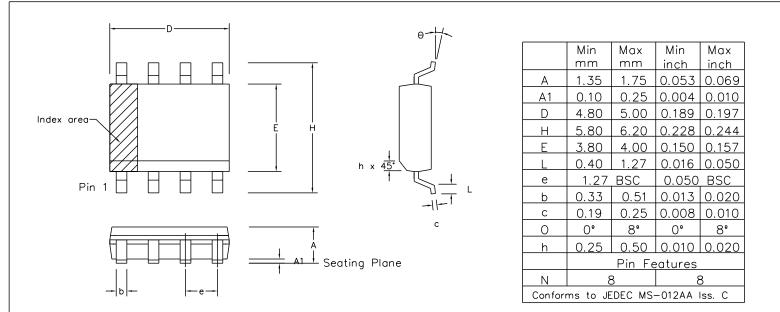


Figure 6 Typical phase noise, input frequency = 3GHz



Notes:

- 1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
- 2. Controlling dimensions are in inches.
- 3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
- 4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
- 5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

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ISSUE	1	2	3	4	5			Previous p	ackag	ge codes	Package Outline for
ACN	6745	201936	202595	203705	212424		MP	/	S	8 lead SOIC (0.150" Body width)	
DATE	5Apr95	27Feb97	12Jun97	9Dec97	22Mar02				/		
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