

## MD1822 + TC8220: Three Level High Speed $\pm 100V$ 3.0A Pulser Demoboard

### Demoboard Features

- ▶ Ultrasound high voltage & high current RTZ pulser
- ▶ MD1822 driving TC8220 with two pairs of MOSFETs
- ▶ 3-level voltage pulse waveform outputs
- ▶  $\pm 3.0A$  source and sink current capability
- ▶ 40 MHz frequency clock on board
- ▶ Programmable logic waveform generation
- ▶ JTAG connection for CPLD programming
- ▶ Connectors for external clock and signals
- ▶ 3.3V CMOS logic interface

### Applications

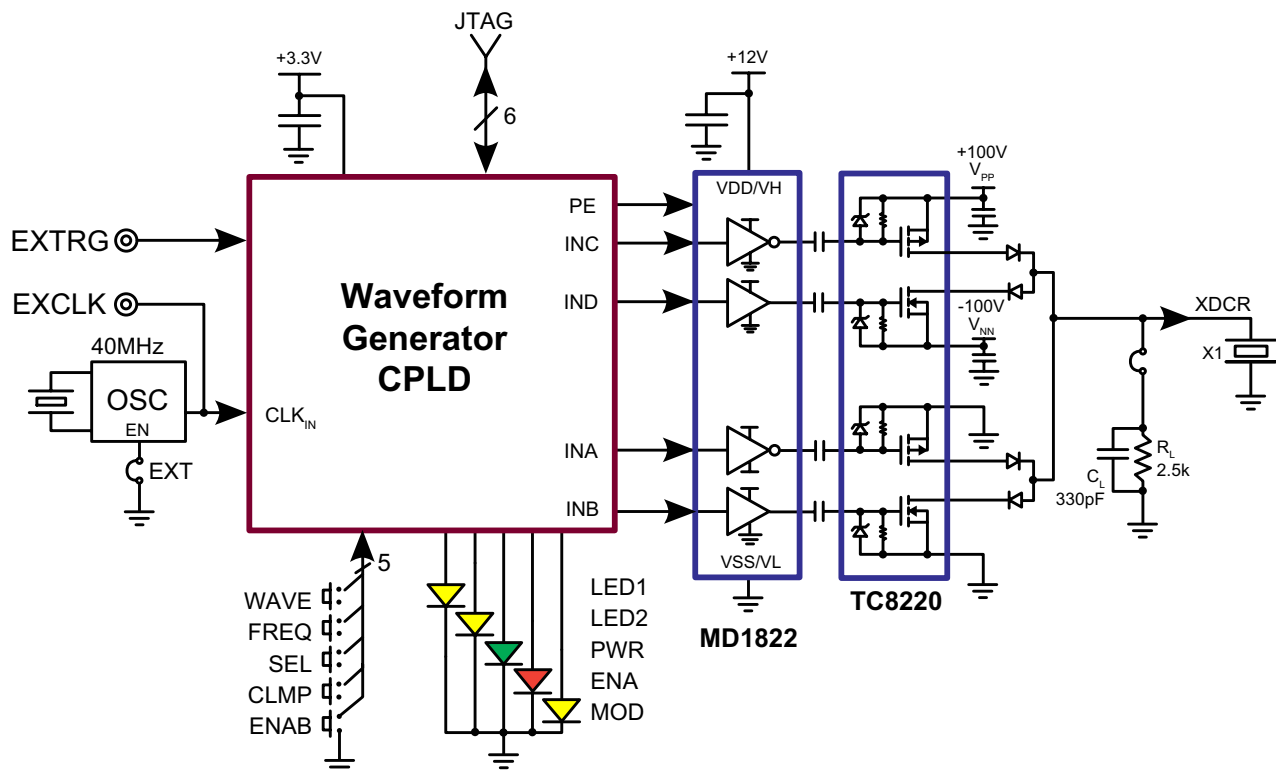
- ▶ Medical ultrasound imaging
- ▶ Piezoelectric transducer drivers
- ▶ Material flaw detection
- ▶ ATE and waveform generator
- ▶ Transducer power driver
- ▶ Capacitive and MEMS sensor driver
- ▶ Ultrasonic NDT detection and sonar ranger

### General Description

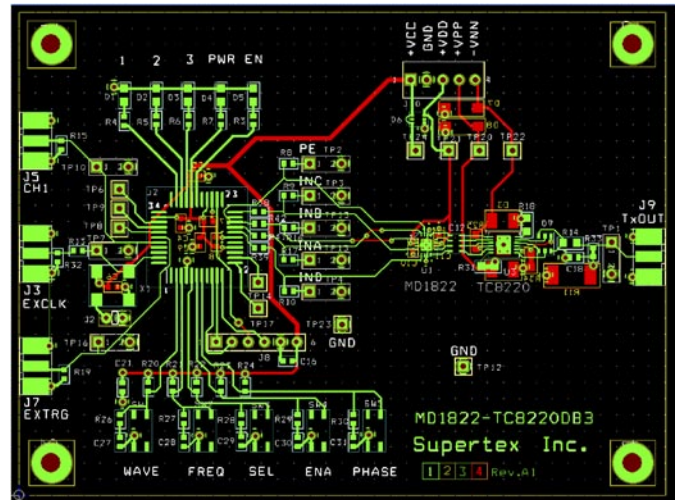
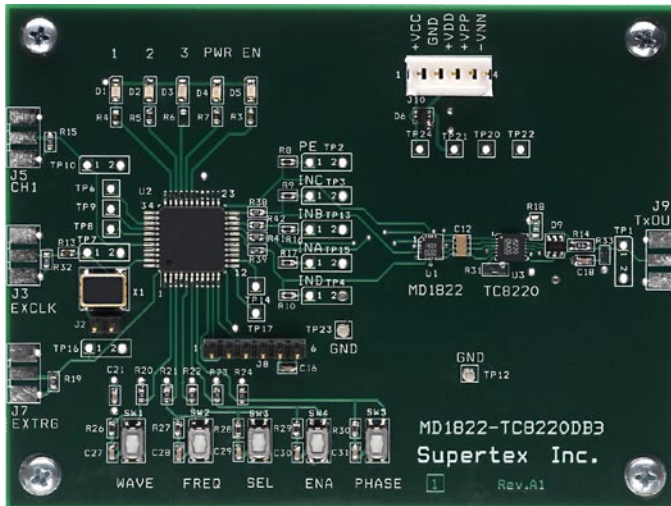
The MD1822DB3 is a demoboard for the three level  $\pm 100V$  2.5A pulser chip-set of the MD1822 MOSFET driver and the TC8220 MOSFET. The demoboard consists of one MD1822 in the 3x3mm 16-lead QFN package driving the TC8220 which has two pairs of high speed and high voltage complementary P- and N-MOSFETs in in one 4x4mm, 8-lead DFN package. This circuit is an ideal, cost-optimized, high voltage and high current RTZ ultrasound transmit pulser.

The CPLD-programmable logic circuit (40 MHz crystal oscillator) generates accurately timed high-speed waveforms on a separate CPL board. Multiple frequency and waveform combinations can be selected as bipolar pulse waveforms. An external clock input can be used if the on-board oscillator is disabled. The external trigger input can be used to synchronize the output waveforms. There are five push buttons for selecting demonstration waveform, frequency, phase, and mode functions. Color LEDs indicate the demo selection states. Jumpers on the board can select either the 330pF/2.5k on-board load, or user test loads.

### Block Diagram



## MD1822DB3 Board and PCB Layout



Actual size = 100mm x 70mm

### Operating Supply Voltages and Current (on J10)

| Symbol          | Parameter                 | Min  | Typ | Max  | Units | Suggested Current Limit * |
|-----------------|---------------------------|------|-----|------|-------|---------------------------|
| VCC             | Logic supply              | 1.8  | 3.3 | 3.3  | V     | 150mA                     |
| GND             | Circuit Ground or 0V      | -    | 0   | -    | V     | ---                       |
| VDD             | MD1822 Positive Supply    | 5.0  | 10  | 11.5 | V     | 10mA                      |
| VPP             | TC8220 HV positive supply | 0    | -   | 100  | V     | 5.0mA                     |
| V <sub>NN</sub> | TC8220 HV negative supply | -100 | -   | 0    | V     | 5.0mA                     |

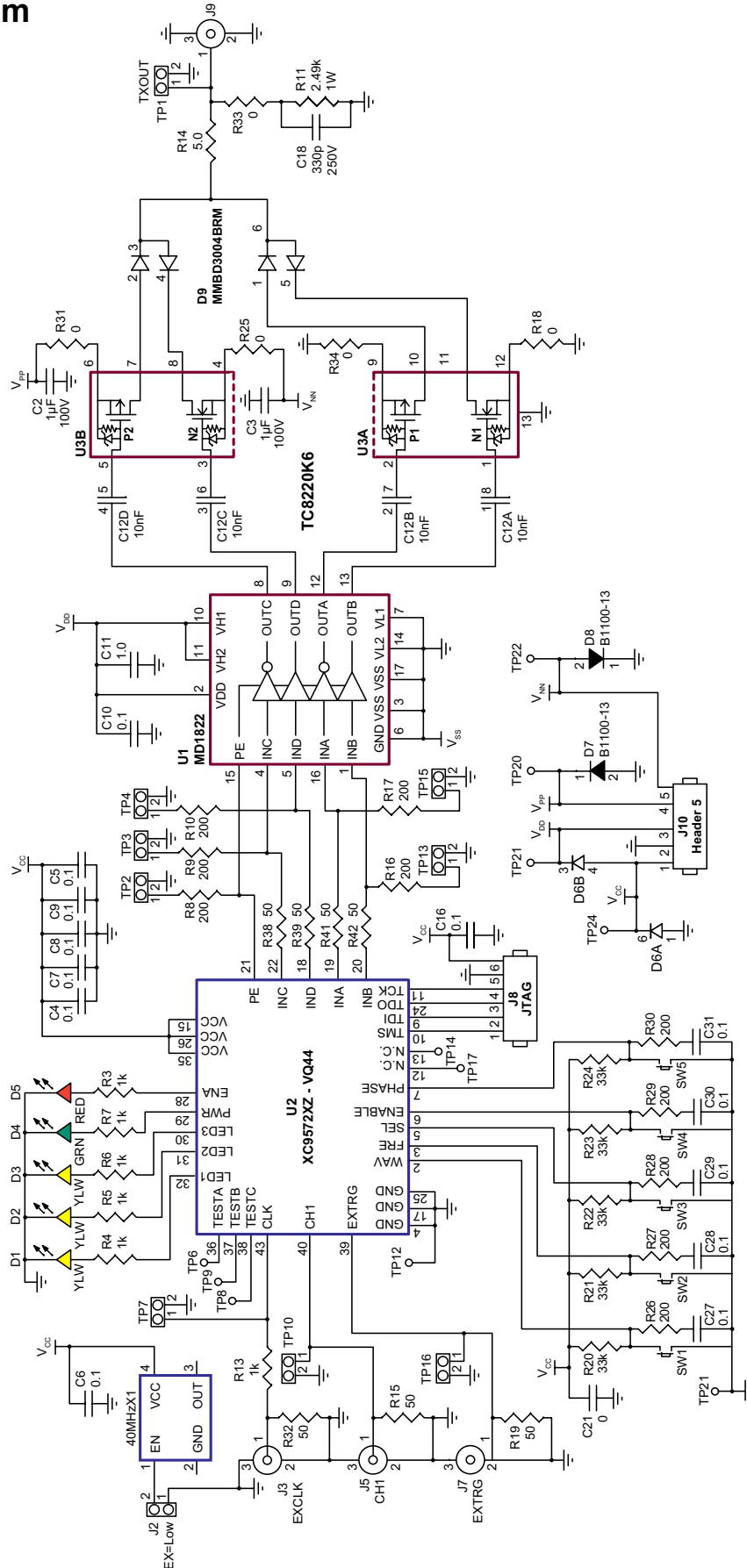
**Note:**

\* Current limits should be changed according the testing waveform, frequency and duty cycles.

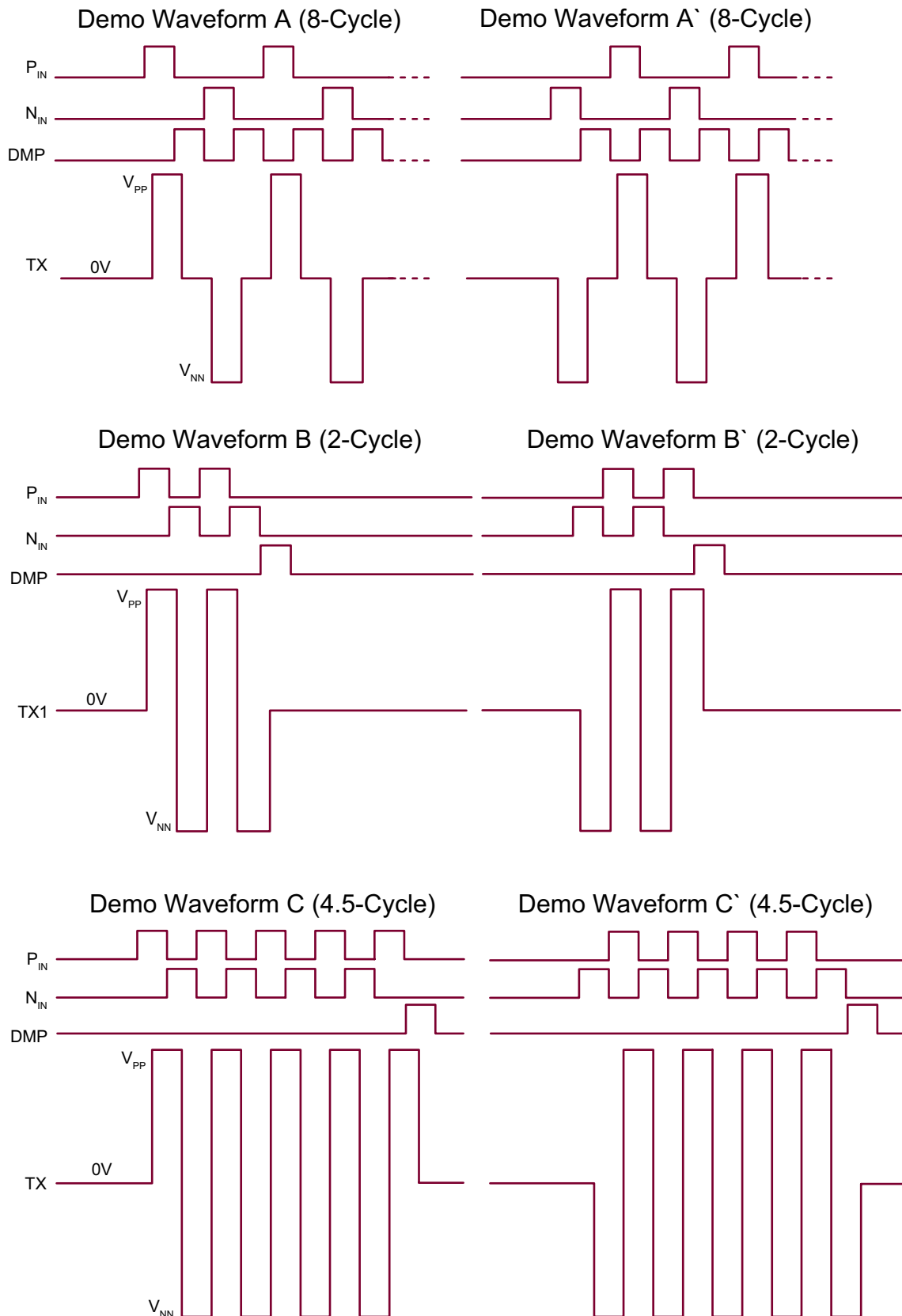
### Push Button Operation Functions

| Button Symbol | Description                       |
|---------------|-----------------------------------|
| WAVE          | Demo waveforms selection          |
| FREQ          | Demo waveform frequency selection |
| SEL           | Not Used                          |
| ENA           | MD1822 PE pin control             |
| PHASE         | Not Used                          |

Schematic Diagram

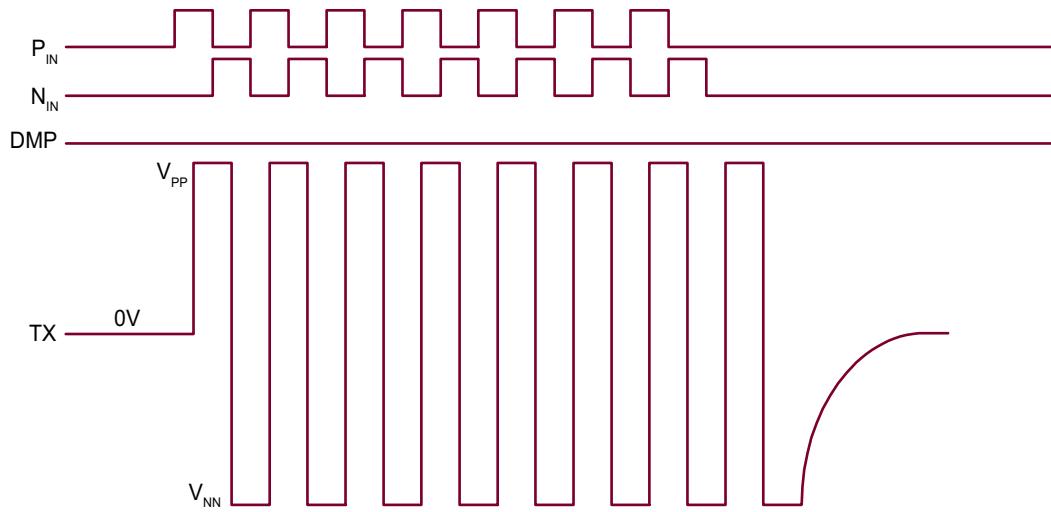


Demo Waveforms

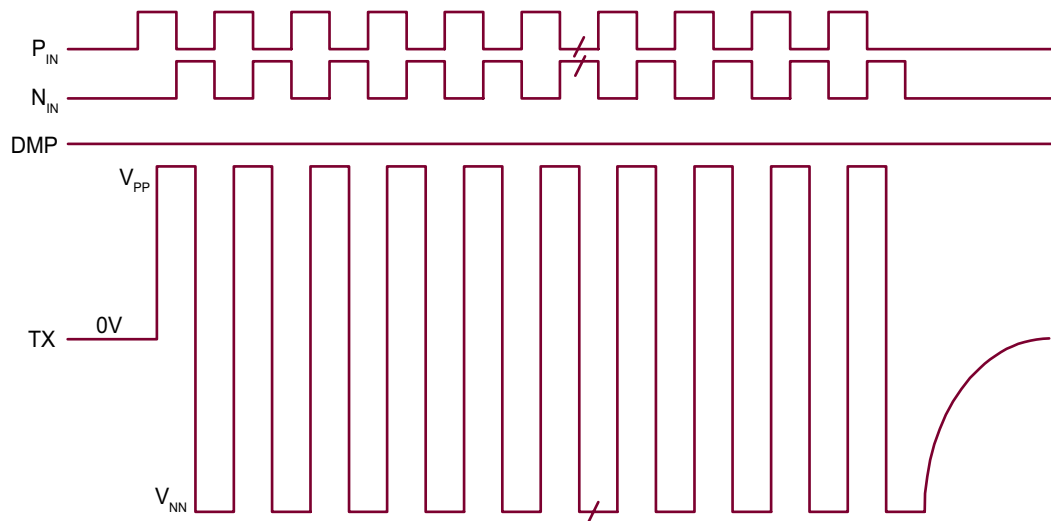


Demo Waveforms (cont.)

Demo Waveform D (8-Cycle w/o Damping)



Demo Waveform E (16-Cycle w/o Damping)



## Test Waveforms

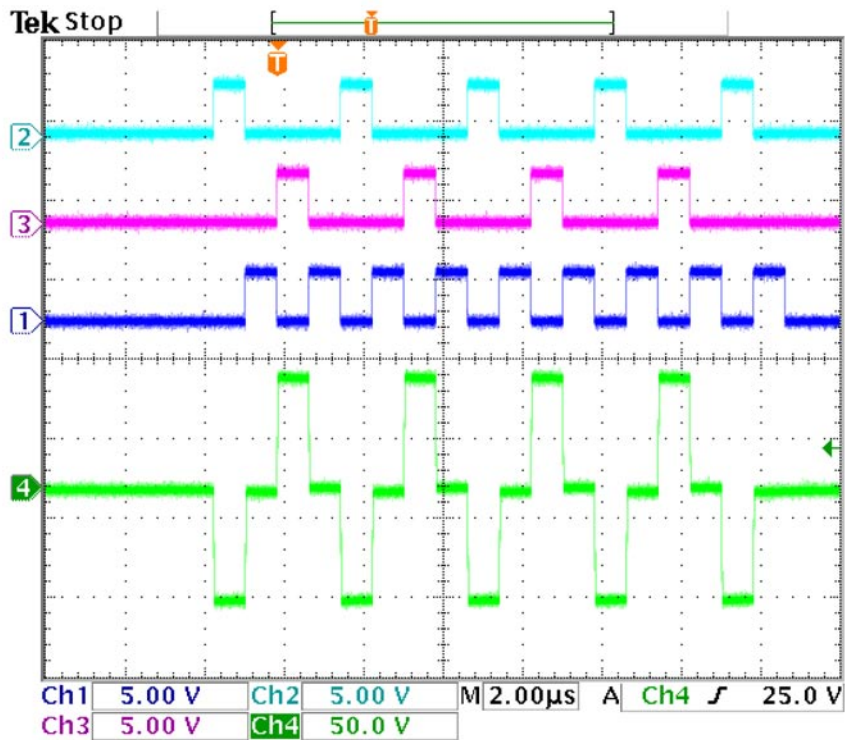


Fig 1: Input and output waveforms at  $V_{DD} = 10V$ ,  $V_{PP}/V_{NN} = \pm 70V$ , Load = 330pF//2.5k.

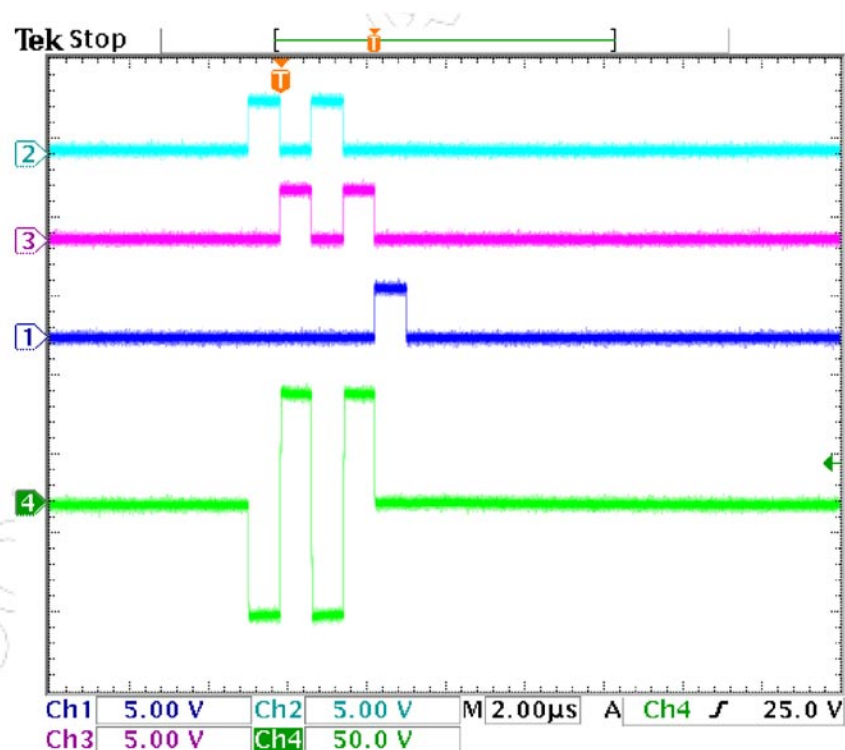


Fig 2: Input and output waveforms at  $V_{DD} = 10V$ ,  $V_{PP}/V_{NN} = \pm 70V$ , Load = 330pF//2.5k.



Test Waveforms (cont.)

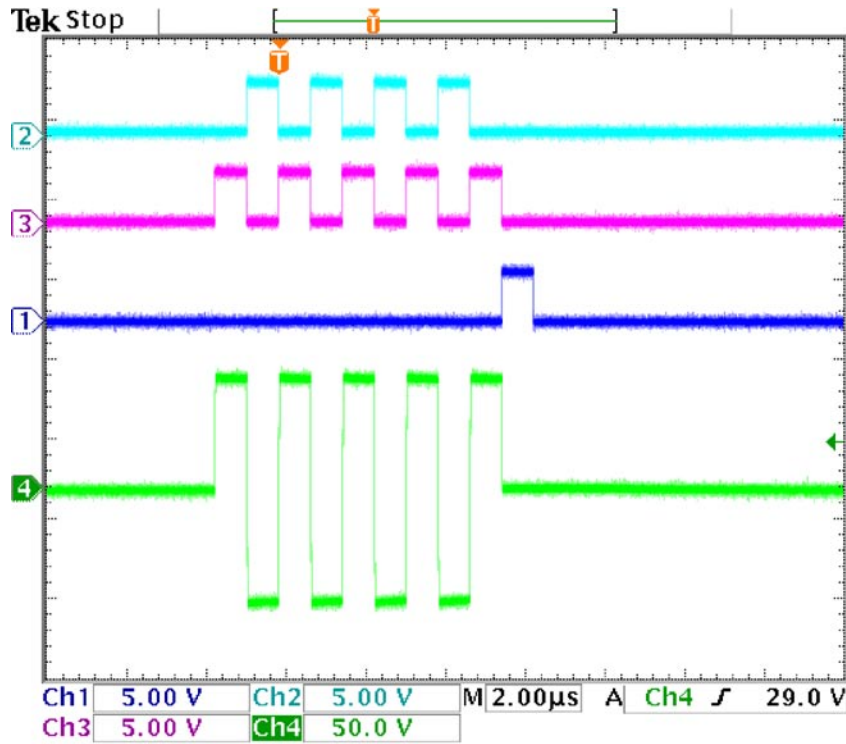


Fig 3: Input and output waveforms at  $V_{DD}=10V$ ,  $V_{PP}/V_{NN} = \pm 70V$ , Load = 330pF//2.5k.

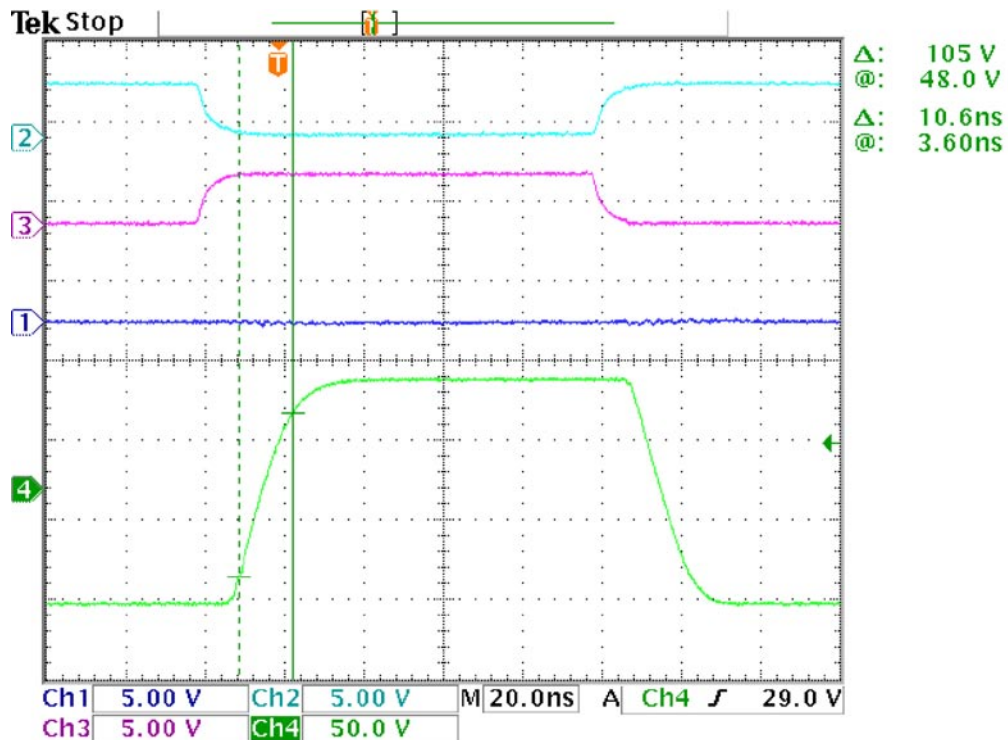


Fig 4: Input to output delay and rise time of output at  $V_{DD} = 10V$ ,  $V_{PP}/V_{NN} = \pm 70V$ , Load = 330pF//2.5k,  $I_{OUT} = 330pF(105V/10.6ns) = 3.2A$ .

Test Waveforms (cont.)

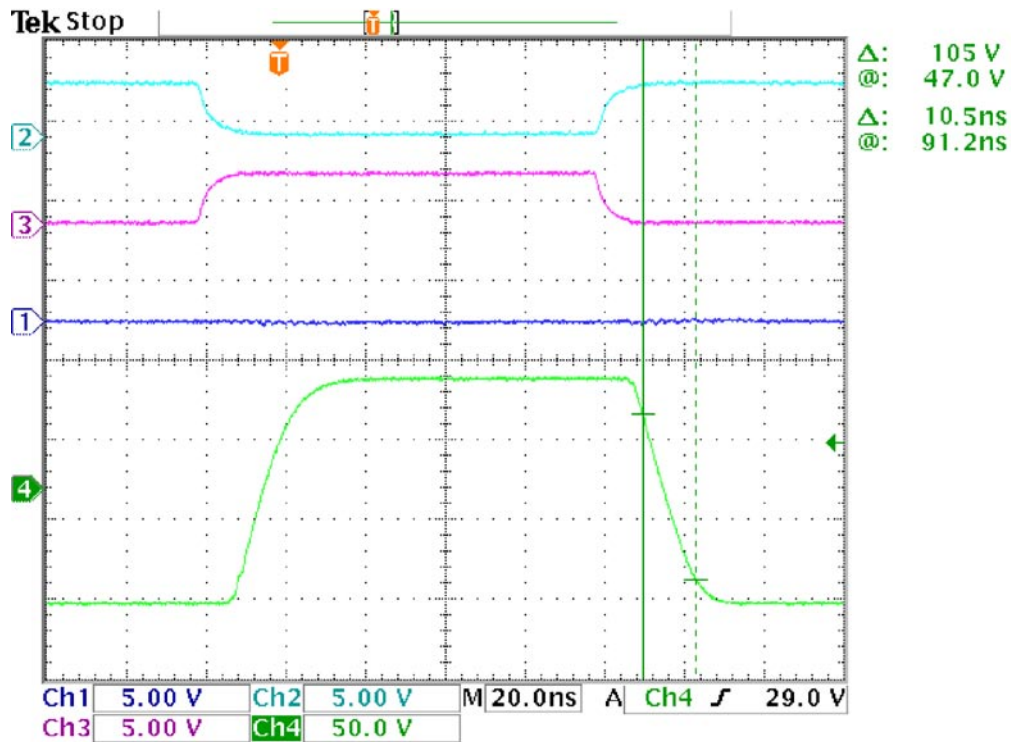


Fig 5: Input to output delay and fall time of output at  $V_{DD} = 10V$ ,  $V_{pp}/V_{NN} = \pm 70V$ , Load = 330pF//2.5k,  $I_{OUT} = 330pF(105V/10.5ns) = 3.2A$ .

JTAG or Boundary Scan Mode

JTAG or Boundary Scan mode is an industry standard (IEEE 1149.1, or 1532) serial programming mode. External logic from a cable, microprocessor, or other device is used to drive the JTAG specific pins, Test Data Out (TDO), Test Data

In (TDI), Test Mode Select (TMS), and Test Clock (TCK). This mode has gained popularity due to its standardization and ability to program CPLD through the same four JTAG pins. The data in this mode is loaded at one bit per TCK.

| JTAG Connector | Pin Number | Description  |
|----------------|------------|--|
| J8-1           | TMS        | Test Mode Select of CPLD.                                      |
| J8-2           | TDI        | Test Data In of CPLD.  |
| J8-3           | TDO        | Test Data Out of CPLD.   |
| J8-4           | TCK        | Test Clock of CPLD.  |
| J8-5           | GND        | Logic Power Supply Ground 0V for programming and testing only. |
| J8-6           | VCC        | Logic Power Supply +3.3V for CPLD programming or testing only. |

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