

High Speed Quad MOSFET Driver

Features

- ▶ 6.0ns rise and fall time
- ▶ 2.0A peak output source/sink current
- ▶ 1.2 to 5.0V input CMOS compatible
- ▶ ± 5.0 to ± 9.0 V supply voltage operation
- ▶ Smart logic threshold
- ▶ Low jitter design
- ▶ Quad matched channels
- ▶ Drives two N and two P-channel MOSFETs
- ▶ Outputs can swing below ground
- ▶ Built-in level translator for negative gate bias
- ▶ User-defined damping for return-to-zero application
- ▶ Low inductance quad flat no-lead package
- ▶ Thermally-enhanced package

Applications

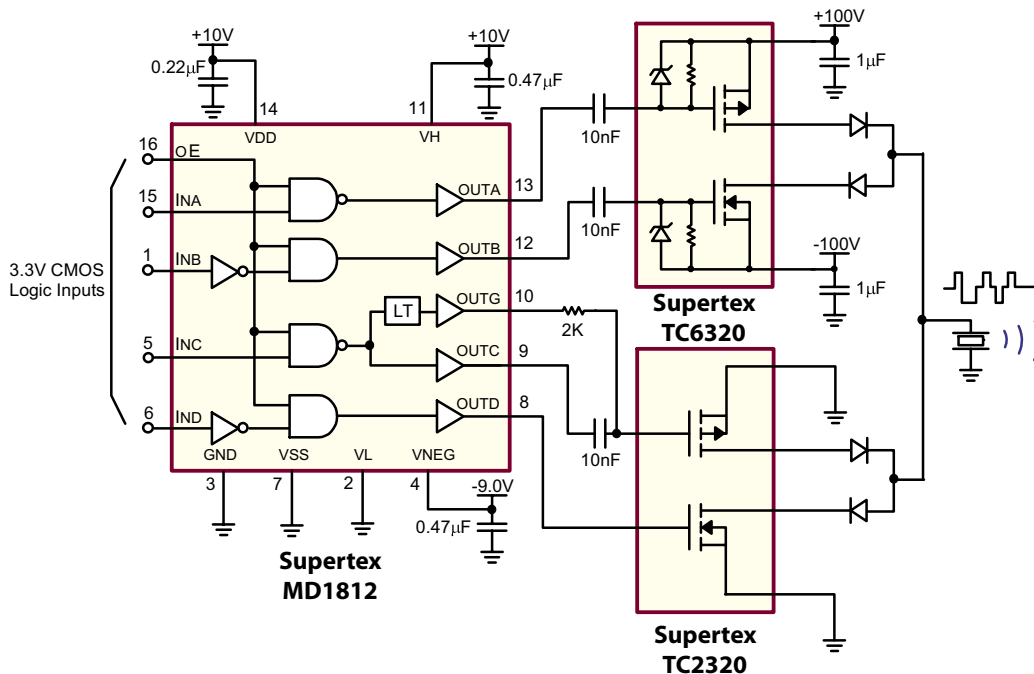
- ▶ Ultrasound PN code transmitter
- ▶ Medical ultrasound imaging
- ▶ Piezoelectric transducer drivers
- ▶ Nondestructive evaluation
- ▶ High speed level translator
- ▶ High voltage bipolar pulser

General Description

The Supertex MD1812 is a high-speed quad MOSFET driver. It is designed to drive two N and two P-channel high voltage DMOS FETs for medical ultrasound applications but may be used in any application that needs a high output current for a capacitive load. The input stage of the MD1812 is a high-speed level translator that is able to operate from logic input signals of 1.2 to 5.0V amplitude. An adaptive threshold circuit is used to set the level translator threshold to the average of the input logic 0 and logic 1 levels. The level translator uses a proprietary circuit, which provides DC coupling together with high-speed operation. The output stage of the MD1812 has separate power connections enabling the output signal L and H levels to be chosen independently from the driver supply voltages.

As an example, the input logic levels may be 0V and 1.8V, the control logic may be powered by +5V and -5V, and the output L and H levels may be varied anywhere over the range of -5.0 to +5.0V. The output stage is capable of peak currents of up to ± 2.0 amps, depending on the supply voltages used and load capacitance. The OE pin serves a dual purpose. First, its logic H level is used to compute the threshold voltage level for the channel input level translators. Secondly, when OE is low, the outputs are disabled, with the A and C outputs high and the B and D outputs low. This assists in properly pre-charging the coupling capacitors that may be used in series in the gate drive circuit of an external PMOS and NMOS. A built-in level shifter provides PMOS gate negative bias drive. This enables the user-defined damping control to generate return-to-zero bipolar output pulses.

Typical Application Circuit



Ordering Information

Device	16-Lead QFN 4x4mm body, 1.0mm height (max), 0.65mm pitch
MD1812	MD1812K6-G

-G indicates package is RoHS compliant ("Green")

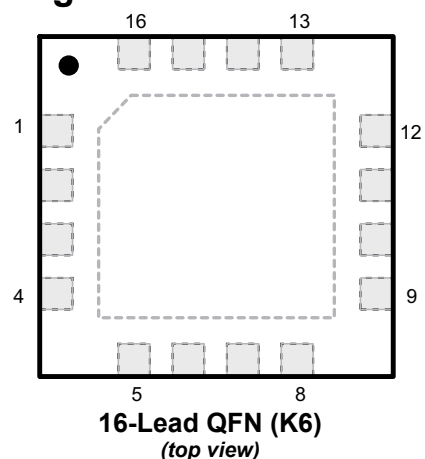


Absolute Maximum Ratings

Parameter	Value
$V_{DD}-V_{SS}$, Logic supply voltage	-0.5V to +13.5V
V_H , Output high supply voltage	$V_L - 0.5V$ to $V_{DD} + 0.5V$
V_L , Output low supply voltage	$V_{SS} - 0.5V$ to $V_H + 0.5V$
V_{SS} , Low side supply voltage	-7.0V to +0.5V
$V_{NEG}-V_{SS}$, Negative supply voltage	$V_{SS} - 10V$ to $V_{SS} + 0.5V$
Logic input levels	$V_{SS} - 0.5V$ to GND +7.0V
Maximum junction temperature	+125°C
Storage temperature	-65°C to 150°C
Soldering temperature	235°C
Package power dissipation	2.2W

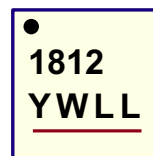
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



16-Lead QFN (K6)
(top view)

Product Marking



Y = Last Digit of Year Sealed
W = Code for Week Sealed
L = Lot Number
— = "Green" Packaging

16-Lead QFN (K6)

DC Electrical Characteristics

($V_H = V_{DD} = 12V$, $V_L = V_{SS} = GND = 0V$, $V_{NEG} = -9.0V$, $V_{OE} = 3.3V$, $T_J = 25^\circ C$)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$V_{DD} - V_{SS}$	Logic supply voltage	4.5	-	13	V	---
V_{SS}	Low side supply voltage	-5.5	-	0	V	---
V_H	Output high supply voltage	$V_{SS} + 2$	-	V_{DD}	V	---
V_L	Output low supply voltage	V_{SS}	-	$V_{DD} - 2$	V	---
V_{NEG}	Negative supply voltage	-13	-	$V_{SS} - 2$	V	May connect to VSS if OUTG not used
I_{DDQ}	V_{DD} quiescent current	-	1.5	-	mA	No input transitions, OE = 1
I_{HQ}	V_H quiescent current	-	-	10	μA	
I_{NEGQ}	V_{NEG} quiescent current	-	150	-	μA	
I_{DD}	V_{DD} average current	-	7.0	-	mA	One channel on at 5.0Mhz, No load
I_H	V_H average current	-	22	-		
I_{NEG}	V_{NEG} average current	-	1.5	-		

DC Electrical Characteristics (cont.) $(V_H = V_{DD} = 12V, V_L = V_{SS} = GND = 0V, V_{NEG} = -9.0V, V_{OE} = 3.3V, T_J = 25^\circ C)$

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{IH}	Input logic voltage high	$V_{OE} - 0.3$	-	5.0	V	For logic inputs INA, INB, INC, and IND
V_{IL}	Input logic voltage low	0	-	0.3		
I_{IH}	Input logic current high	-	-	1.0	μA	
I_{IL}	Input logic current low	-	-	1.0		
V_{IH}	OE Input logic voltage high	1.2	-	5.0	V	For logic input OE
V_{IL}	OE Input logic voltage low	0	-	0.3		
R_{IN}	Input logic impedance to GND	12	20	30	K Ω	
C_{IN}	Logic input capacitance	-	5.0	10	pF	---

AC Electrical Characteristics $(V_H = V_{DD} = 12V, V_L = V_{SS} = GND = 0V, V_{NEG} = -9.0V, V_{OE} = 3.3V, T_J = 25^\circ C)$

Sym	Parameter	Min	Typ	Max	Units	Conditions
t_{if}	Input or OE rise & fall time	-	-	10	ns	Logic input edge speed requirement
t_{PLH}	Propagation delay when output is from low to high	-	7.0	-	ns	$C_{LOAD} = 1000pF$, see timing diagram Input signal rise/fall time 2ns
t_{PHL}	Propagation delay when output is from high to low	-	7.0	-		
t_{POE}	Propagation delay OE to output	-	9	-		
t_{PCG}	Propagation delay INC to OUTG	-	28	-		
t_r	Output rise time	-	6.0	-		
t_f	Output fall time	-	6.0	-		
$ t_r - t_f $	Rise and fall time matching	-	1.0	-	ns	for each channel
$ t_{PLH} - t_{PHL} $	Propagation low to high and high to low matching	-	1.0	-		
Δt_{dm}	Propagation delay matching	-	± 2.0	-	ns	Device to device delay match

Outputs $(V_H = V_{DD} = 12V, V_L = V_{SS} = GND = 0V, V_{NEG} = -9.0V, V_{OE} = 3.3V, T_J = 25^\circ C)$

Sym	Parameter	Min	Typ	Max	Units	Conditions
R_{SINK}	Output sink resistance	-	-	12.5	Ω	$I_{SINK} = 50mA$
R_{SOURCE}	Output source resistance	-	-	12.5	Ω	$I_{SOURCE} = 50mA$
I_{SINK}	Peak output sink current	-	2.0	-	A	---
I_{SOURCE}	Peak output source current	-	2.0	-	A	---

Application Information

For proper operation of the MD1812, low inductance bypass capacitors should be used on the various supply pins. The GND pin should be connected to the logic ground. The INA, INB, INC, IND and OE pins should be connected to a logic source with a swing of GND to VCC, where VCC is 1.2 to 5.0 volts. When input logic(s) is high, output(s) will swing to VL, and when input(s) logic is low, output(s) will swing to VH. All inputs must be kept low until the device is powered up. Good trace practices should be followed corresponding to the desired operating speed. The internal circuitry of the MD1812 is capable of operating up to 100MHz, with the primary speed limitation being the loading effects of the load capacitance. Because of this speed and the high transient currents that result with capacitive loads, the bypass capacitors should be as close to the chip pins as possible. Unless the load specifically requires bipolar drive, the VSS and VL pins should have low inductance feed-through connections directly to a ground plane. If these voltages are not zero, then they need bypass capacitors in a manner similar to the positive power supplies. The power connection VDD should have a ceramic bypass capacitor to the ground plane, with short leads and decoupling components to prevent resonance in the power leads.

Output drivers, OUTA and OUTC, drive the gate of an external P-channel MOSFET, while output drivers OUTB and OUTD drive the gate of an external N-channel MOSFET, and they all swing from VH to VL. The auxiliary output drive, OUTG, swings from VSS to VNEG, and drives the gate of an external P-channel MOSFET via a 2.0K Ω series resistor.

The voltages of VH and VL decide the output signal levels. These two pins can draw fast transient currents of up to 2.0A, so they should be provided with an appropriate bypass capacitor located next to the chip pins. A ceramic capacitor of up to 1.0 μ F may be appropriate, with a series ferrite bead to prevent resonance in the power supply lead coming to the capacitor. Pay particular attention to minimizing trace lengths, current loop area, and using sufficient trace width to reduce inductance. Surface mount components are highly recommended. Since the output impedance of this driver is very low, in some cases it may be desirable to add a small series resistance in series with the output signal to obtain better waveform transitions at the load terminals. This will reduce the output voltage slew rate at the terminals of a capacitive load.

The OE pin sets the threshold level of logic for inputs ($V_{OE} + V_{GND}$) / 2. When OE is low, OUTA and OUTC are at VH. OUTB and OUTD are at VL. Auxiliary output OUTG, is at VSS, regardless of the inputs INA or INB.

Pay particular attention that parasitic couplings are minimized from the output to the input signal terminals. The parasitic feedback may cause oscillations or spurious waveform shapes on the edges of signal transitions. Since the input operates with signals down to 1.2V, even small coupled voltages may cause problems. Use of a solid ground plane and good power and signal layout practices will prevent this problem. Be careful that a circulating ground return current from a capacitive load cannot react with common inductance to cause noise voltages in the input logic circuitry. Best timing performance is obtained for OUTC when the voltage of ($V_{SS} - V_{NEG}$) = ($V_H - V_L$).

Logic Truth Table

Logic Inputs			Output		
OE	INA	INB	OUTA	OUTB	
H	L	L	V_H	V_H	
H	L	H	V_H	V_L	
H	H	L	V_L	V_H	
H	H	H	V_L	V_L	
L	X	X	V_H	V_L	
OE	INC	IND	OUTC	OUTG	OUTD
H	L	L	V_H	V_{SS}	V_H
H	L	H	V_H	V_{SS}	V_L
H	H	L	V_L	V_{NEG}	V_H
H	H	H	V_L	V_{NEG}	V_L
L	X	X	V_H	V_{SS}	V_L

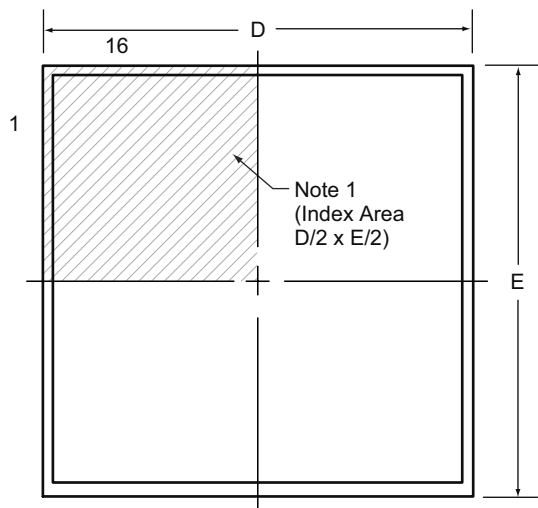
Pin Description

Pin #	Function	Description
1	INB	Logic input. Controls OUTB when OE is high.
2	VL	Supply voltage for N-channel output stage.
3	GND	Device ground.
4	VNEG	Supply voltage the auxiliary gate drive.
5	INC	Logic input. Controls OUTC when OE is high.
6	IND	Logic input. Controls OUTD when OE is high.
7	VSS	Supply voltage for low-side analog, level shifter, and gate drive circuit.
8	OUTD	Output driver.
9	OUTC	Output driver.
10	OUTG	Auxiliary output driver.
11	VH	Supply voltage for P-channel output stage
12	OUTB	Output driver.
13	OUTA	Output driver.
14	VDD	Supply voltage for high-side analog, level shifter, and gate drive circuit.
15	INA	Logic input. Controls OUTA when OE is high.
16	OE	Output enable logic input.

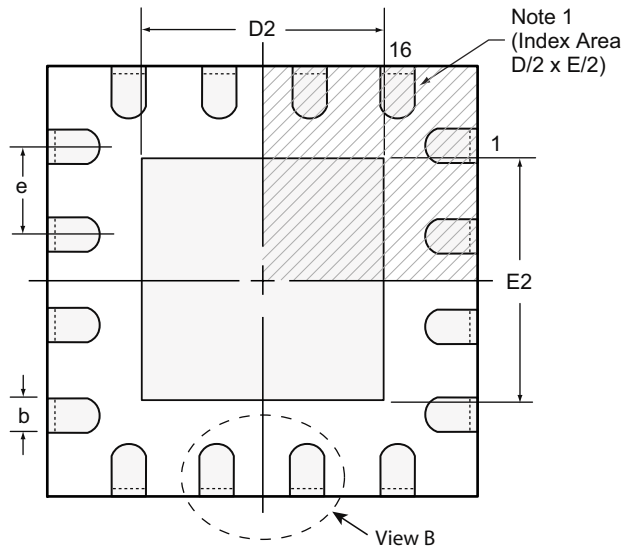
Note: Thermal pad and pin #4, VNEG must be connected externally.

16-Lead QFN Package Outline (K6)

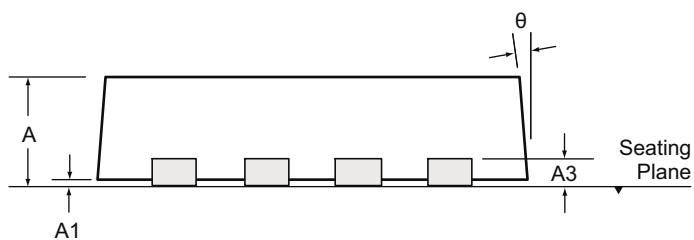
4x4mm body, 1.00mm height (max), 0.65mm pitch



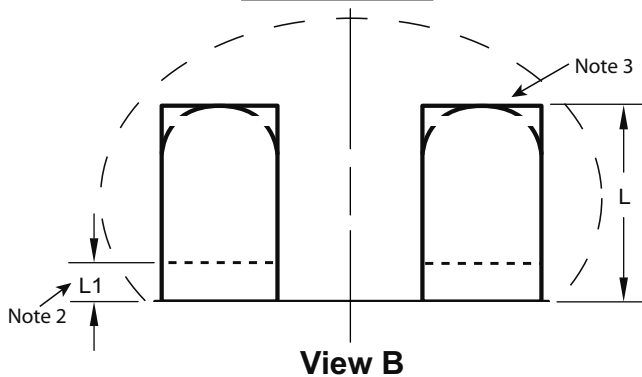
Top View



Bottom View



Side View



View B

Notes:

1. Details of Pin 1 identifier are optional, but must be located within the indicated area. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.25	3.85	2.50	3.85	2.50	0.65 BSC	0.30*	0.00	0°
	NOM	0.90	0.02		0.30	4.00	2.65	4.00	2.65		0.40*	-	-
	MAX	1.00	0.05		0.35	4.15	2.80	4.15	2.80		0.50*	0.15	14°

JEDEC Registration MO-220, Variation VGGC-2, Issue K, June 2006.

Dimensions marked with (*) are non-JEDEC dimensions. The value listed is for reference only.

Drawings not to scale.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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