PLESSEY
Semiconductors

T-45-19-05

SP8647A & B

250MHz ÷ 10/11

The SP8647 is an ECL variable modulus divider, with ECL 10K and TTL/CMOS compatible outputs. It divides by 10 when either of the ECL control inputs, $\overline{PE1}$ or $\overline{PE2}$, is in the high state and by 11 when both are low (or open circuit).

The two clock inputs are interchangeable and either will act as a clock inhibit when connected to an ECL high level. Normally, one input is left open circuit and the other is AC coupled, with externally-applied bias.

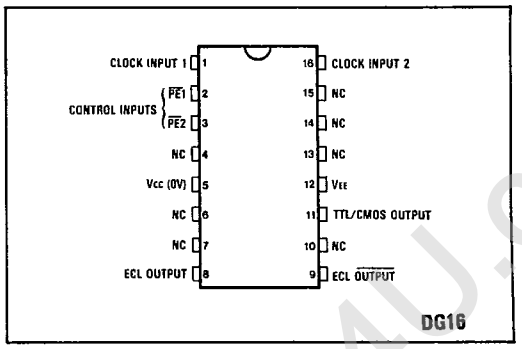

Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Inputs/Outputs
- Open Collector TTL/CMOS Output
- AC Coupled Input (External Bias)

QUICK REFERENCE DATA

- Supply Voltage V_{CC}-V_{EE} : 5.2V ± 0.25V
- Power Consumption: 260mW
- Temperature Range:
  - -55°C to +125°C (A Grade)
  - -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC} - V_{EE}	8V
Output current	20mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Open collector voltage (Pin 11)	+12V
Max. clock I/P voltage	2.5V p-p
Max. open collector current	15mA

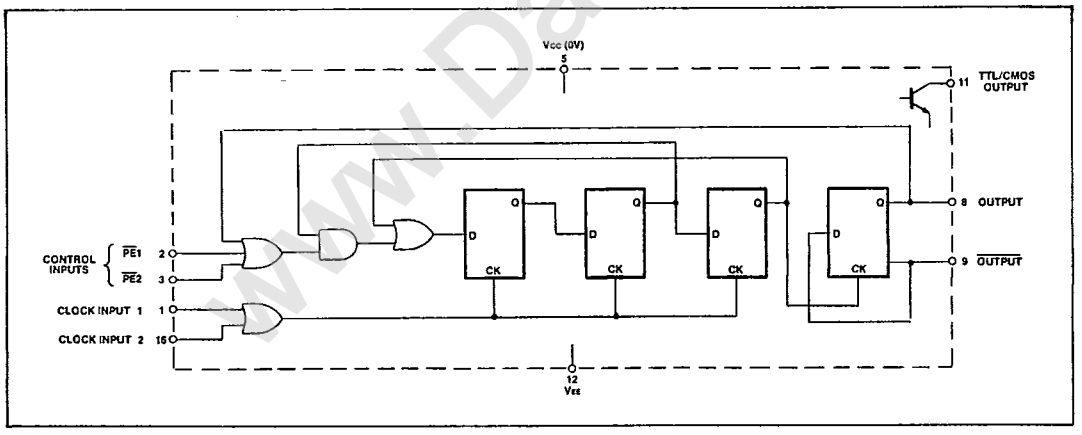

Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS (ECL OPERATION)

Supply Voltage: V_{CC} = 0V V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{amb} = -55°C to +125°C B Grade T_{amb} = -30°C to +70°C

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Characteristic	Symbol	Value Min.	Value Max.	Units	Conditions	Notes
Maximum frequency (sinewave input)	f_{max}	250		MHz	Input = 400-800mV p-p	Note 6
Minimum frequency (sinewave input)	f_{min}		50	MHz	Input = 400-800mV p-p	Note 6
Power supply current	I_{EE}		65	mA	V_{EE} = -5.2V	Note 6
ECL output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25°C)	
ECL output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
Clock and $\overline{PE}$ input high voltage	V_{INH}	-0.93		V	V_{EE} = -5.2V (25°C)	
Clock and $\overline{PE}$ input low voltage	V_{INL}		-1.62	V	V_{EE} = -5.2V (25°C)	
Clock to ECL output delay	t_p		6	ns		Note 7
Set-up time	t_s	2.5		ns		Note 7
Release time	t_r	3		ns		Note 7

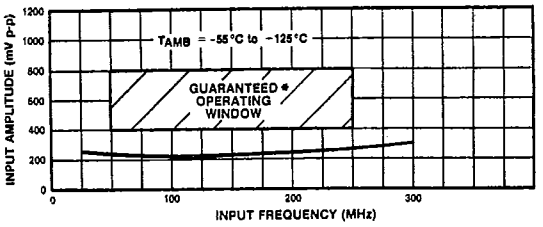
NOTES
1. Unless otherwise stated, the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C.
3. The test configuration for dynamic testing is shown in Fig.6.
4. The set up time t_s is defined as minimum time that can elapse between L → H transition of control input and the next L → H clock pulse transition to ensure that +10 is obtained.
5. The release time t_r is defined as the minimum time that can elapse between H → L transition of the control input and the next L → H clock pulse transition to ensure that the +11 mode is obtained.
6. SP8647B tested at 25°C only.
7. Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS (TTL OPERATION)

Supply Voltage: V_{CC} = 5V ± 0.25V V_{EE} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C B Grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value Min.	Value Max.	Units	Conditions	Notes
Maximum frequency (sinewave input)	f_{max}	250		MHz	Input = 400-800mV p-p	Note 3
Minimum frequency (sinewave input)	f_{min}		50	MHz	Input = 400-800mV p-p	Note 3
Power supply current	I_{EE}		65	mA		Note 3
TTL output low voltage	V_{OL}		0.5	V	V_{CC} = +5.25V Sink current = 8mA	Note 3, 5
TTL output high voltage	V_{OH}	3.5		V	V_{CC} = +5.0V	Note 3, 5
Clock to TTL output high delay (positive going)	t_{PLH}		15	ns		Note 4
Clock to TTL output low delay (negative going)	t_{PHL}		15	ns		Note 4
Set-up time	t_s	2.5		ns		Note 4
Release time	t_r	3		ns		Note 4

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. SP8647B tested at 25°C only.
4. Guaranteed but not tested.
5. TTL output for use up to 15MHz output frequency. $C_{load} \leq 5pF$.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristic of SP8647A

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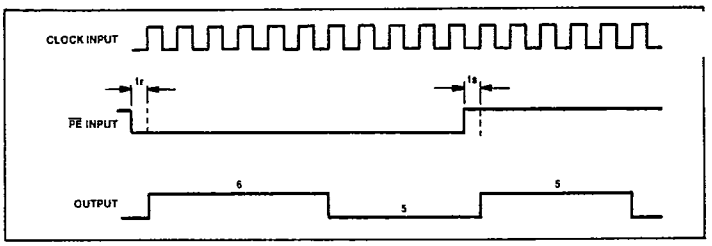

Fig.4 Timing diagram

TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	11
H	L	10
L	H	10
H	H	10

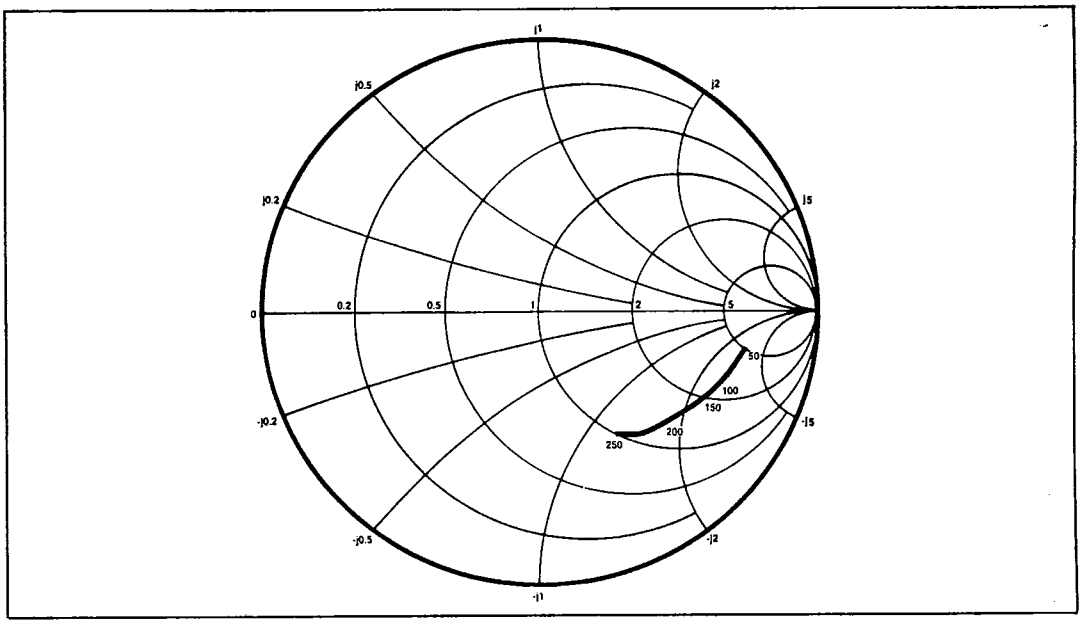

Fig.5 Typical input impedance. Test conditions: supply voltage 5V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock and control inputs are ECL III compatible. There is an internal pulldown resistor to V_{EE} of 4.3k on each input and therefore any unused input can be left open circuit. If it is desirable to capacitively couple the signal source to the clock then an external bias is required as shown in Fig. 6. The external bias voltage should be -1.3V at 25°C.
2. The outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig. 8.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. Input impedance is a function of frequency. See Fig. 5.
5. The TTL/CMOS O/P is a free collector, with an output rise/fall time which is a function of load resistance and load capacitance. The load capacitance should therefore be kept to a minimum and the load resistance should not be too small otherwise V_{OL} will be too great. eg TTL output current = 8mA V_{OL} = 0.5V. For CMOS outputs, the value of load resistor should be the maximum consistent with satisfactory rise times.
6. All components should be suitable for the frequency in use.

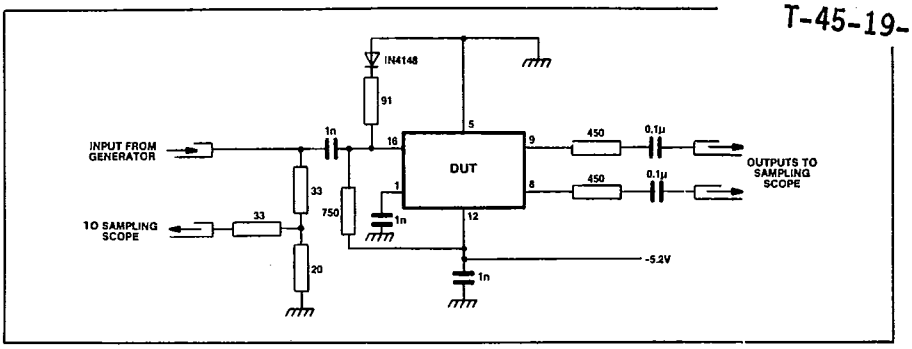

Fig.6 Test circuit

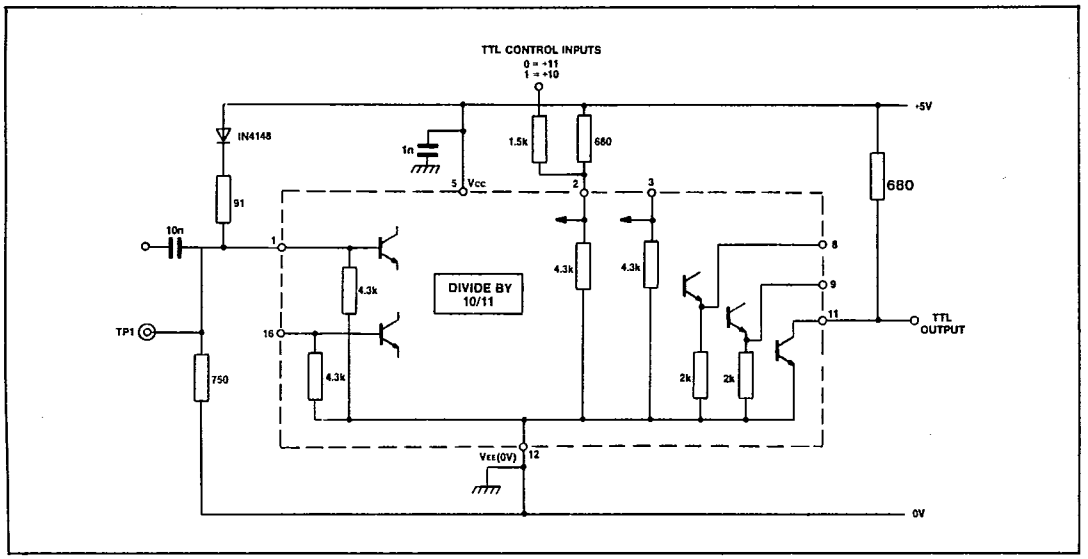

Fig.7 Typical application showing interfacing. NB Voltage at TP1 should be 3.7V at 25°

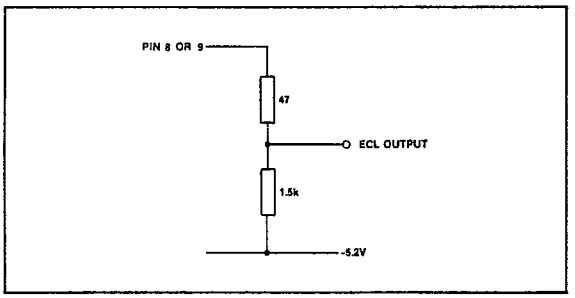

Fig.8 Interfacing to ECL 10K