PLESSEY
Semiconductors

T-45-19-05

SP8630AC

600MHz ÷ 10 FIXED MODULUS DIVIDER
(CONFORMS TO MIL-STD-883C CLASS B)

The SP8630 is an asynchronous emitter coupled logic counter which provides an ECL compatible output when used with an external pulldown resistor. It requires an AC coupled input of 600mV p-p.

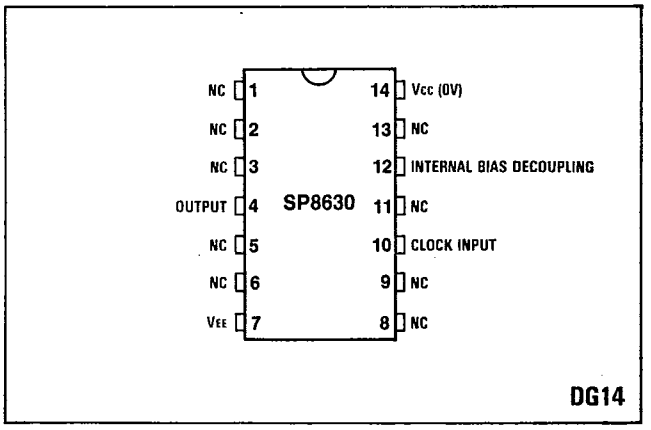


Fig.1 Pin connections - top view

FEATURES

- MIL-M-38510 Change Notification Observed
- Full Quality Conformance Inspection
- ECL Compatible Output
- AC Coupled Inputs(Internal Bias)
- Power Consumption: 350mW
- Temperature Range: -55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage:	-8V
Output current:	15mA
Storage temperature range:	-55°C to +150°C
Max. junction temperature:	+175°C
Max. clock I/P voltage:	2.5V p-p

CHANGE NOTIFICATION

The change notification requirements of MIL-M-38510 will be implemented on this device type. Known customers will be notified of any changes since last buy when ordering further parts if significant changes have been made.

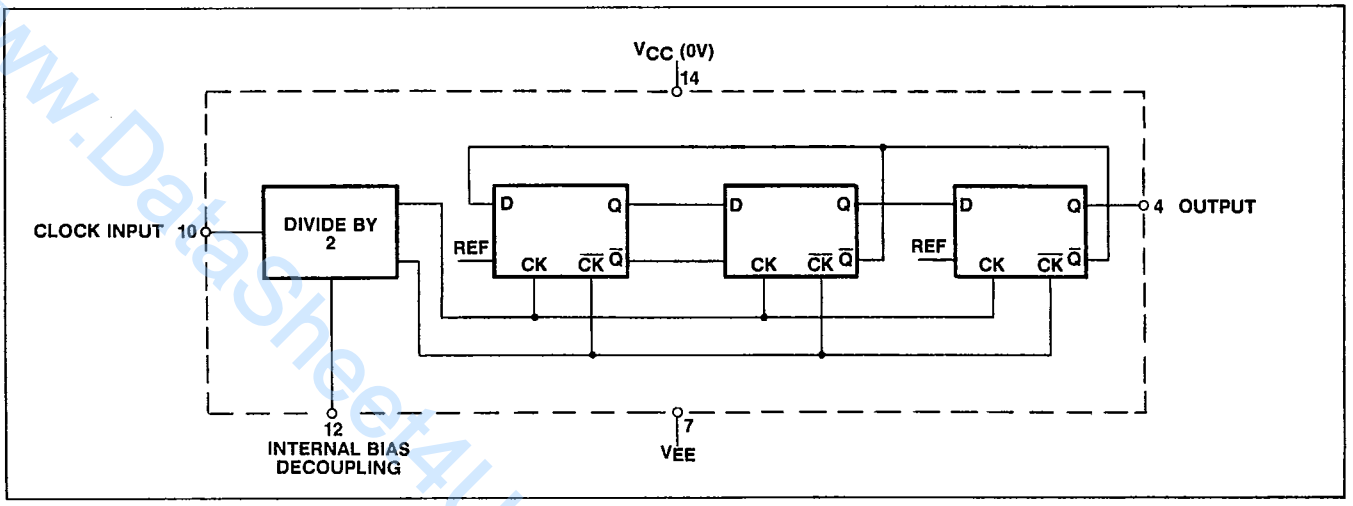


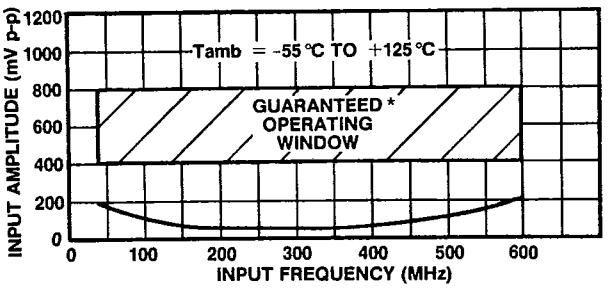
Fig.2 Functional diagram, SP8630

Rev.	A	B	
Date	11 Mar 87	13 July 87	

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Value		Sub group	Notes	Method/Conditions/Temp.
		Min.	Max.			
Operating frequency range	f_{max}	40MHz	600MHz	9,10,11	-	Input = 400mV p-p to 800mV p-p V_{EE} = -5.45V to -4.95V T_{amb} = -55°C to +125°C
Function test		-	-	7,8	Note 1	V_{EE} = -5.20V T_{amb} = -55°C to +125°C
Power supply current	I_{EE}	-	70mA	1,2,3	-	V_{EE} = -5.2V T_{amb} = -55°C to +125°C
ECL output high voltage	V_{OH}	-0.85V	-0.7V	1	-	V_{EE} = -5.2V T_{amb} = +25°C
ECL output high voltage	V_{OH}	-0.73V	-0.50V	2	-	V_{EE} = -5.2V T_{amb} = +125°C
ECL output high voltage	V_{OH}	-1.01V	-0.8V	3	-	V_{EE} = -5.2V T_{amb} = -55°C
ECL output low voltage	V_{OL}	-1.8V	-1.5V	1	-	V_{EE} = -5.2V T_{amb} = +25°C
ECL output low voltage	V_{OL}	-1.73V	-1.38V	2	-	V_{EE} = -5.2V T_{amb} = +125°C
ECL output low voltage	V_{OL}	-1.90V	-1.56V	3	-	V_{EE} = -5.2V T_{amb} = -55°C

NOTES
1. This test is carried out in conjunction with static tests (sub group 1,2 and 3) and is sufficient to verify the function of the device.
3. Sub groups 4,5,6 are not required.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristics SP8630

OPERATING NOTES

1. The clock input (pin 10) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12 to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the input to V_{EE} (i.e. Pin 10 to Pin 7). This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/μs.
4. The outputs are compatible with ECL II. There is an internal load of 3k at output. The output can be interfaced to ECL/10K by the addition of 1.5k to the output to increase the output voltage swing.
5. Input impedance is a function of frequency. See Fig.4.
6. All components should be suitable for the frequency in use.

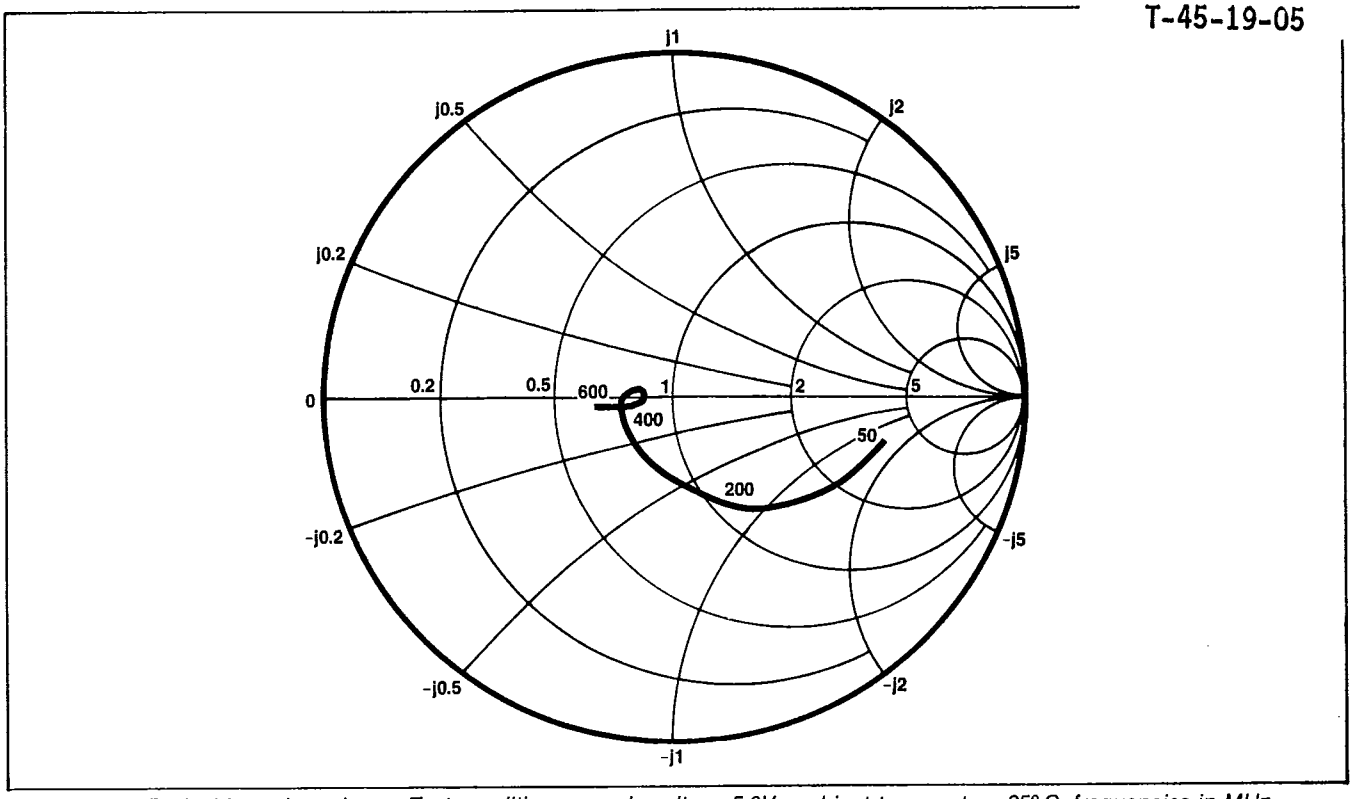


Fig.4 Typical input impedance. Test conditions: supply voltage 5.0V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

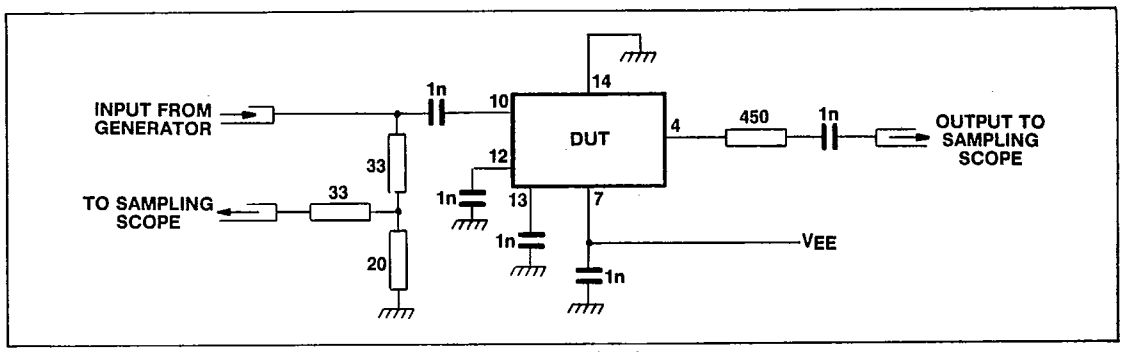


Fig.5 Test circuit

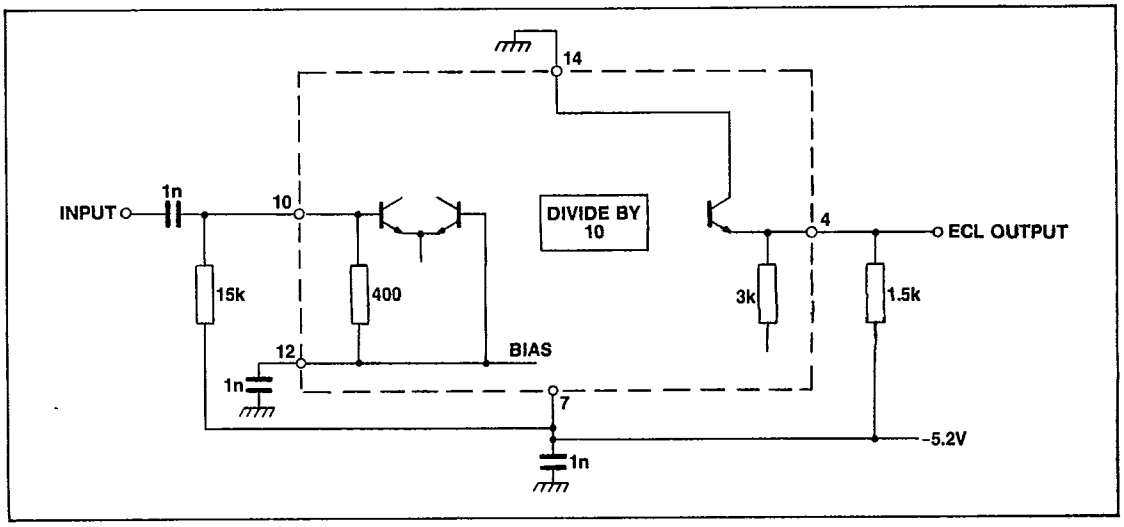


Fig.6 Typical applications circuit showing interfacing

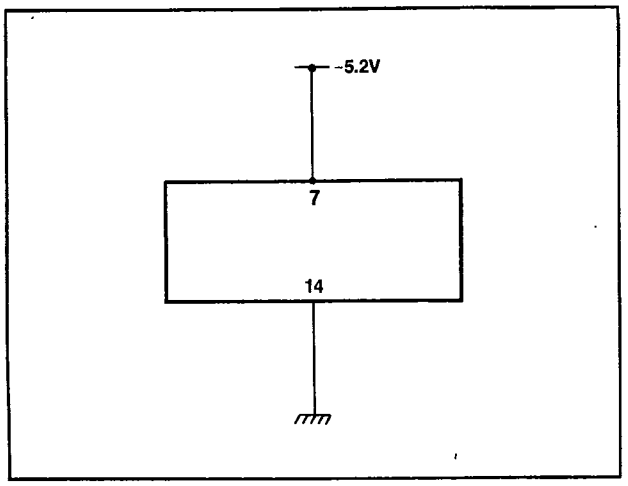
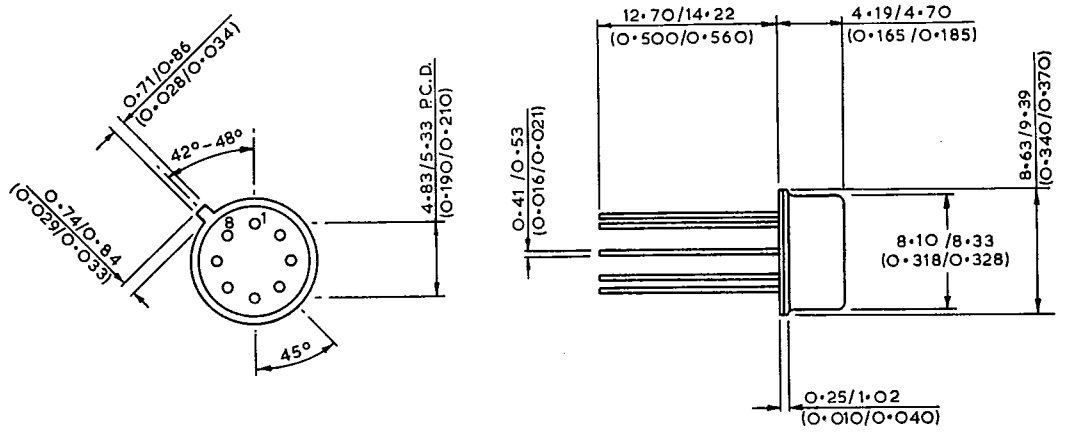
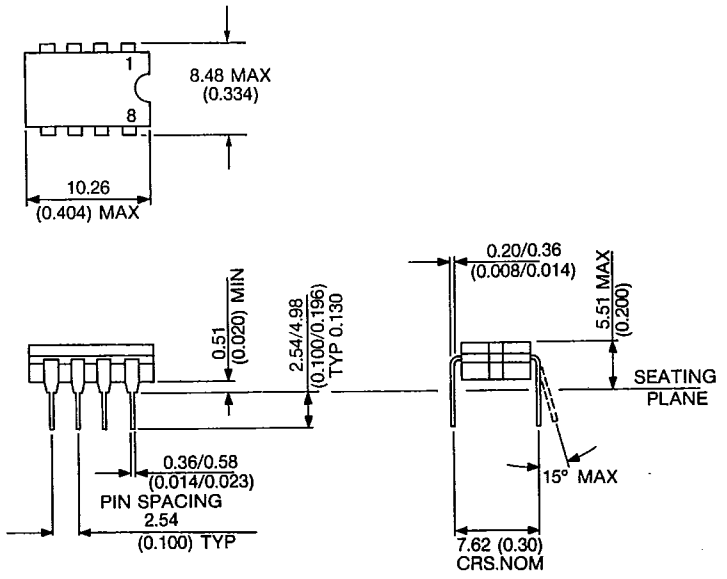


Fig.7 Burn-in/Life test circuit
NOTES (1) PDA is 5% and based on sub groups 1 and 7



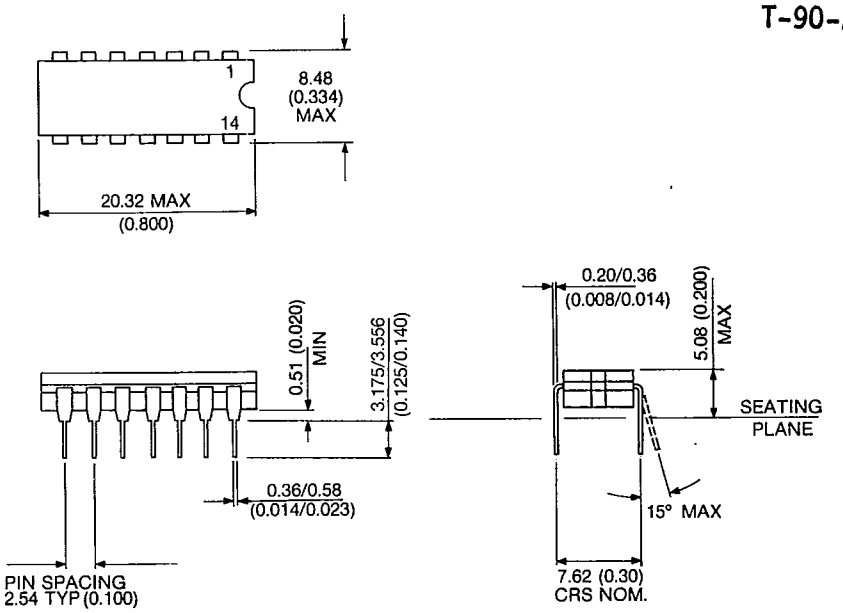
NOTE: This package does not have 'standoff' and therefore does not conform fully to MIL-M-38510F case outline A-1.

8-LEAD METAL CAN

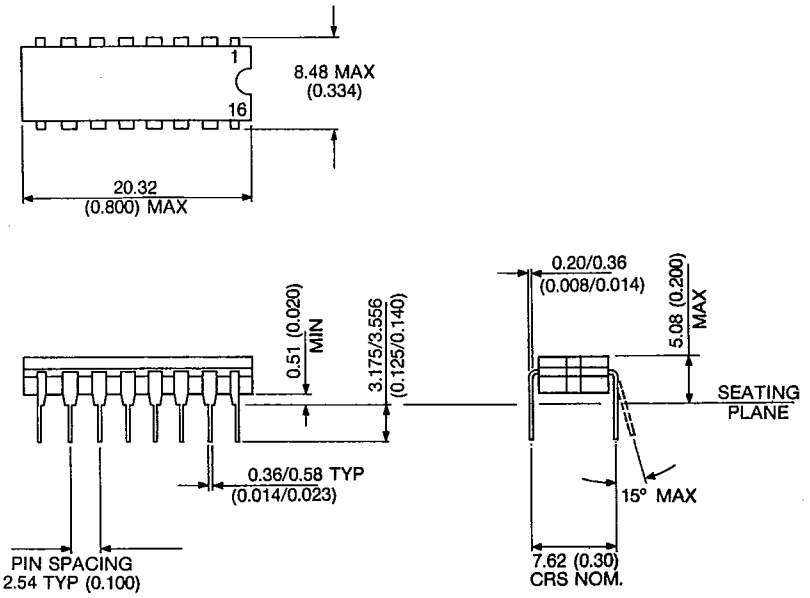


8 LEAD CERAMIC DIL CERDIP - DG8

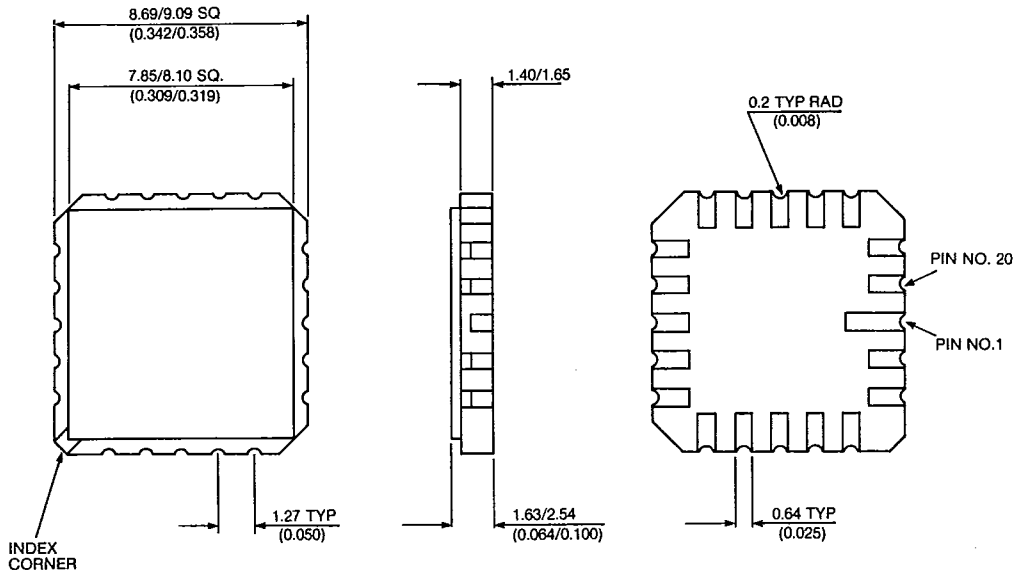
T-90-20



14 LEAD CERAMIC DIL CERDIP - DG14



16 LEAD CERAMIC DIL CERDIP - DG16



20-PIN LEADLESS CHIP CARRIER - LC20
(HERMETIC)