Very Low Phase Noise 300MHz ÷10/11

Supersedes February 1992 edition

DS3230 - 3.1 April 1994

The SP8401 is a very low phase noise variable modulus divider. Special circuit techniques have been used to reduce the phase noise considerably below that produced by standard dividers. The modulus control input is CMOS or TTL compatible.

The SP8401 is packaged in a 28 pin plastic SO package to be compatible with the SP8400 and SP8402 devices.

FEATURES

- Very low Phase Noise (Typically -160dBc/Hz at 1kHz offset)
- Supply Voltage 5V

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6.5V
Output Current 20mA
Storage Temperature Range -55°C to +125°C
Maximum Clock Input Voltage 2.5V p-p

ORDERING INFORMATION

SP8401 KG MPES(Commercial Grade)

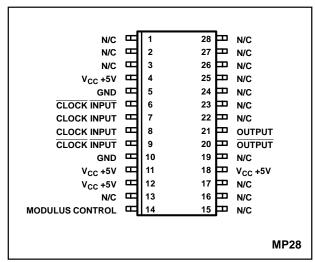


Fig.1 Pin connections - top view

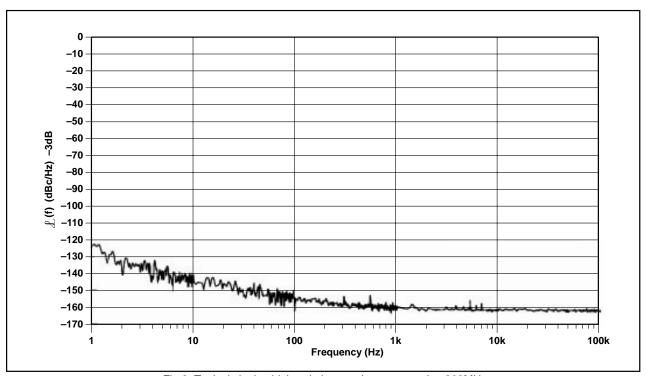


Fig.2 Typical single sideband phase noise measured at 300MHz

ELECTRICAL CHARACTERISTICS

Guaranteed over: Supply voltage V_{CC} = +4.75V to +5.25V Temperature T_{amb} = -10°C to +75°C Tested at +4.75V and +5.25V at T_{amb} = +25°C

Characteristic	Pin	Value			Units	Conditions
Cital acteristic	FIII	Min.	Тур.	Max.		Conditions
Supply current	4, 11, 12, 18	50	57	64	mA	Output loaded with 300R See Fig.5
Output voltage swing	20, 21	340	440		mV	p-p @ 330MHz input ÷ 11 mode
						Output loaded with 300R
Input sensitivity 50MHz to 300MHz	7, 8			140	mV	RMS Sine wave into 50 Ohms
				(-4)	dBm	(dBm equivalent) See Fig.3
Modulus Control Inputs						
Logic high voltage	14	2.2			V	÷ 10 mode
Low low voltage	14			0.8		÷ 11 mode
Input current	14			180	μΑ	Modulus control input voltage 5V
Set up time t _s	14		4		ns	
Release time t _r	14		4		ns	

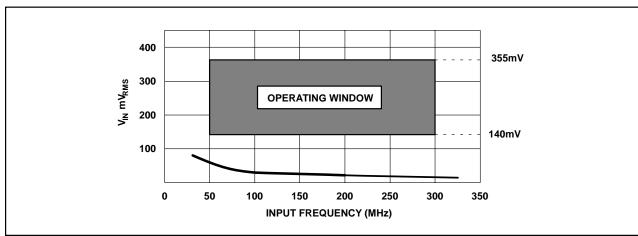


Fig.3 Typical input sensitivity

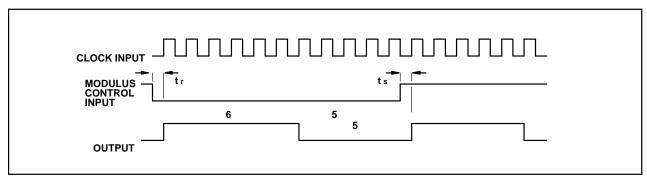


Fig.4 Timing diagram

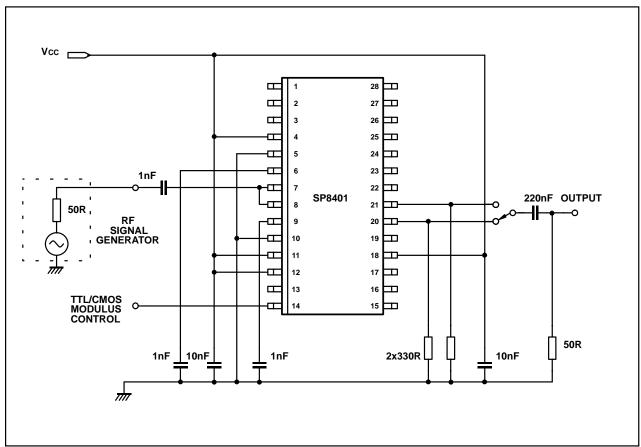
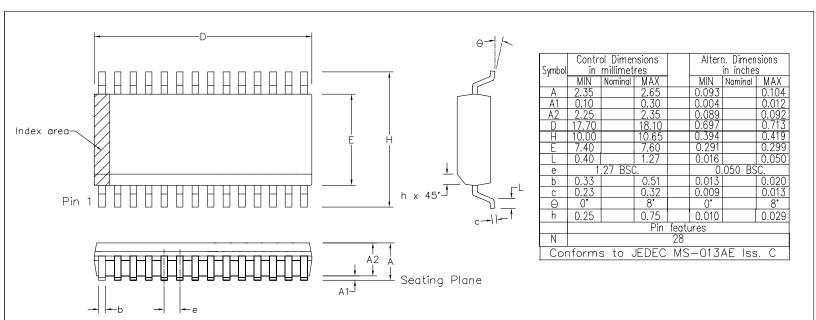


Fig.4 Test circuit



- 1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
- 2. Controlling dimension are in millimeters.

- Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
 Dimension E1 do not include inter—lead flash or protusion. These shall not exceed 0.010" per side.
 Dimension b does not include dambar protusion/intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

(C) Mitel				ORIGINATING SITE: SWINDON			
ISSUE	1	2					Title: Package Outline Drawing for 28 Ids SOIC(W)-0.300" Body Width (MP)
ACN	006746	201943				SEMICONDUCTOR	
DATE	7APR95	27FEB97					Drawing Number GPD00017
APPROVED							



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