



T-46-23-14

## UM62256 Series

### 32K × 8 CMOS SRAM

#### Features

- Single +5 volt power supply
- Access times: 100/120/150 ns (max.)
- Current:
  - Standard version: Operating: 70 mA (max.)  
Standby: 2 mA (max.)
  - Low power version: Operating: 70 mA (max.)  
Standby: 100 μA (max.)
- Fully static operation, no clock or refreshing required
- Directly TTL compatible: All inputs and outputs
- Common I/O using three-state output.
- Data retention voltage: 2V (min.) for low power version
- Available in 28 pin DIP or SOP packages (See ordering information)

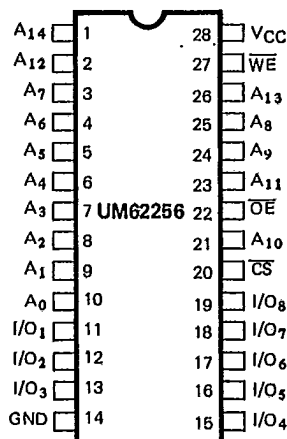


#### General Description

The UM62256 is a high-speed, low-power 262,144-bit static random access memory organized as 32,768 words by 8 bits and operates on a single 5-volt power supply. It is built using UMC's high performance CMOS process.

Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

#### Pin Configuration

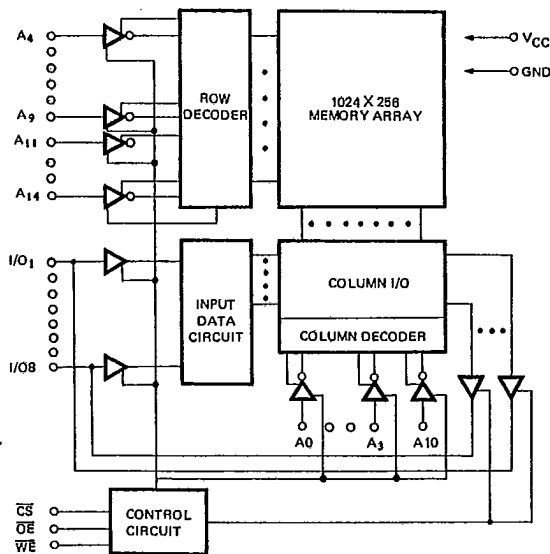


structures.

Minimum standby power is drawn by this device when  $\overline{CS}$  is at a high level, independent of the other input levels.

Data retention is guaranteed at a power supply voltage as low as 2V for the low power version.

#### Block Diagram





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**Pin Description**

Designation	Description
A <sub>0</sub> - A <sub>14</sub>	Address Input
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
I/O <sub>1</sub> - I/O <sub>8</sub>	Data Input/Output
V <sub>CC</sub>	Power Supply (+5V)
GND	Ground

**Recommended DC Operating Conditions**

(T<sub>A</sub> = 0°C to +70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	3.5	V <sub>CC</sub> + 0.5V	V
V <sub>IL</sub>	Input Low Voltage	-0.3	0	+0.8	V
C <sub>L</sub>	Output Load	-	-	100	pF
TTL	Output Load	-	-	1	-

**Absolute Maximum Ratings\***

V<sub>CC</sub> to GND ..... -0.5V to +7.0V  
 IN, IN/OUT Volt to GND ..... -0.5V to V<sub>CC</sub> +0.5V  
 Operating Temperature, T<sub>opr</sub> ..... 0°C to +70°C  
 Storage Temperature, T<sub>stg</sub> ..... -55°C to +125°C  
 Temperature Under Bias, T<sub>blas</sub> ..... -10°C to +85°C  
 Power Dissipation, P<sub>T</sub> ..... 1.0W/SOP 0.7W  
 Soldering Temp. & Time ..... 206°C, 10 sec

**\*Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**DC Electrical Characteristics** (T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = 5V ± 10%, GND = 0V)

Symbol	Parameter	UM62256-10/ 12/15		UM62256-10L/ 12L/15L		Unit	Test Conditions
		Min.	Max.	Min.	Max.		
I <sub>LI</sub>	Input Leakage Current	-	2	-	2	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current	-	2	-	2	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V <sub>I/O</sub> = GND to V <sub>CC</sub>
I <sub>CC</sub>	Active Power Supply Current	-	70	-	70	mA	$\overline{CS} = V_{IL}$ , I <sub>I/O</sub> = 0 mA
I <sub>CC1</sub>	Dynamic Operating Current	-	70	-	70	mA	Min. Cycle, Duty = 100% $\overline{CS} = V_{IL}$ , I <sub>I/O</sub> = 0 mA
I <sub>SB</sub>	Standby Power Supply Current	-	5	-	3	mA	$\overline{CS} = V_{IH}$
I <sub>SB1</sub>		-	2	-	0.1	mA	$\overline{CS} \geq V_{CC} - 0.2$ , V <sub>IN</sub> $\geq V_{CC} - 0.2V$ or V <sub>IN</sub> $\leq 0.2V$
V <sub>OL</sub>	Output Low Voltage	-	0.4	-	0.4	V	I <sub>OL</sub> = 4 mA
V <sub>OH</sub>	Output High Voltage	2.4	-	2.4	-	V	I <sub>OH</sub> = -1.0 mA



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**Truth Table**

Mode	CS	OE	WE	I/O Operation	Supply Current
Standby	H	X	X	High Z	I <sub>SB</sub> , I <sub>SB1</sub>
Output Disable	L	H	H	High Z	I <sub>CC</sub> , I <sub>CC1</sub>
Read	L	L	H	D <sub>OUT</sub>	I <sub>CC</sub> , I <sub>CC1</sub>
Write	L	X	L	D <sub>IN</sub>	I <sub>CC</sub> , I <sub>CC1</sub>

Note: X : H or L

**Capacitance** (T<sub>A</sub> = 25°C, f = 1.0 MHz)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
C <sub>IN</sub> *	Input Capacitance		6	pF	V <sub>IN</sub> = 0V
C <sub>I/O</sub> *	Input/Output Capacitance		8	pF	V <sub>I/O</sub> = 0V

Standard SRAM

\* This parameter is sampled and not 100% tested.

**AC Characteristics** (T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = 5V ± 10%)

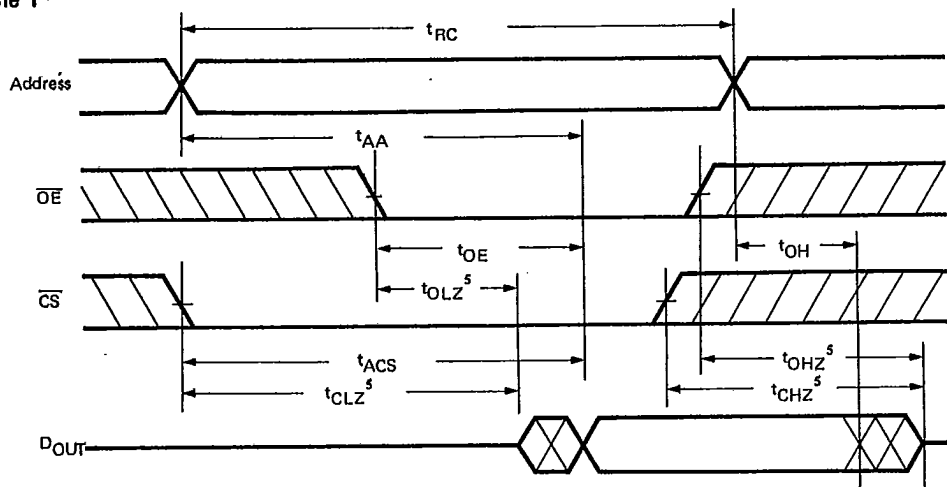
Symbol	Parameter	UM62256-10 UM62256-10L		UM62256-12 UM62256-12L		UM62256-15 UM62256-15L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>								
t <sub>RC</sub>	Read Cycle Time	100	—	120	—	150	—	ns
t <sub>AA</sub>	Address Access Time	—	100	—	120	—	150	ns
t <sub>ACS</sub>	Chip Select Access Time	—	100	—	120	—	150	ns
t <sub>OE</sub>	Output Enable to Output Valid	—	50	—	60	—	70	ns
t <sub>CLZ</sub>	Chip Selection to Output in Low Z	10	—	10	—	10	—	ns
t <sub>OLZ</sub>	Output Enable to Output in Low Z	5	—	5	—	5	—	ns
t <sub>CHZ</sub>	Chip Deselection to Output in High Z	0	35	0	40	0	50	ns
t <sub>OHZ</sub>	Output Disable to Output in High Z	0	35	0	40	0	50	ns
t <sub>OH</sub>	Output Hold from Address Change	10	—	10	—	10	—	ns
<b>Write Cycle</b>								
t <sub>WC</sub>	Write Cycle Time	100	—	120	—	150	—	ns
t <sub>CW</sub>	Chip Selection to End of Write	80	—	85	—	100	—	ns
t <sub>AS</sub>	Address Set up Time	0	—	0	—	0	—	ns
t <sub>AW</sub>	Address Valid to End of Write	80	—	85	—	100	—	ns
t <sub>WP</sub>	Write Pulse Width	60	—	70	—	90	—	ns
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	ns
t <sub>WHZ</sub>	Write to Output in High Z	0	35	0	40	0	50	ns
t <sub>DW</sub>	Data to Write Time Overlap	40	—	50	—	60	—	ns
t <sub>DH</sub>	Data Hold from Write Time	0	—	0	—	0	—	ns
t <sub>OHZ</sub>	Output Disable to Output in High Z	0	35	0	40	0	50	ns
t <sub>OW</sub>	Output Active from End of Write	10	—	10	—	10	—	ns



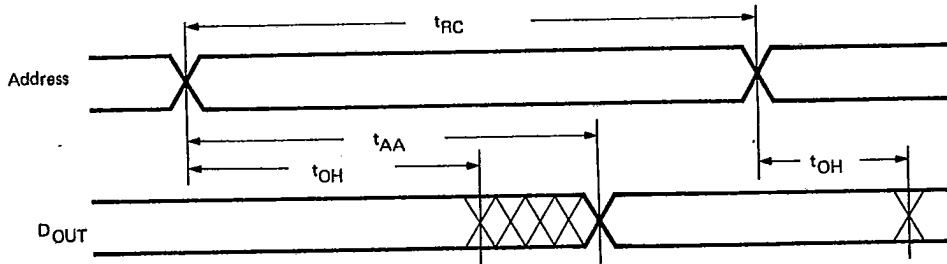
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**Timing Waveforms**

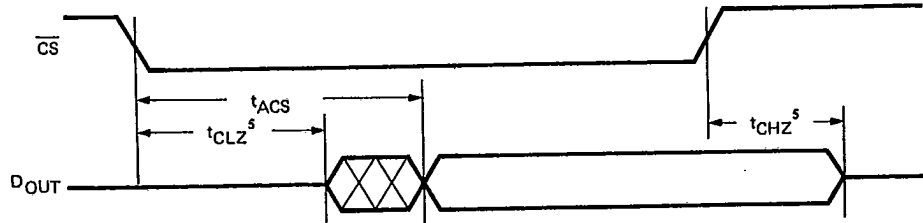
**Read Cycle 1 (1)**



**Read Cycle 2 (1, 2, 4)**



**Read Cycle 3 (1, 3, 4)**



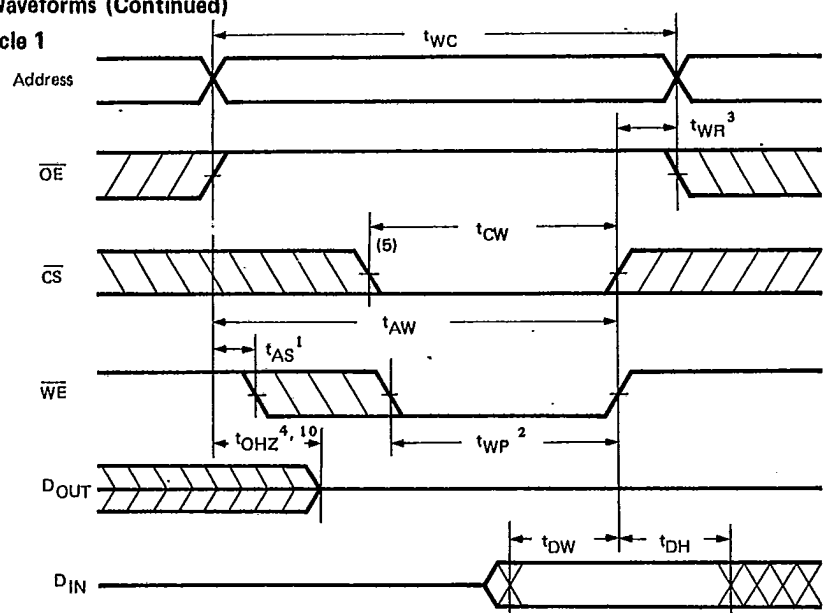
- Notes: 1.  $\overline{WE}$  is High for Read Cycle,  
 2. Device is continuously selected,  $\overline{CS} = V_{IL}$ .  
 3. Address valid prior to or coincident with  $\overline{CS}$  transition low.  
 4.  $OE = V_{IL}$ .  
 5. Transition is measured  $\pm 500mV$  from steady state. This parameter is sampled and not 100% tested.



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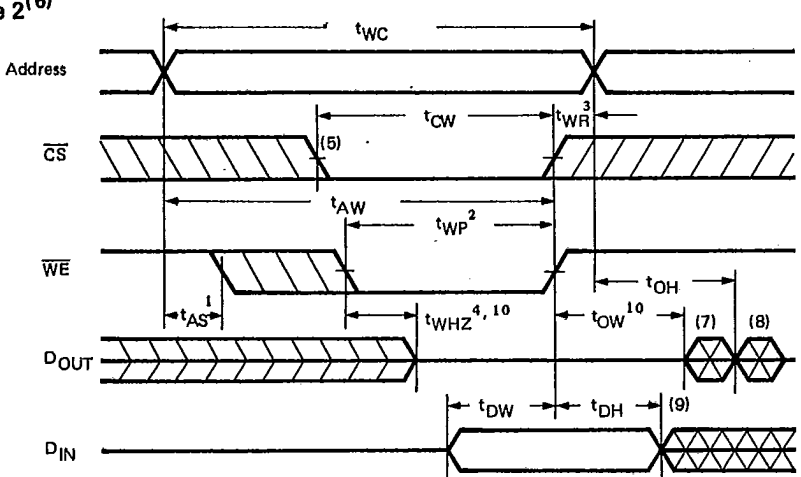
**Timing Waveforms (Continued)**

**Write Cycle 1**



Standard  
 SRAM

**Write Cycle 2<sup>(6)</sup>**



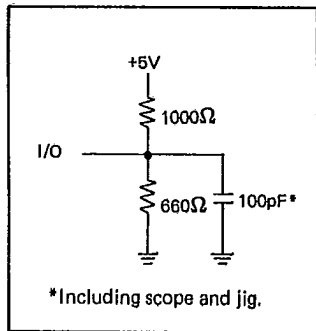
- Notes:
1.  $t_{AS}$  is measured from the address valid to the beginning of write.
  2. A write occurs during the overlap ( $t_{WP}$ ) of a low  $\overline{CS}$  and a low  $\overline{WE}$ .
  3.  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going high to the end of write cycle.
  4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
  5. If the  $\overline{CS}$  low transition occurs simultaneously with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  transition, outputs remain in a high impedance state.
  6.  $\overline{OE}$  is continuously low ( $\overline{OE} = V_{IL}$ ).
  7.  $D_{OUT}$  is the same phase of write data of this write cycle.
  8.  $D_{OUT}$  is the read data of next address.
  9. If  $\overline{CS}$  is low during this period, I/O pins are in the output state, Data input signals of opposite phase to the outputs must not be applied to I/O pins.
  10. Transition is measured  $\pm 500mV$  from steady state. This parameter is sampled and not 100% tested.



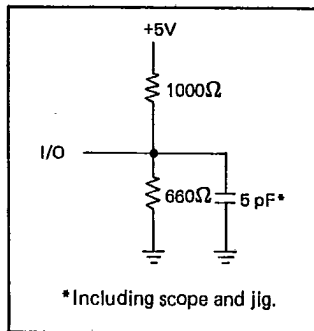
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**AC Test Conditions**

Input Pulse Levels	0.8V to 2.2V
Input Rise and Fall Times	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1, 2



**Figure 1. Output Load**



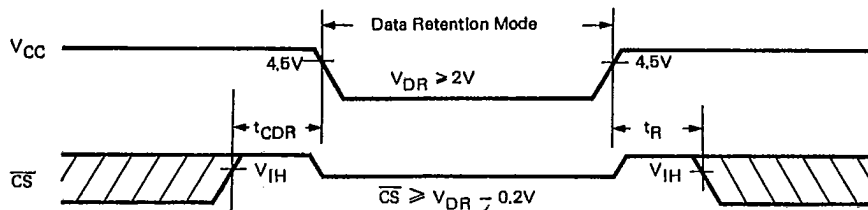
**Figure 2. Output Load for  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$ , and  $t_{OW}$**

**Data Retention Characteristics** ( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ; L version only)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
$V_{DR}$	$V_{CC}$ for Data Retention	2.0	5.5	V	$\overline{CS} \geq V_{CC} - 0.2\text{V}$
$I_{CCDR}$	Data Retention Current	—	50	$\mu\text{A}$	$V_{CC} = 3.0\text{V}$ , $\overline{CS} \geq V_{CC} - 0.2\text{V}$ $V_{IN} \geq V_{CC} - 0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$
$t_{CDR}$	Chip Deselect to Data Retention Time	0	—	ns	See Retention
$t_R$	Operation Recovery Time	$t_{RC}^*$	—	ns	Waveform

\* $t_{RC}$  = Read Cycle Time

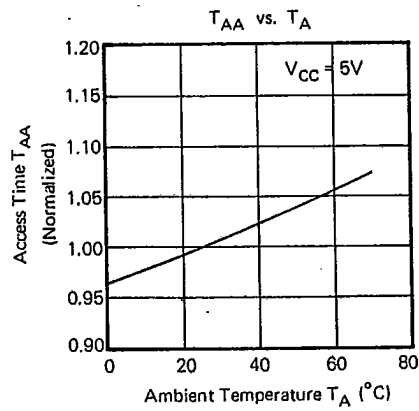
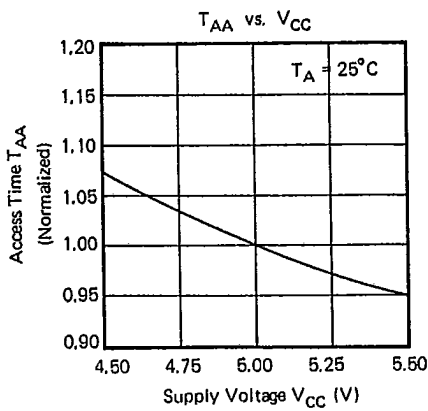
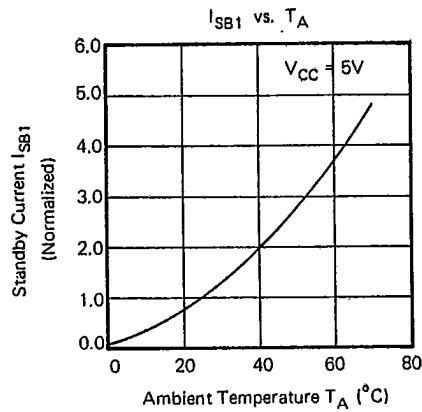
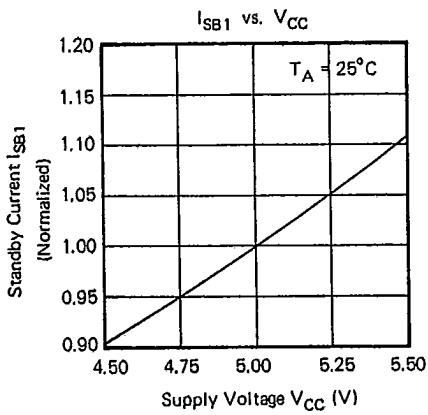
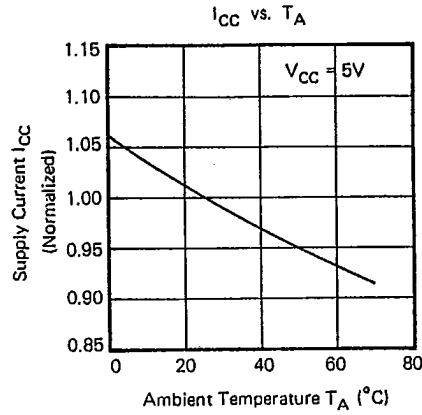
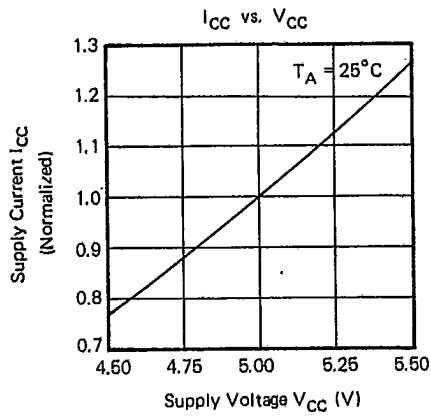
**Timing Waveform Low  $V_{CC}$  Data Retention Waveform**





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**Characteristic Curves**





T-46-23-14  
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**Ordering Information**

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Package
UM62256-10	100 ns	70	2	28L DIP
UM62256-10L	100 ns	70	0.1	28L DIP
UM62256M-10	100 ns	70	2	28L SOP
UM62256M-10L	100 ns	70	0.1	28L SOP
UM62256-12	120 ns	70	2	28L DIP
UM62256-12L	120 ns	70	0.1	28L DIP
UM62256M-12	120 ns	70	2	28L SOP
UM62256M-12L	120 ns	70	0.1	28L SOP
UM62256-15	150 ns	70	2	28L DIP
UM62256-15L	150 ns	70	0.1	28L DIP
UM62256M-15	150 ns	70	2	28L SOP
UM62256M-15L	150 ns	70	0.1	28L SOP