October 1997

FAIRCHILD SEMICONDUCTOR TM

FDC6320C
Dual N & P Channel , Digital FET

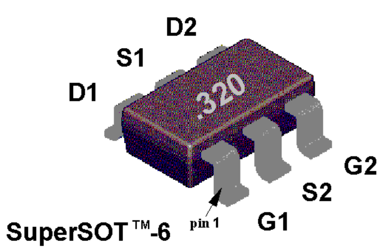
General Description

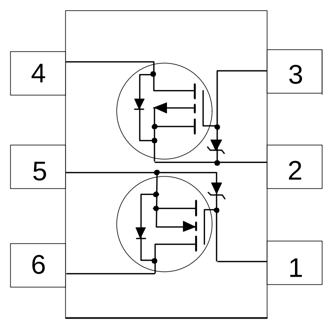
These dual N & P Channel logic level enhancement mode field effec transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. The device is an improved design especially for low voltage applications as a replacement for bipolar digital transistors in load switching applications. Since bias resistors are not required, this dual digital FET can replace several digital transistors with difference bias resistors.

Features

- N-Ch 25 V, 0.22 A, $R_{DS(ON)}$ = 5 Ω @ V_{GS}= 2.7 V.
- P-Ch 25 V, -0.12 A, $R_{DS(ON)}$ = 13 Ω @ V_{GS}= -2.7 V.
- Very low level gate drive requirements allowing direct operation in 3 V circuits. $V_{GS(th)}$ < 1.5 V.
- Gate-Source Zener for ESD ruggedness. >6kV Human Body Model
- Replace NPN & PNP digital transistors.

SOT-23 | SuperSOT™-6 | SuperSOT™-8 | SO-8 | SOT-223 | SOIC-16





Absolute Maximum Ratings T_A = 25°C unless other wise noted

Symbol	Parameter		N-Channel	P-Channel	Units
V_{DSS}, V_{CC}	Drain-Source Voltage, Power Supply Voltage		25	-25	V
V_{GSS}, V_{IN}	Gate-Source Voltage,		8	-8	V
I_D, I_O	Drain/Output Current	- Continuous	0.22	-0.12	A
		- Pulsed	0.5	-0.5	
P_D	Maximum Power Dissipation	(Note 1a)	0.9		W
		(Note 1b)	0.7		
T_J,T_{STG}	Operating and Storage Tempature Ranger		-55 to 150		°C
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pf / 1500 Ohm)		6		kV
THERMAL CHARACTERISTICS					
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	140		°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	60		°C/W

DMOS Electrical Characteristics (T_A = 25 °C unless otherwise noted)

Symbol	Parameter	Conditions		Type	Min	Typ	Max	Units
OFF CHARACTERISTICS								
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA		N-Ch	25			V
		V_{GS} = 0 V, I_D = -250 µA		P-Ch	-25			
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	I_D = 250 µA, Referenced to 25 °C		N-Ch		25		mV /°C
		I_D = -250 µA, Referenced to 25 °C		P-Ch		-20		
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}= 20 V, V_{GS}= 0 V,		N-Ch			1	µA
			T_J = 55°C				10	
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} =-20 V, V_{GS} = 0 V,		P-Ch			-1	µA
			T_J = 55°C				-10	
I_{GSS}	Gate - Body Leakage Current	V_{GS} = 8 V, V_{DS}= 0 V		N-Ch			100	nA
		V_{GS} = -8 V, V_{DS}= 0 V		P-Ch			-100	nA
ON CHARACTERISTICS (Note 2)								
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	I_D = 250 µA, Referenced to 25 °C		N-Ch		-2.1		mV / °C
		I_D= -250 µA, Referenced to 25 °C		P-Ch		1.9		
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D= 250 µA		N-Ch	0.65	0.85	1.5	V
		V_{DS} = V_{GS}, I_D= -250 µA		P-Ch	-0.65	-1	-1.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 2.7 V, I_D = 0.2 A		N-Ch		3.8	5	Ω
			T_J =125°C			6.3	9	
		V_{GS} = 4.5 V, I_D = 0.4 A				3.1	4	
		V_{GS} = -2.7 V, I_D = -0.05 A		P-Ch		10.6	13	
			T_J =125°C			15	21	
		V_{GS} = -4.5 V, I_D = -0.2 A				7.9	10	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = 2.7 V, V_{DS} = 5 V		N-Ch	0.2			A
		V_{GS} = -2.7 V, V_{DS} = -5 V		P-Ch	-0.05			
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D= 0.4 A		N-Ch		0.2		S
		V_{DS} = -5 V, I_D= -0.2 A		P-Ch		0.135		
DYNAMIC CHARACTERISTICS								
C_{iss}	Input Capacitance	N-Channel V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz		N-Ch		9.5		pF
				P-Ch		11		
C_{oss}	Output Capacitance			N-Ch		6		pF
		P-Channel V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		P-Ch		7		
C_{rss}	Reverse Transfer Capacitance			N-Ch		1.3		pF
				P-Ch		1.4		

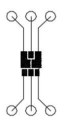
DMOS Electrical Characteristics (T_A = 25 ^oC unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	N-Channel	N-Ch		5	11	nS
		V_{DD} = 6 V, I_D = 0.5 A,	P-Ch		6	12	
t_r	Turn - On Rise Time	V_{GS} = 4.5 V, R_{GEN} = 50 Ω	N-Ch		4.5	10	nS
			P-Ch		6	12	
$t_{D(off)}$	Turn - Off Delay Time	P-Channel	N-Ch		4	10	nS
		V_{DD} = -6 V, I_D = -0.5 A,	P-Ch		7.4	15	
t_f	Turn - Off Fall Time	V_{GEN}= -4.5 V, R_{GEN} = 50 Ω	N-Ch		3.2	8	nS
			P-Ch		4	10	
Q_g	Total Gate Charge	N-Channel V_{DS} = 5 V, I_D = 0.2 A, V_{GS} = 4.5 V	N-Ch		0.29	0.4	nC
			P-Ch		0.23	0.32	
Q_{gs}	Gate-Source Charge		N-Ch		0.105		nC
		P-Channel V_{DS} = -5 V, I_D = -0.2A, V_{GS} = -4.5 V	P-Ch		0.12		
Q_{gd}	Gate-Drain Charge		N-Ch		0.045		nC
			P-Ch		0.03		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			0.5	A
			P-Ch			-0.5	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.5 A (Note 2)	N-Ch		0.97	1.3	V
		V_{GS} = 0 V, I_S = -0.5 A (Note 2)	P-Ch		-1	-1.3	

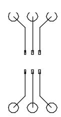
Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

Typical $R_{\theta JA}$ using the board layouts shown below on FR-4 PCB in a still air environment:



a. 140^{o}C/W on a 0.125 in^2 pad of 2oz copper.



b. 180^{o}C/W on a 0.005 in^2 of pad of 2oz copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics: N-Channel

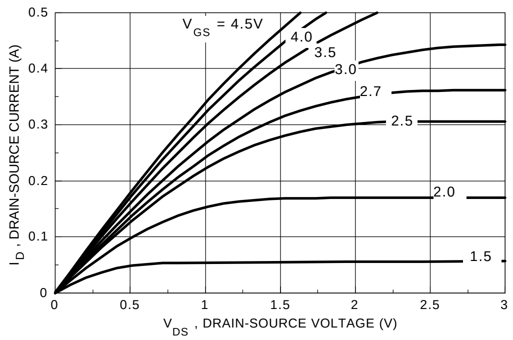


Figure 1. On-Region Characteristics.

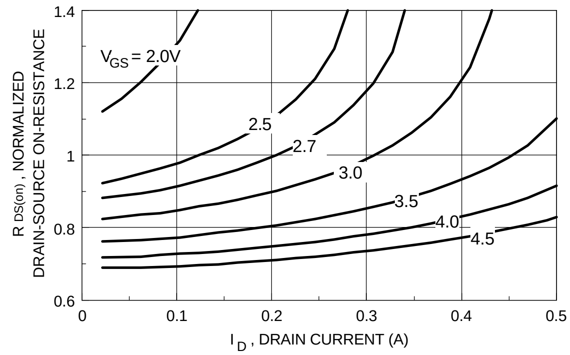


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

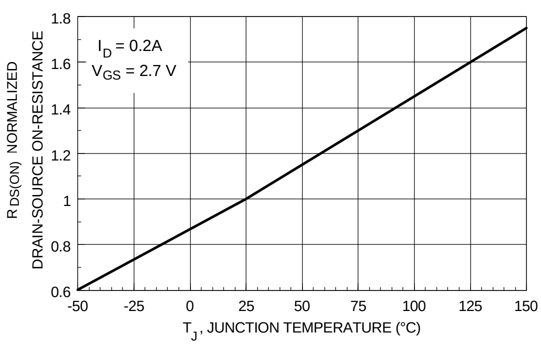


Figure 3. On-Resistance Variation with Temperature.

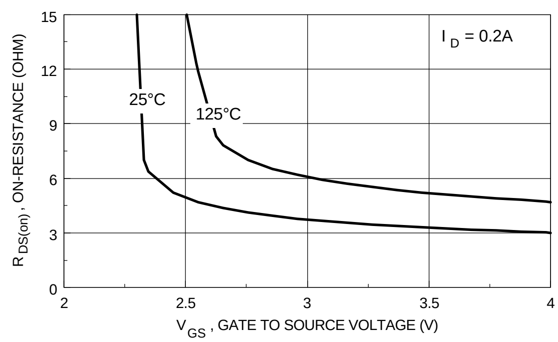


Figure 4. On Resistance Variation with Gate-To- Source Voltage.

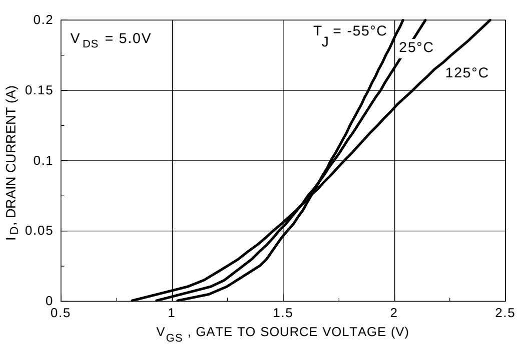


Figure 5. Transfer Characteristics.

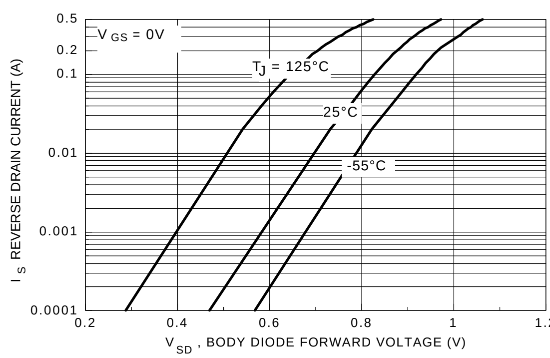


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics: N-Channel (continued)

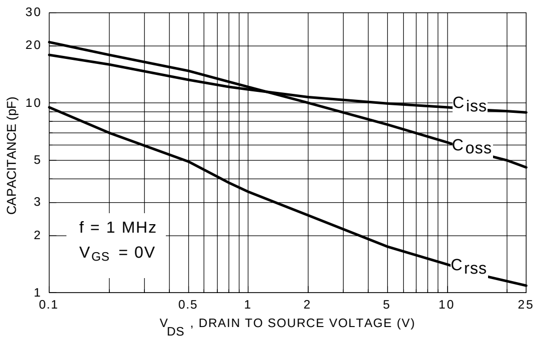


Figure 7. Capacitance Characteristics.

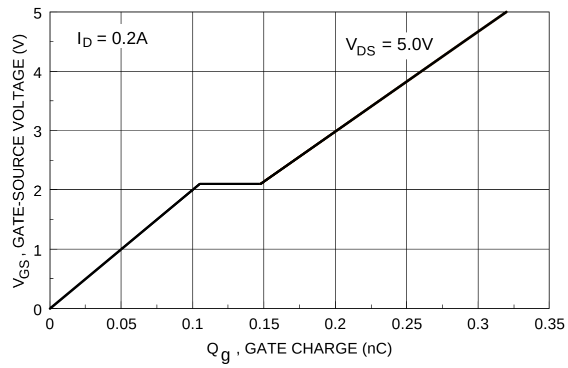


Figure 8. Gate Charge Characteristics.

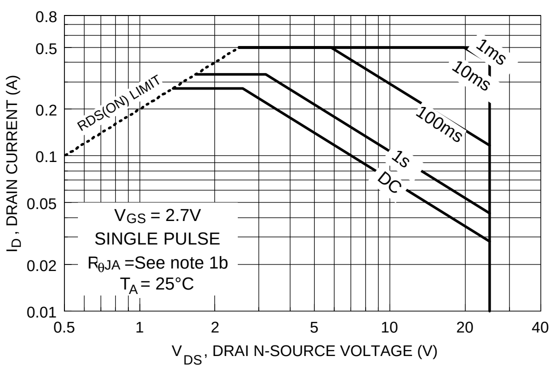


Figure 9. Maximum Safe Operating Area.

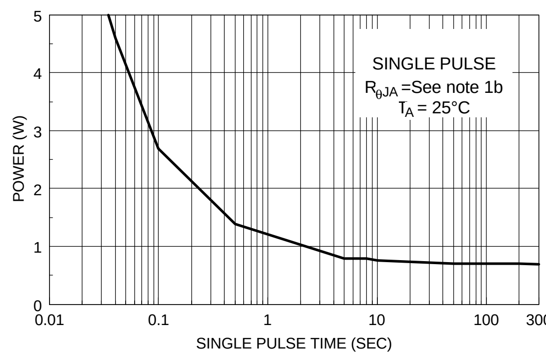


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Electrical Characteristics: P-Channel

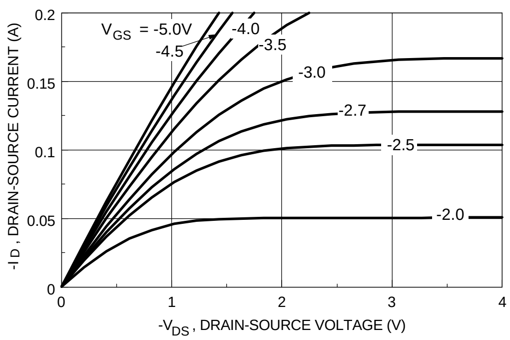


Figure 11. On-Region Characteristics.

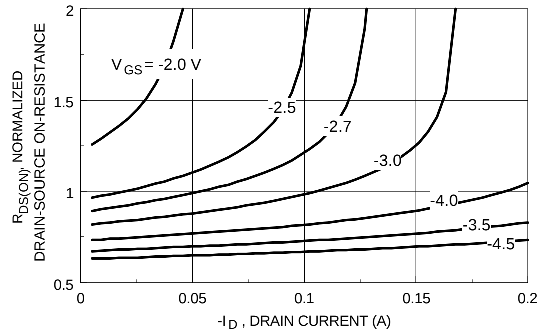


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

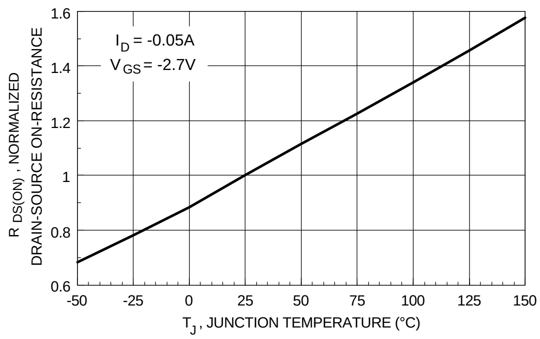


Figure 13. On-Resistance Variation with Temperature.

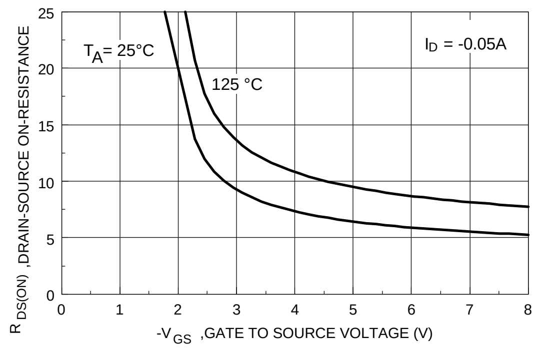


Figure 14. On Resistance Variation with Gate-To- Source Voltage.

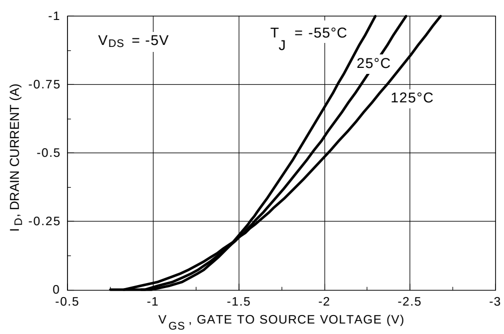


Figure 15. Transfer Characteristics.

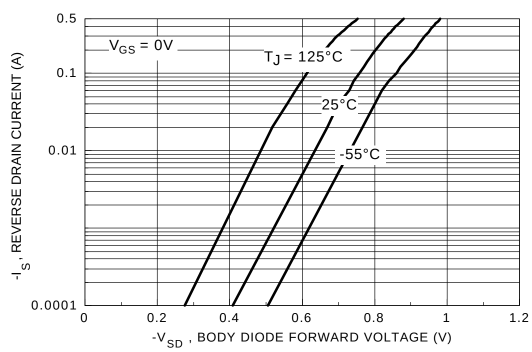


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics: P-Channel (continued)

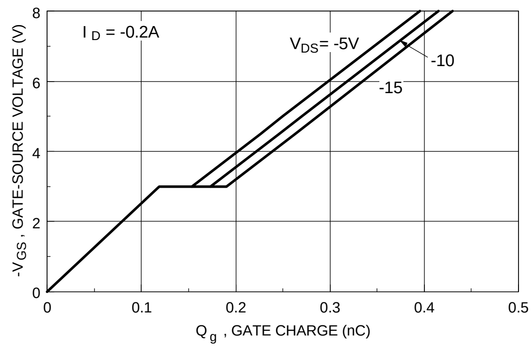


Figure 17. Gate Charge Characteristics.

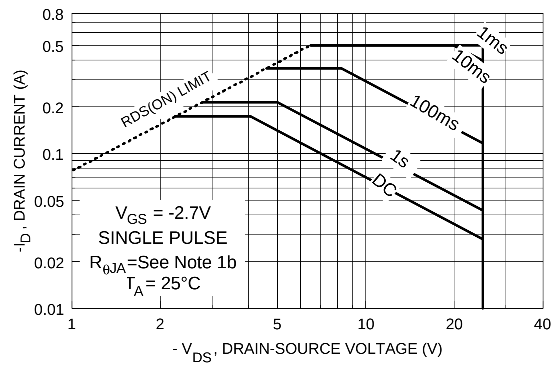


Figure 18. Maximum Safe Operating Area.

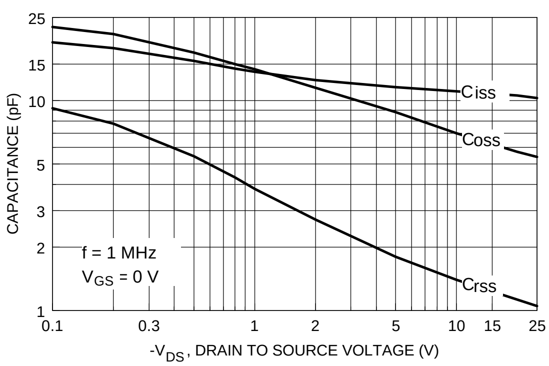


Figure 19. Capacitance Characteristics.

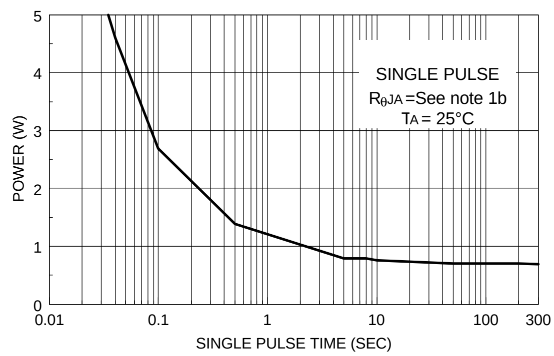


Figure 20. Single Pulse Maximum Power Dissipation.

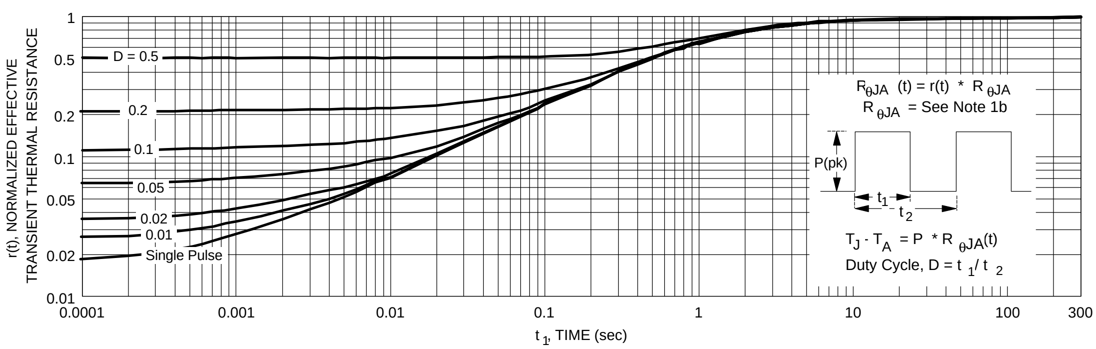


Figure 21. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1b.Transient thermal response will change depending on the circuit board design.